ASIC:

Status of resubmission/ List of changes/Left to do

AGIPD Collaboration meeting 11-13 November 2015

A. Klyuev et all ASIC designers for the AGIPD collaboration

List of patches applied: Top level

1. AOUT RC reduction: E1 instead of M2 in vertical direction, M3 instead of M1 at the bottom, better grounding of separation anti-crosstalk lines
2. Power_right changed: VDDA from E1 to MA
3. Improved vias (M2_M3) connecting the biasing and the AOUT input signals to the offchip driver
4. New power-up reset pad
5. New offchip driver with a buffered vref_chipbuf to suppress channel signal crosstalks through the biasing
6. New pixel layout (mostly MQ and up, improved contacts)
7. Added VDDA MA metal clamps from the right power group to the pixel matrix
8. Added vdda clamps from the right power group to the outmux
9. Added ground clamps from the pixel matrix to the output signal separators
10. Added M1 parallel to M2 VDDA bus in the outmux with corresponding via sets
11. Doubled mux clock and tokens buffers, new routing from the periphery

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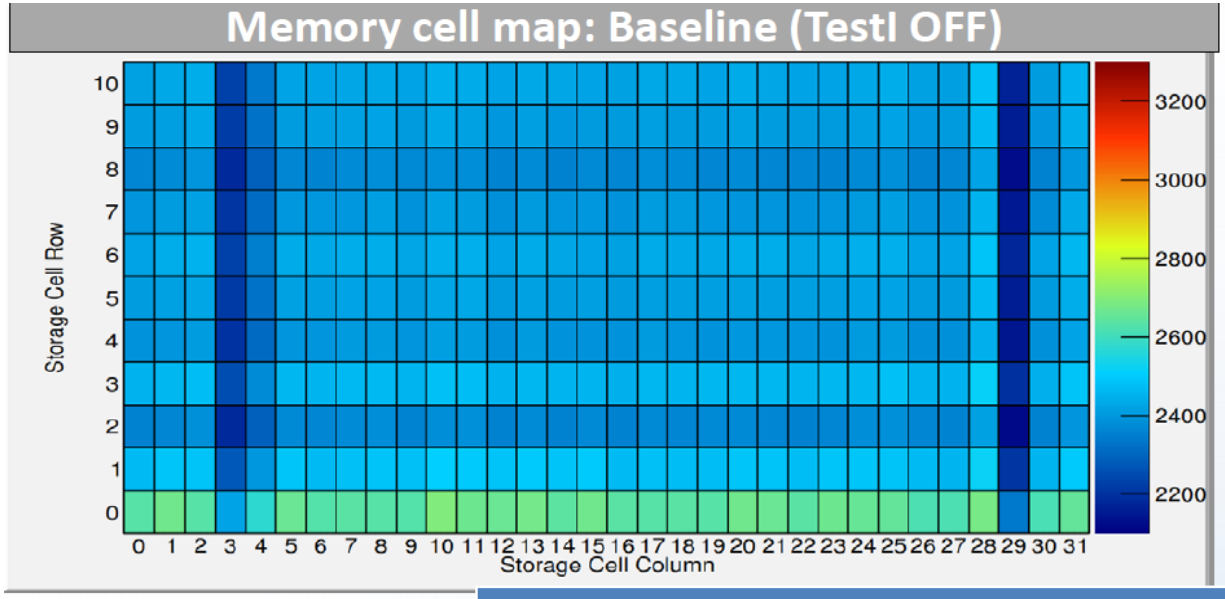
List of patches applied: Pixel

1. pixel_ma changed to have wider (and trough) vdd_pa vdd_pix and vss lines (MA, E1)
2. (D)MIM caps (e.g. pixelPowDecoupCap(1), filter_caps opa_ds..) layout and position changed
3. Orientation and connection (now via MA) of test pulse cap changed
4. MG: Rearranged bias (now over active part) control (no longer under preamp FB cap)and power (widened) lines
5. Increased # of vias for power (esp. FY FT F1)
6. Added MQ lines for power, filled MG crOssings with VGss
7. Added LY Shield under input pad
8. Increased # of vnwell_pix vias to wells
9. aux_calibr, preamp_3gain_highGain layout changes

Pixel improvements

AGIPD 1.0

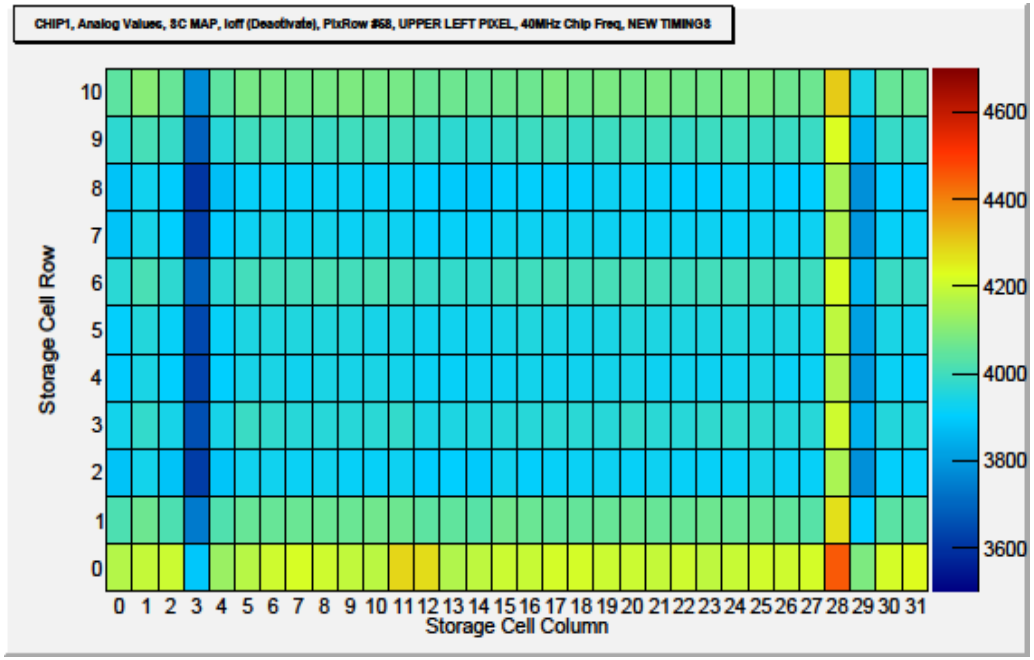
Crosstalk between address lines and analog circuitry nodes

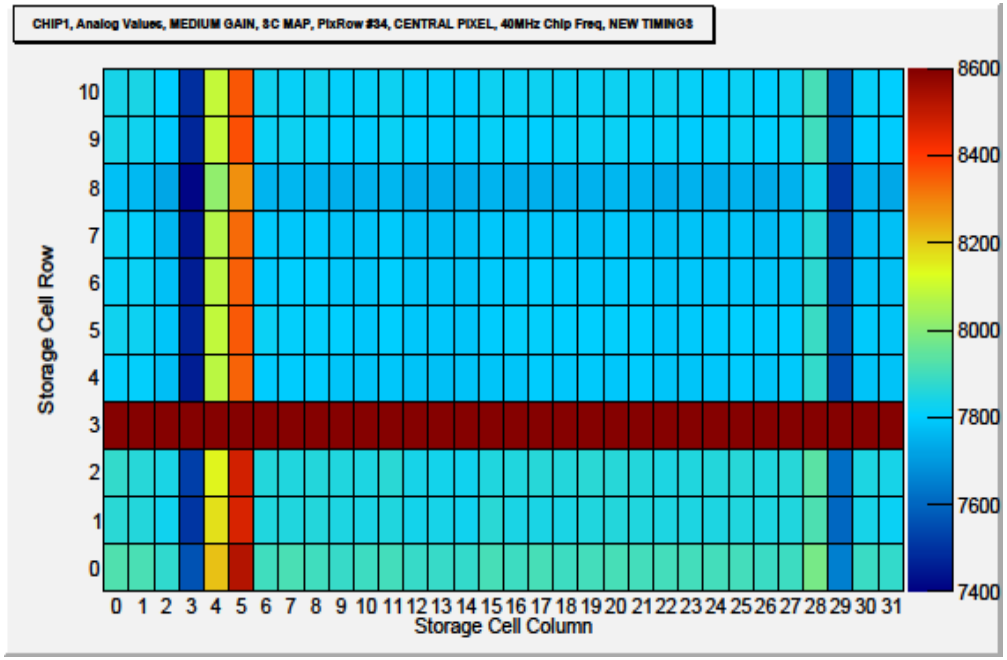


Several sources of crosstalk could be extracted and verified by simulations

Crosstalk between ...		Parasitic capacitance
MEMCOL3	$V_{ref,CDS}$	11.1 fF
MEMROW3	Test current load	20.0 fF
MEMROW0	Pixel input	5.35 fF
MEMCOL29	Vref,PXB	12.5 fF
MEMCOL29	Pix Out	18.3 fF

AGIPD10 vs AGIPD11 - Crosstalks

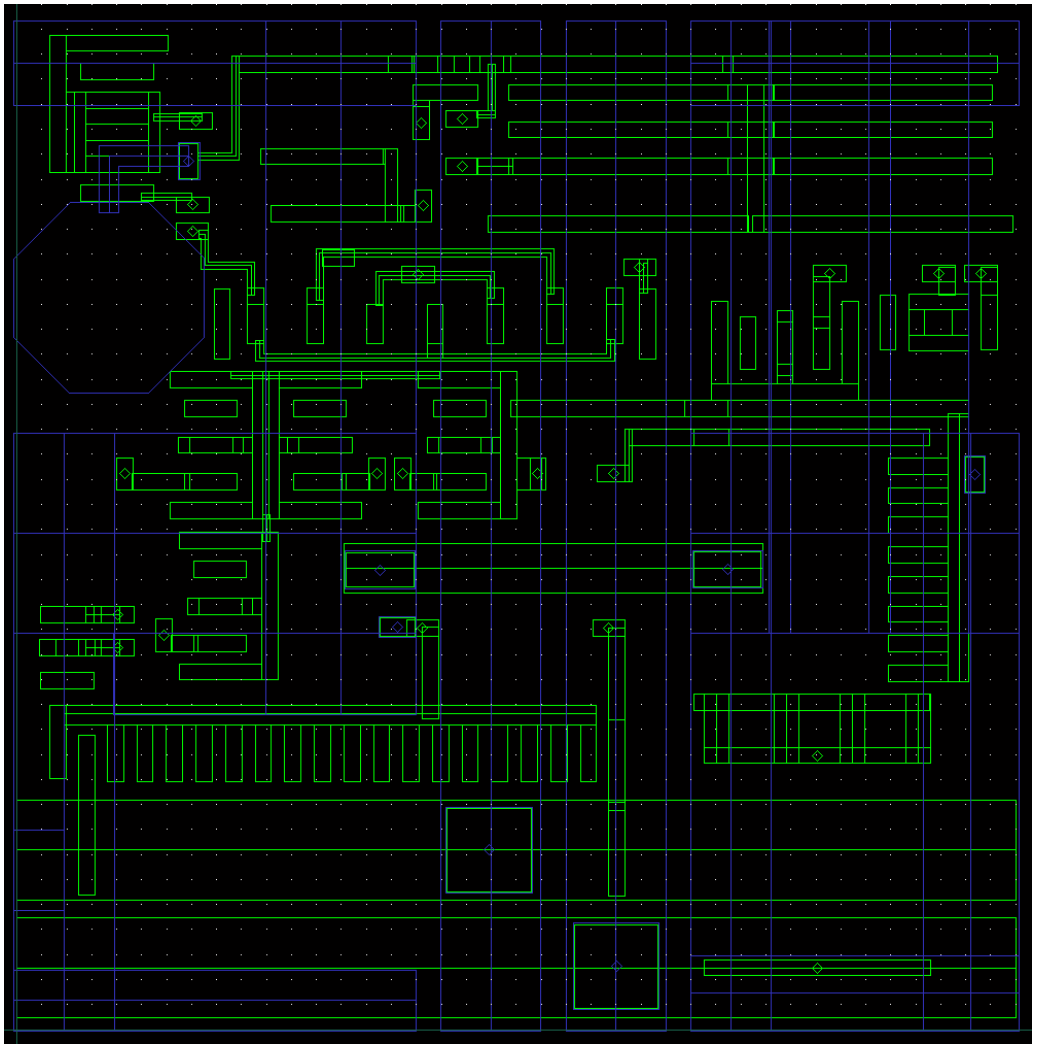




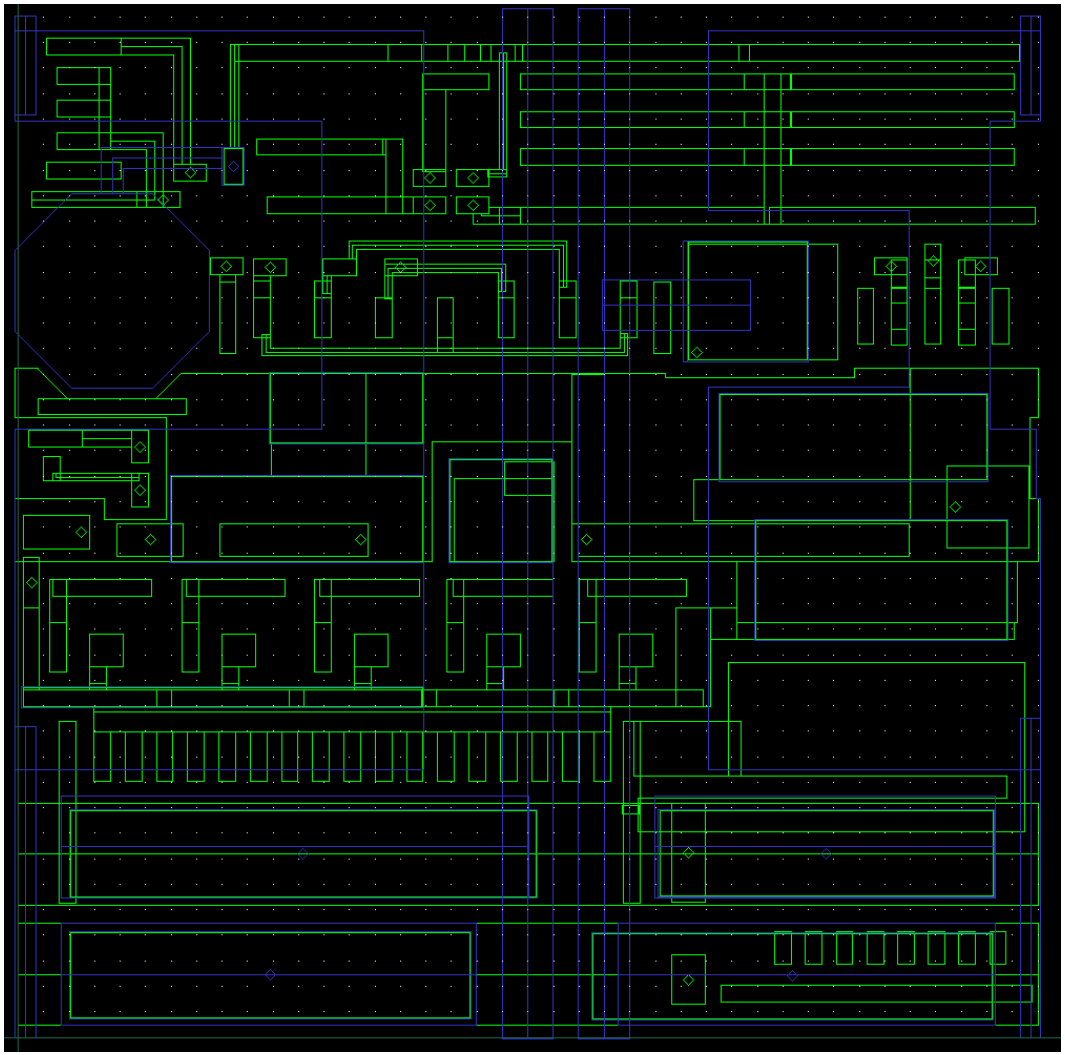
Parasitic Coupling	AGIPD10	AGIPD11
Row_SELA_0/pix_in	5.35 fF	< 1 fF
Col_SELA_3/Vrefcds	11 fF	1.2 fF
Row_SELA_3/test_curr	20 fF	< 1 fF
Col_SELA_29/Vrefpxb	12.5 fF	9.2 fF

Pixel improvements

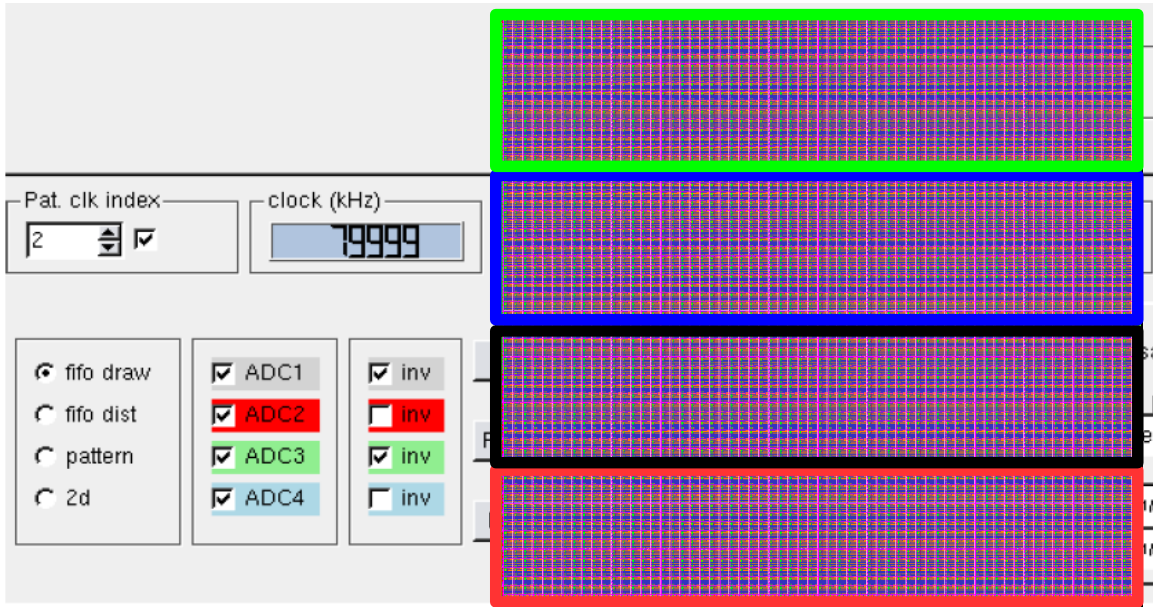
AGIPD 1.0



AGIPD 1.1

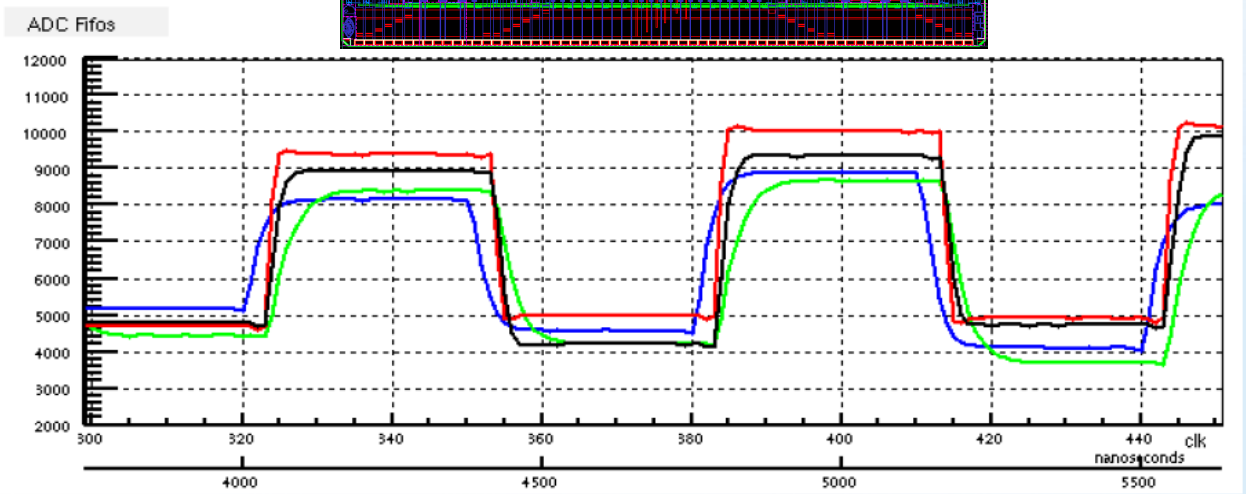


Output signal speed issue



- Waveform samples of output of AGIPD1.0
- Pattern clocked @40 MHz
  ADC clocked @80 MHz

→Clearly visible are:
- Different risetimes of ADCs
- Different pulseheights

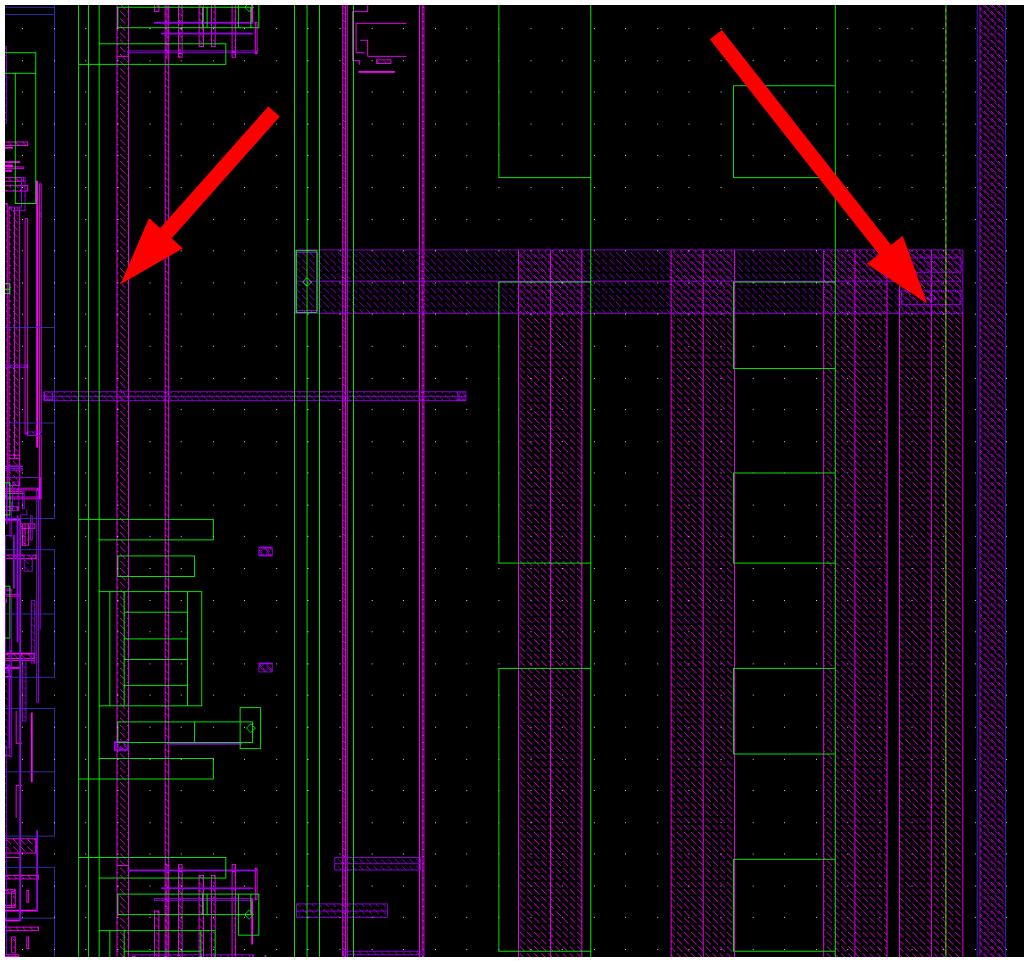


t_{10to90} measured:

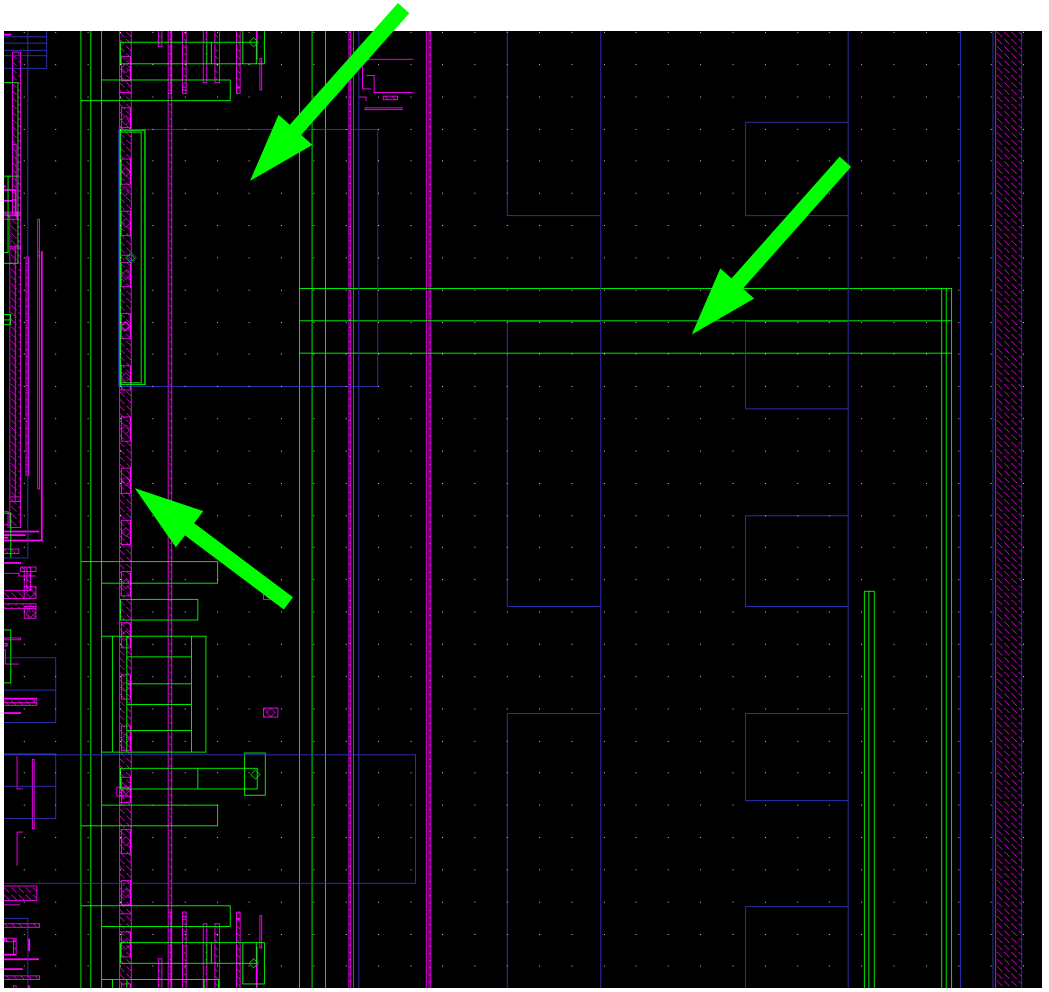
Wirebonds	
ADC2= Left	21 ns
ADC1= Center/Left	27 ns
ADC4= Center/Right	41 ns
ADC3= Right	56 ns

Output signal speed issue

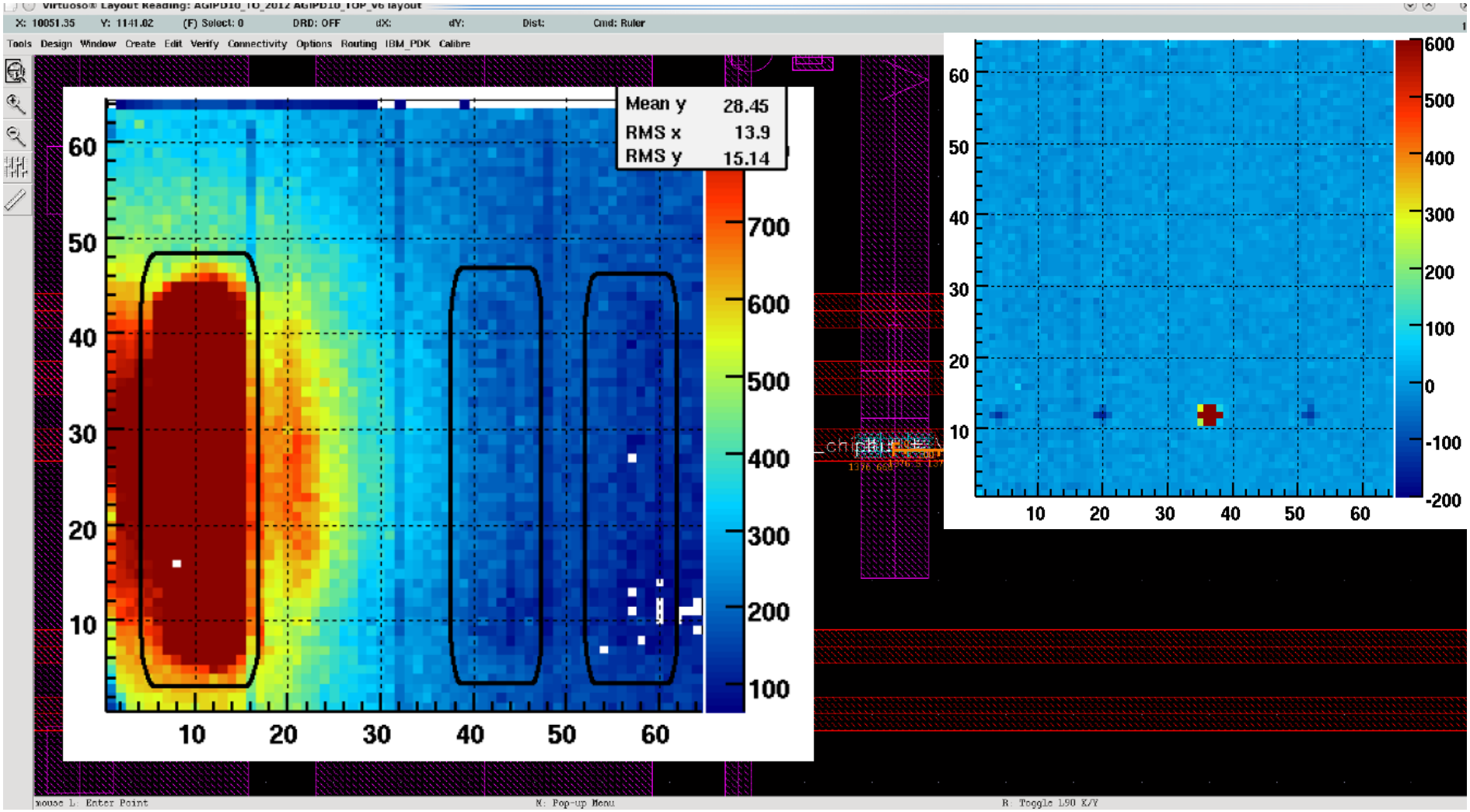
AGIPD 1.0



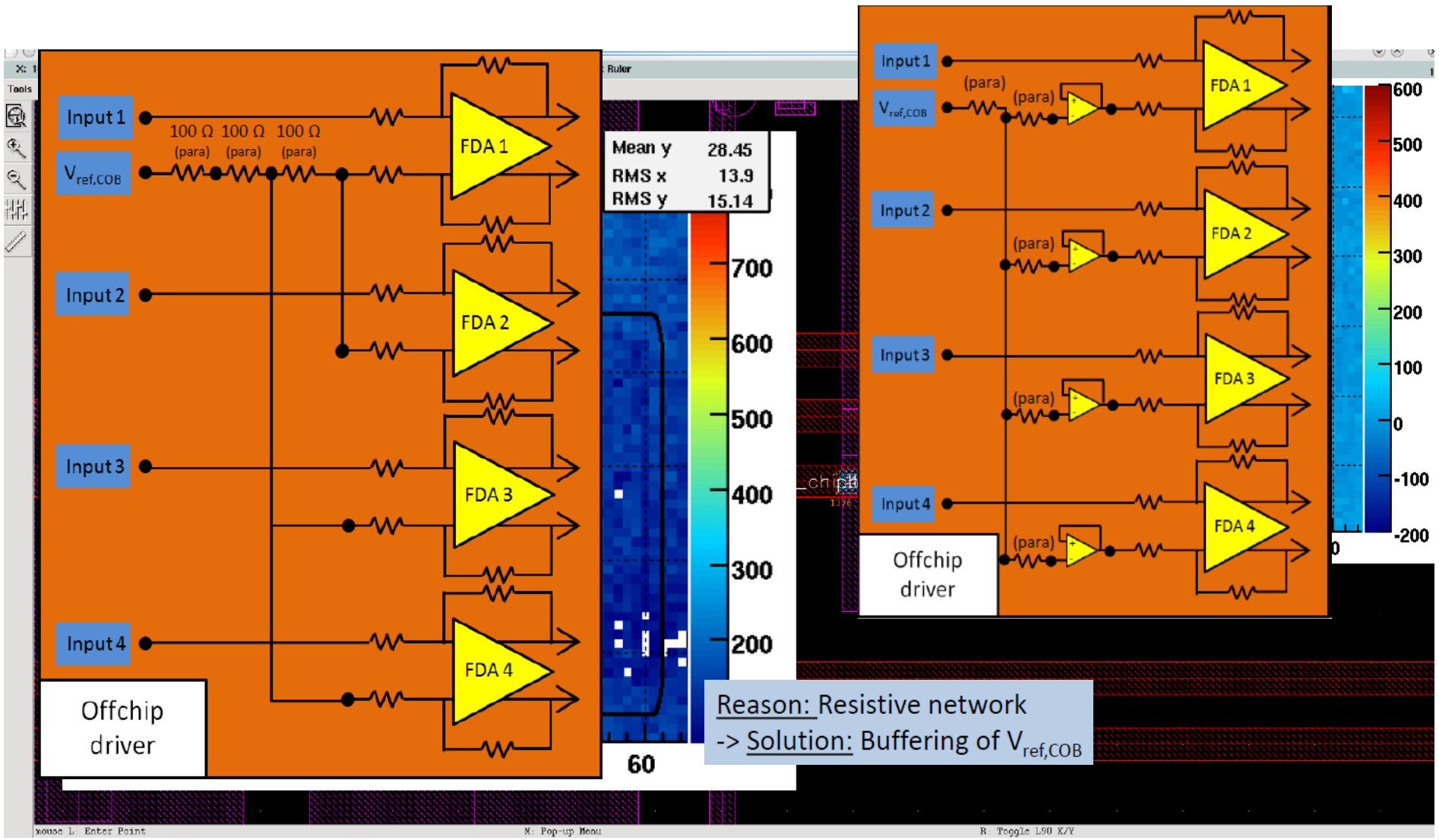
AGIPD 1.1



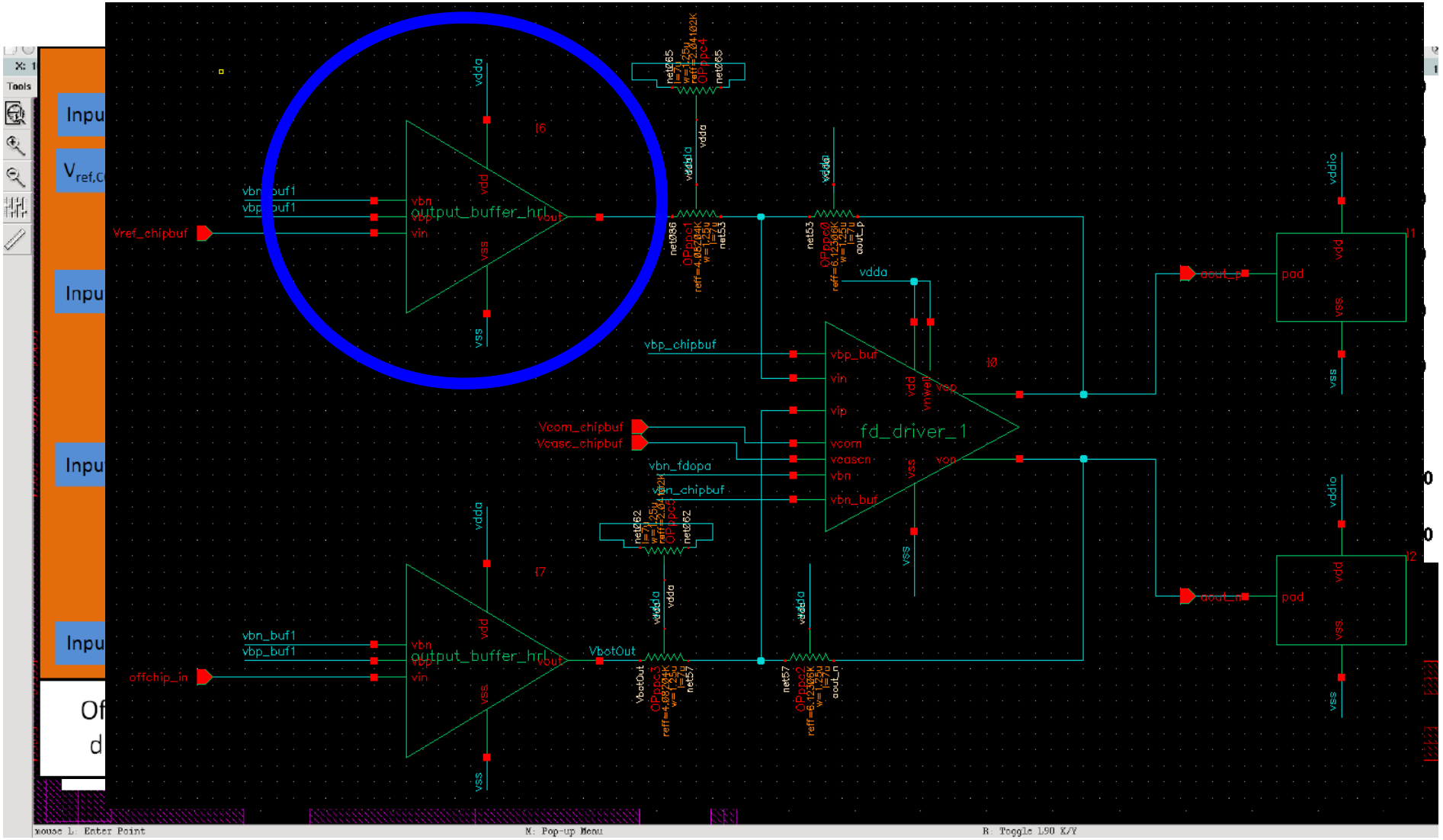
Ghosting



Ghosting


Input 1
Input 2
Input 3
Input 4
$V_{ref,COB}$
100 Ω (para)
100 Ω (para)
100 Ω (para)
FDA 1
FDA 2
FDA 3
FDA 4
Offchip driver
Mean y 28.45
RMS x 13.9
RMS y 15.14
700
600
500
400
300
200
60
(para)
600
500
400
300
200
100
0
-100
-200
Reason: Resistive network
-> Solution: Buffering of $V_{ref,COB}$

Ghosting


output_buffer_hrl
fd_driver_1
Vref_chipbuf
offchip_in
Vcom_chipbuf
Vcasc_chipbuf
vbp_chipbuf
vbn_fdopa
vbn_chipbuf
vbn_buf1
vbp_buf1
VbotOut
vdda
vddio
vss
pad
aout_p
aout_n

Power mesh improvements

first port	second port	
1 {Layout Port vdd_preamp}	{Layout Port vddpa_cb}	0.264820
2 {Layout Port vdd_preamp}	{Layout Port vddpa_cc}	0.254816
3 {Layout Port vdd_preamp}	{Layout Port vddpa_ct}	0.284383
4 {Layout Port vdd_preamp}	{Layout Port vddpa_lb}	0.330787
5 {Layout Port vdd_preamp}	{Layout Port vddpa_lc}	0.298685
6 {Layout Port vdd_preamp}	{Layout Port vddpa_lt}	0.344454
7 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_cb}	0.875277
8 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_cc}	0.881805
9 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_ct}	1.00542
10 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_lb}	0.954286
11 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_lc}	0.947453
12 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_lt}	1.02888
13 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_rb}	0.847875
14 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_rc}	0.884601
15 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_rt}	1.05051
16 {Layout Port vdd_preamp}	{Layout Port vddpa_rb}	0.242085
17 {Layout Port vdd_preamp}	{Layout Port vddpa_rc}	0.268469
18 {Layout Port vdd_preamp}	{Layout Port vddpa_rt}	0.328556

~1 Ohm

AGIPD 1.0

1 {Layout Port vdd_analog_PAD}	{Layout Port vdd_muxb}	4.50291
2 {Layout Port vdd_analog_PAD}	{Layout Port vdd_muxc}	3.16835
3 {Layout Port vdd_analog_PAD}	{Layout Port vdd_muxt}	6.17491
4 {Layout Port vdd_analog_PAD}	{Layout Port vdda_cb}	0.169596
5 {Layout Port vdd_analog_PAD}	{Layout Port vdda_cc}	0.172521
6 {Layout Port vdd_analog_PAD}	{Layout Port vdda_ct}	0.217845
7 {Layout Port vdd_analog_PAD}	{Layout Port vdda_lb}	0.219568
8 {Layout Port vdd_analog_PAD}	{Layout Port vdda_lc}	0.199112
9 {Layout Port vdd_analog_PAD}	{Layout Port vdda_lt}	0.253874
10 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_cb}	0.734857
11 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_cc}	0.731455
12 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_ct}	0.943812
13 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_lb}	0.847009
14 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_lc}	0.779617
15 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_lt}	1.01929
16 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_rb}	0.720869
17 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_rc}	0.745681
18 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_rt}	0.977527
19 {Layout Port vdd_analog_PAD}	{Layout Port vdda_rb}	0.127501
20 {Layout Port vdd_analog_PAD}	{Layout Port vdda_rc}	0.202653
21 {Layout Port vdd_analog_PAD}	{Layout Port vdda_rt}	0.248594

~0.8 Ohm

first port	second port	value
1 {Layout Port vdd_preamp}	{Layout Port vddpa_cb}	0.251101
2 {Layout Port vdd_preamp}	{Layout Port vddpa_cc}	0.241566
3 {Layout Port vdd_preamp}	{Layout Port vddpa_ct}	0.263659
4 {Layout Port vdd_preamp}	{Layout Port vddpa_lb}	0.293476
5 {Layout Port vdd_preamp}	{Layout Port vddpa_lc}	0.267731
6 {Layout Port vdd_preamp}	{Layout Port vddpa_lt}	0.301566
7 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_cb}	0.608261
8 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_cc}	0.598815
9 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_ct}	0.644467
10 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_lb}	0.666144
11 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_lc}	0.647854
12 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_lt}	0.741537
13 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_rb}	0.592928
14 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_rc}	0.615367
15 {Layout Port vdd_preamp}	{Layout Port vddpa_mq_rt}	0.695682
16 {Layout Port vdd_preamp}	{Layout Port vddpa_rb}	0.275503
17 {Layout Port vdd_preamp}	{Layout Port vddpa_rc}	0.292451
18 {Layout Port vdd_preamp}	{Layout Port vddpa_rt}	0.340166

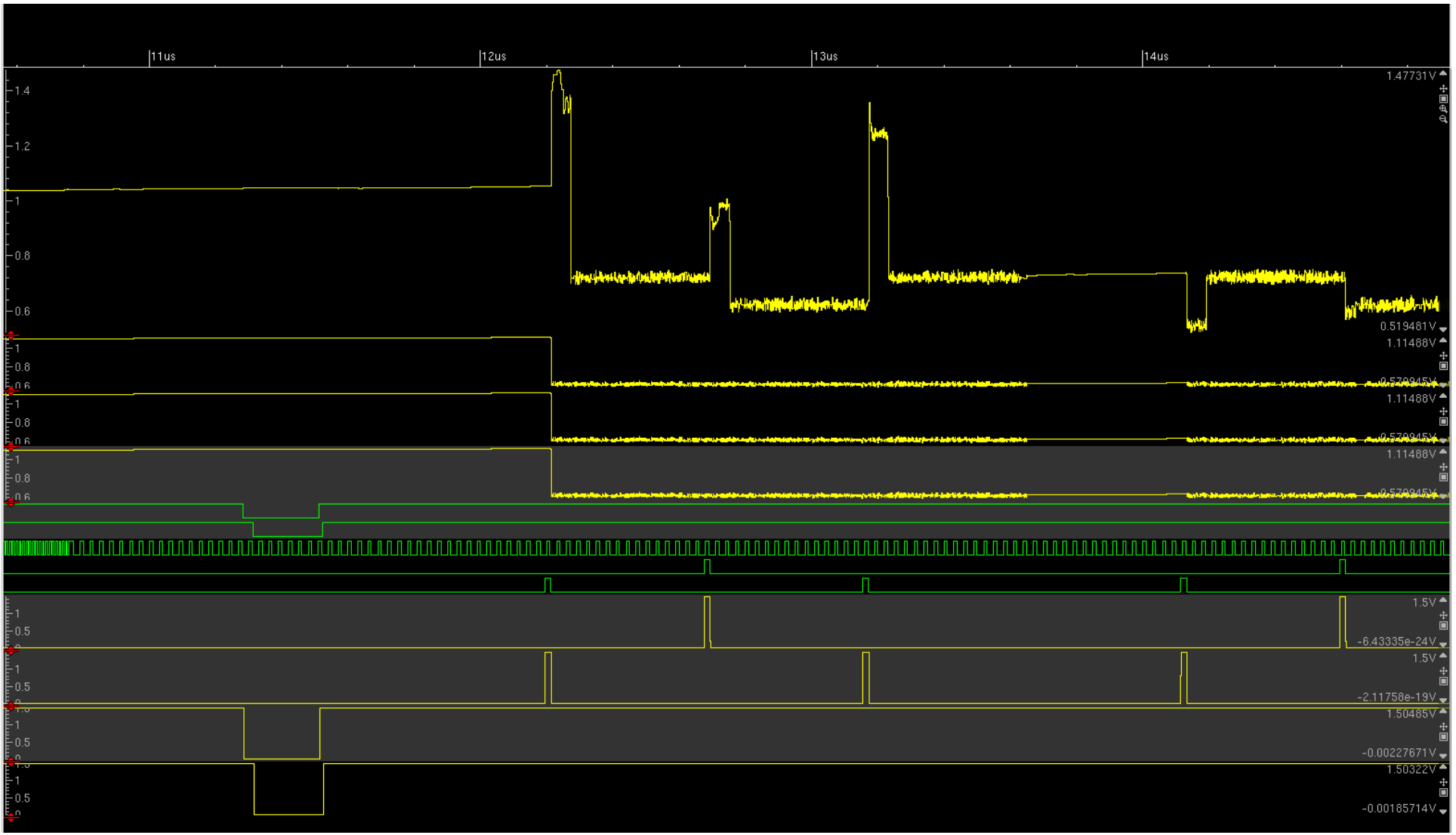
~0.65 Ohm

AGIPD 1.1

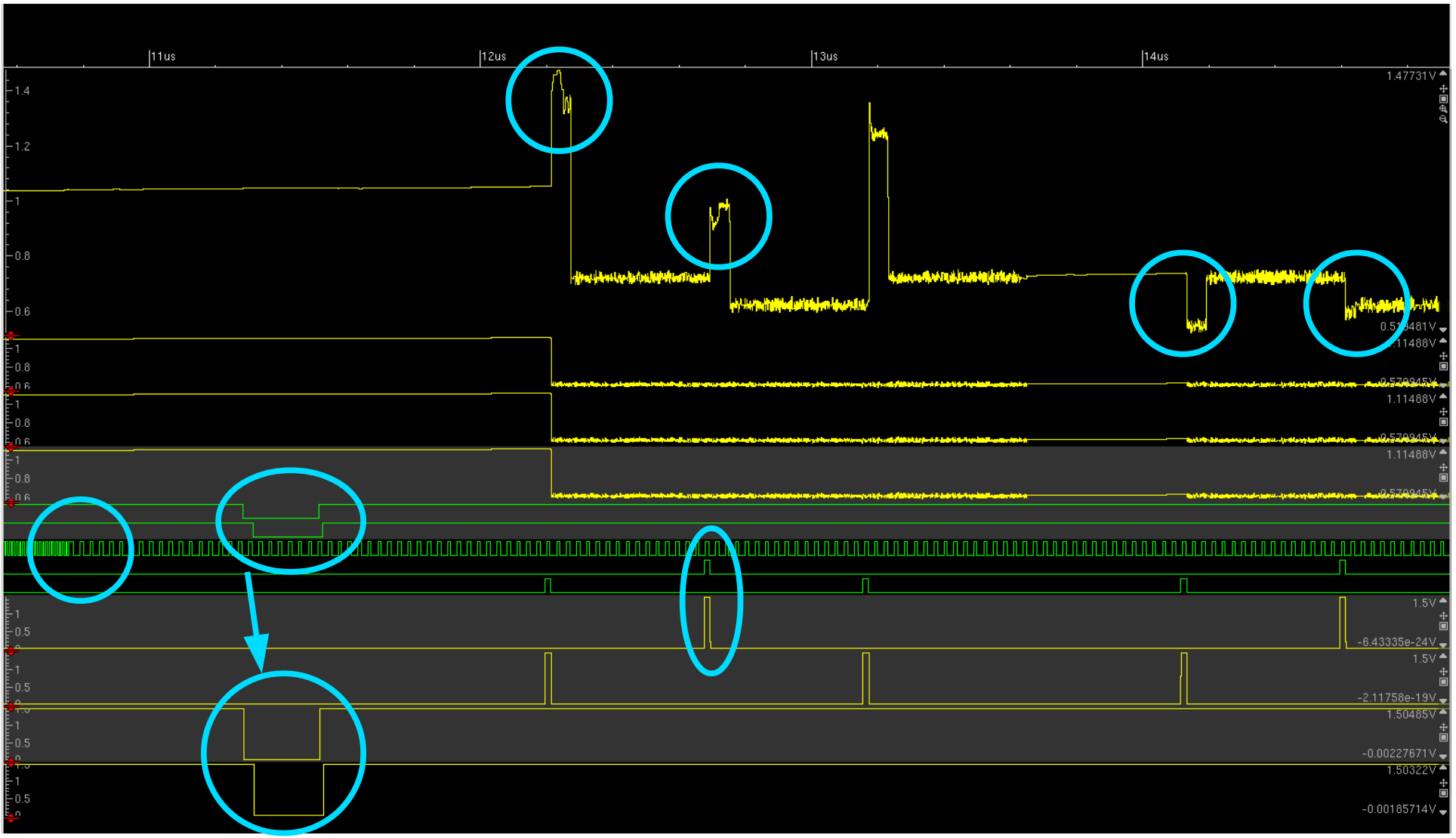
1 {Layout Port vdd_analog_PAD}	{Layout Port vdd_muxb}	1.19961
2 {Layout Port vdd_analog_PAD}	{Layout Port vdd_muxc}	0.533168
3 {Layout Port vdd_analog_PAD}	{Layout Port vdd_muxt}	0.757212
4 {Layout Port vdd_analog_PAD}	{Layout Port vdda_cb}	0.154663
5 {Layout Port vdd_analog_PAD}	{Layout Port vdda_cc}	0.154324
6 {Layout Port vdd_analog_PAD}	{Layout Port vdda_ct}	0.191142
7 {Layout Port vdd_analog_PAD}	{Layout Port vdda_lb}	0.198285
8 {Layout Port vdd_analog_PAD}	{Layout Port vdda_lc}	0.178307
9 {Layout Port vdd_analog_PAD}	{Layout Port vdda_lt}	0.226049
10 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_cb}	0.482952
11 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_cc}	0.473007
12 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_ct}	0.516483
13 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_lb}	0.532073
14 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_lc}	0.501242
15 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_lt}	0.567258
16 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_rb}	0.441116
17 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_rc}	0.478333
18 {Layout Port vdd_analog_PAD}	{Layout Port vdda_mq_rt}	0.552227
19 {Layout Port vdd_analog_PAD}	{Layout Port vdda_rb}	0.108325
20 {Layout Port vdd_analog_PAD}	{Layout Port vdda_rc}	0.150609
21 {Layout Port vdd_analog_PAD}	{Layout Port vdda_rt}	0.210877

~0.45 Ohm

AMS functional simulation



AMS functional simulation



To-do list of changes

- DGN caps inside the outmux
- GND contacts from outmux to the pixel
- Discuss IBM test structures placement → supertop layout placement
- Place blocking DGN caps in the bottom and on the right side of the ASIC
- Put monitoring bump bonds for VDDA VDDPA GND on the top (right) of the ASIC
- Add cutting mark
- Discuss bump bonding mark

AGIPD 1.1 Submission

Expected improvements and patches for the AGIPD 1.1 version:

- Better and stable level separation of the gain bits by implementing different powering schemes and revised operation timings
- Easier and faster calibration of the system due to:
  - Removing the ghosting crosstalk by adding a buffer in the off-chip driver circuitry
  - Removing the cross talk between the address lines and the analog nodes
  - Improved internal calibration structures
- Faster readout up to 33 MHz with new output lines and power distribution layout
- New stable Power-On-Reset circuitry