Interface Electronics

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DESY-FEB
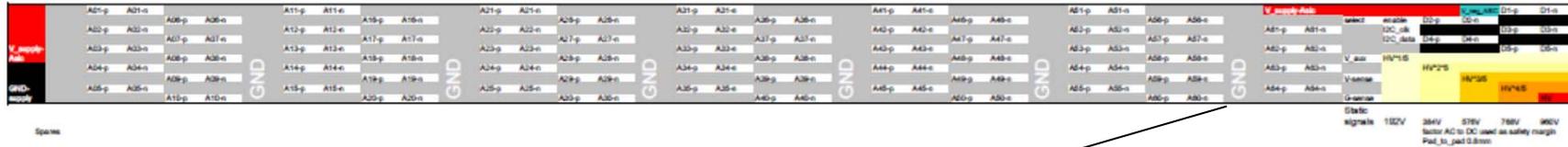
AGIPD Meeting at PSI, March 9th 2011

HELMHOLTZ | ASSOCIATION

DESY

Outline

➢ Update to backplane

➢ Signal transfer ASIC to analogue chain
  ➢ Simulations
  ➢ Impacts to circuit diagram
  ➢ Drawbacks

➢ Personal view

Update to backplane

Negative voltage with low current for the ASIC

GND	V_supply-Asic					V_neg_ASIC	D1-p	D1-n
		select	enable	D2-p	D2-n			
	A61-p	A61-n		I2C_clk			D3-p	D3-n
				I2C_data	D4-p	D4-n		
	A62-p	A62-n					D5-p	D5-n
			V_aux	HV*1/5				
	A63-p	A63-n			HV*2*5			
			V-sense			HV*3/5		
	A64-p	A64-n					HV*4/5	
			G-sense					HV
	Static signals	192V	384V	576V	768V	960V		

factor AC to DC used as safety margin
Pad_to_pad 0.8mm

Deliverable?

SAMTEC:

SEAF- Right angle still not available. They shift the date from March to April 2011:

Not available would need a more complex design inside the vacuum.

A ring more for the HV: while defining the footprint. Close to MIL-norm

As consequence a bit of resorting at the left end

➢ Open issue: - Kind of signal source (ASIC) : I, U, Z
                            - Kind of termination at interface electronics

Distance between ASIC and Receiver:

Open issue, but
    10cm wide module
    Voltage-reg. in the vacuum (10cm)
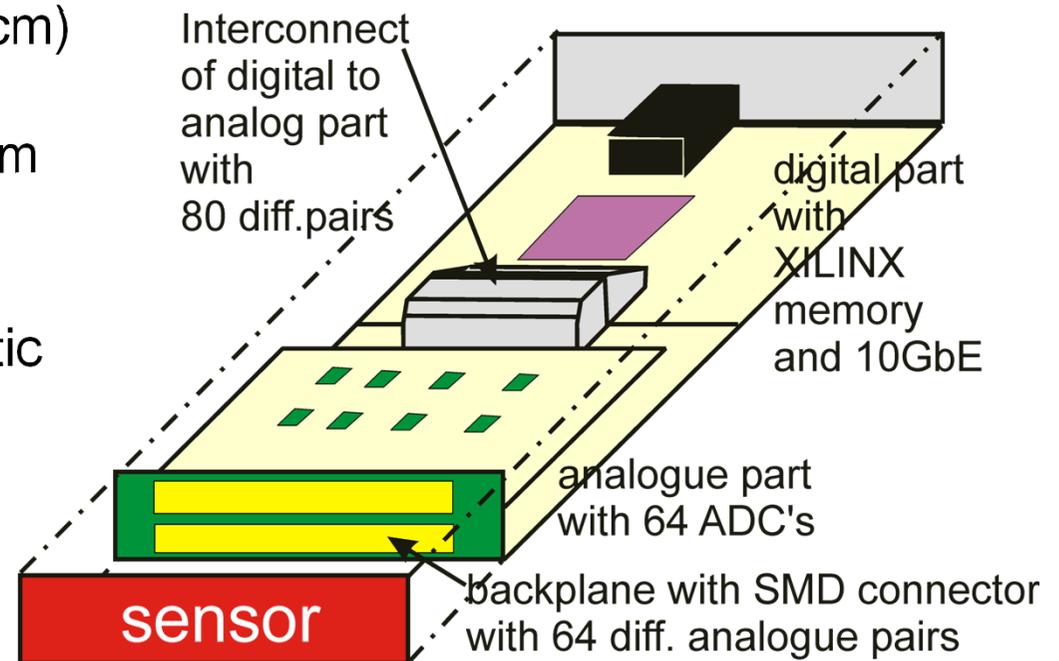   three connectors (7 cm)
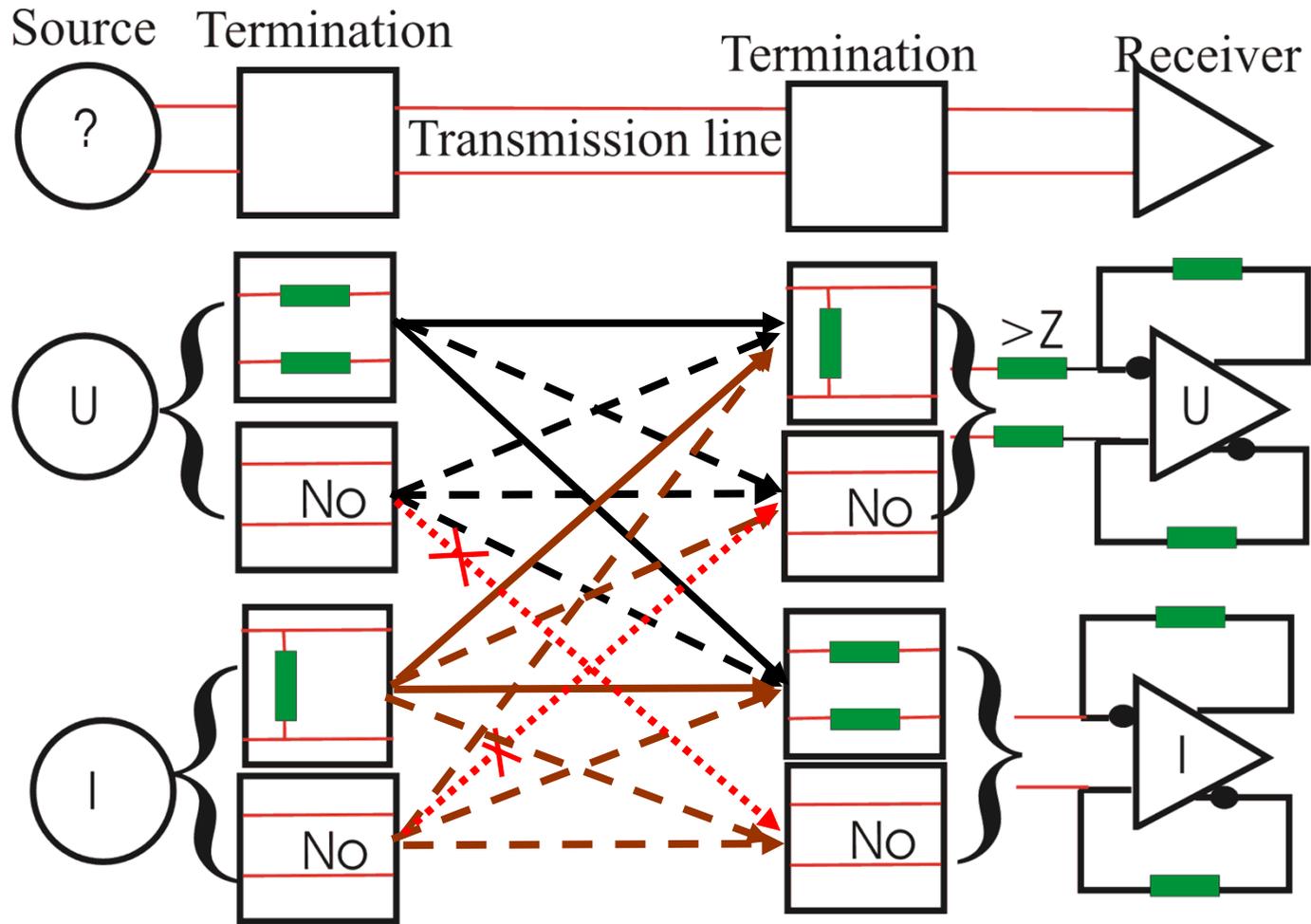   trace in Interface electronics 2cm
    trace on HDI

30 cm might be a bit too pessimistic
            but not too far from reality

= 2ns per signal pass

Interconnect
of digital to
analog part
with
80 diff.pairs

digital part
with
XILINX
memory
and 10GbE

analogue part
with 64 ADC's

backplane with SMD connector
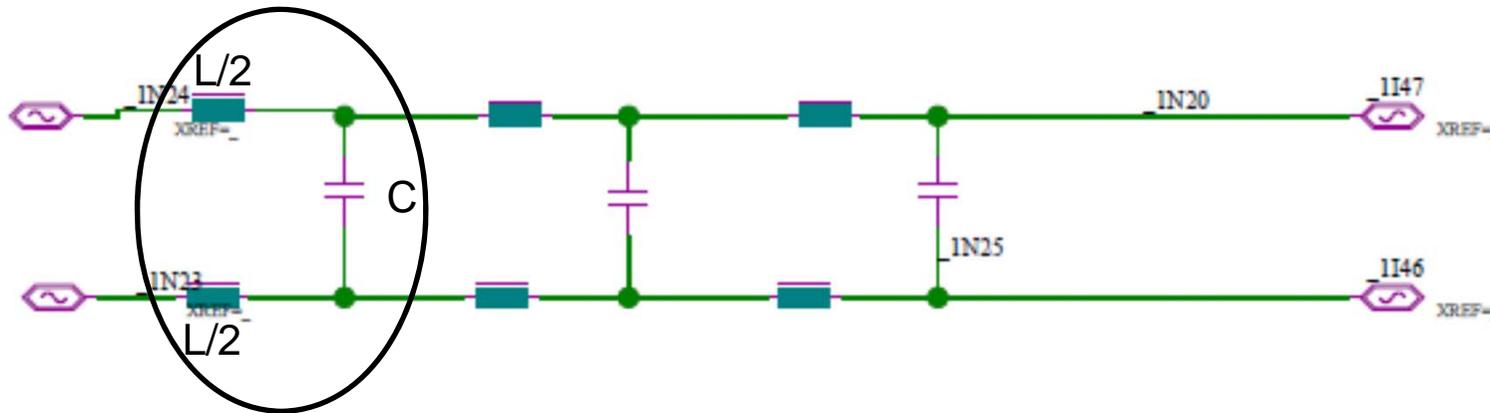with 64 diff. analogue pairs

sensor

U-source without I-limiter needs U-receiver
I-source without U-limiter needs I-receiver
Terminated (also not 100%) : allows both:
    For 100%: I-source and U-source models or idential
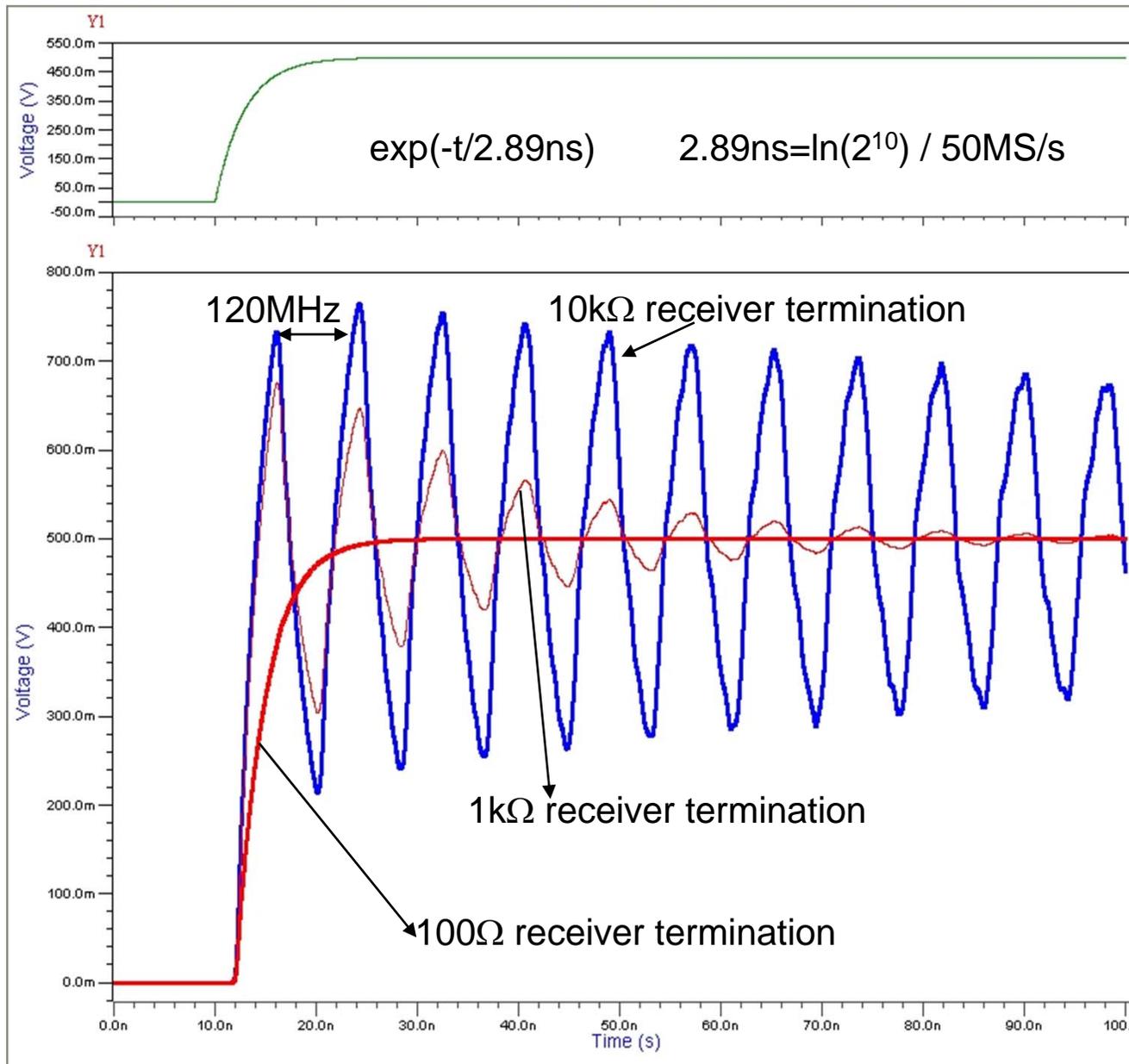   Implementation differs

Driver options allow
 all combinations

18 elements for 2ns: L*C = 2ns/ 18

$Z^2 = (100\Omega)^2 = L/C$

$$\exp(-t/2.89\text{ns}) \qquad 2.89\text{ns}=\ln(2^{10}) / 50\text{MS/s}$$

120MHz

10kΩ receiver termination
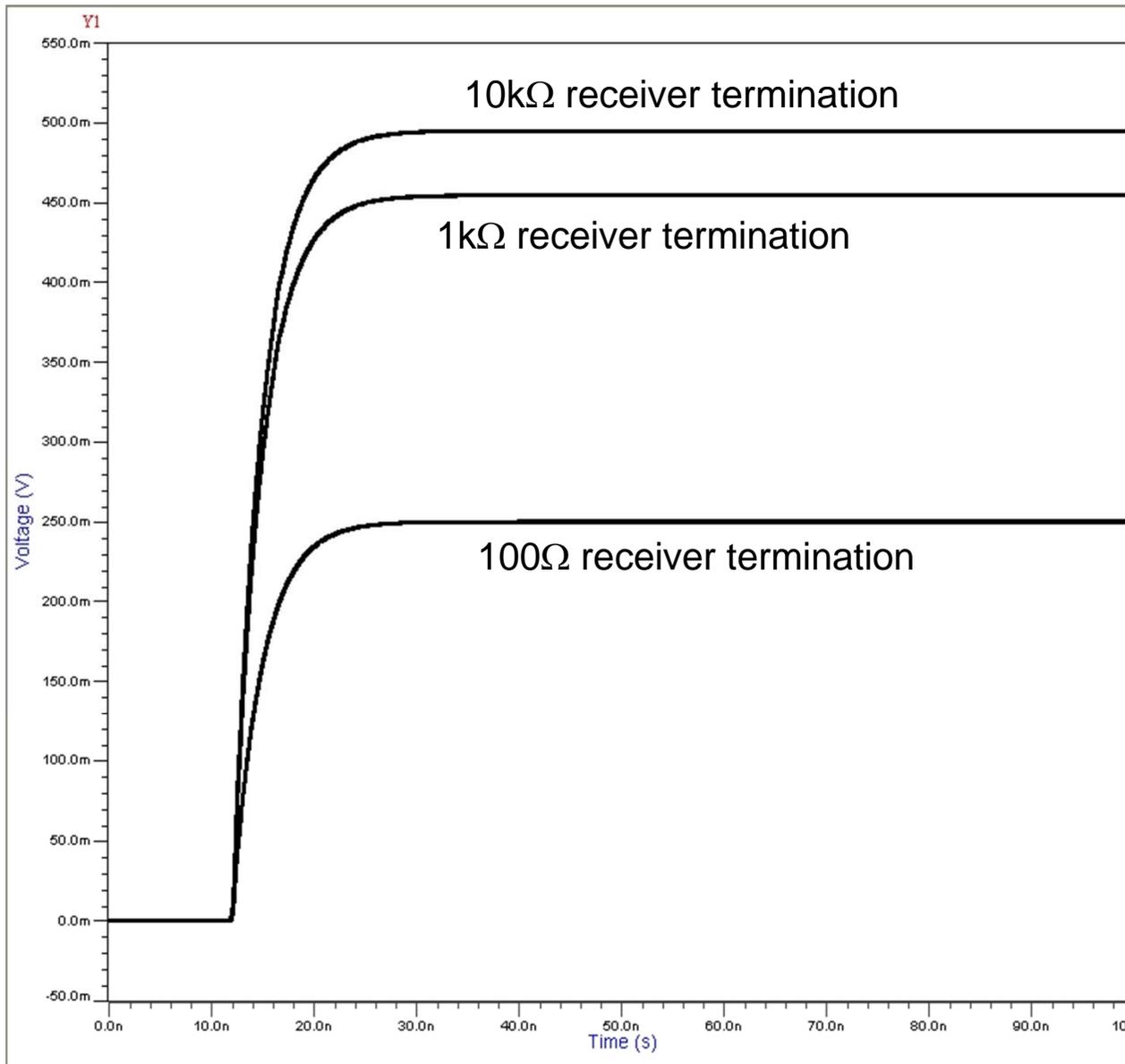
1kΩ receiver termination

100Ω receiver termination

50MS/s needs a bandwidth of 50MHz:

No chance to suppress at 120MHz.

50MS/s with no source termination needs termination at receiver and driver strength at ASIC
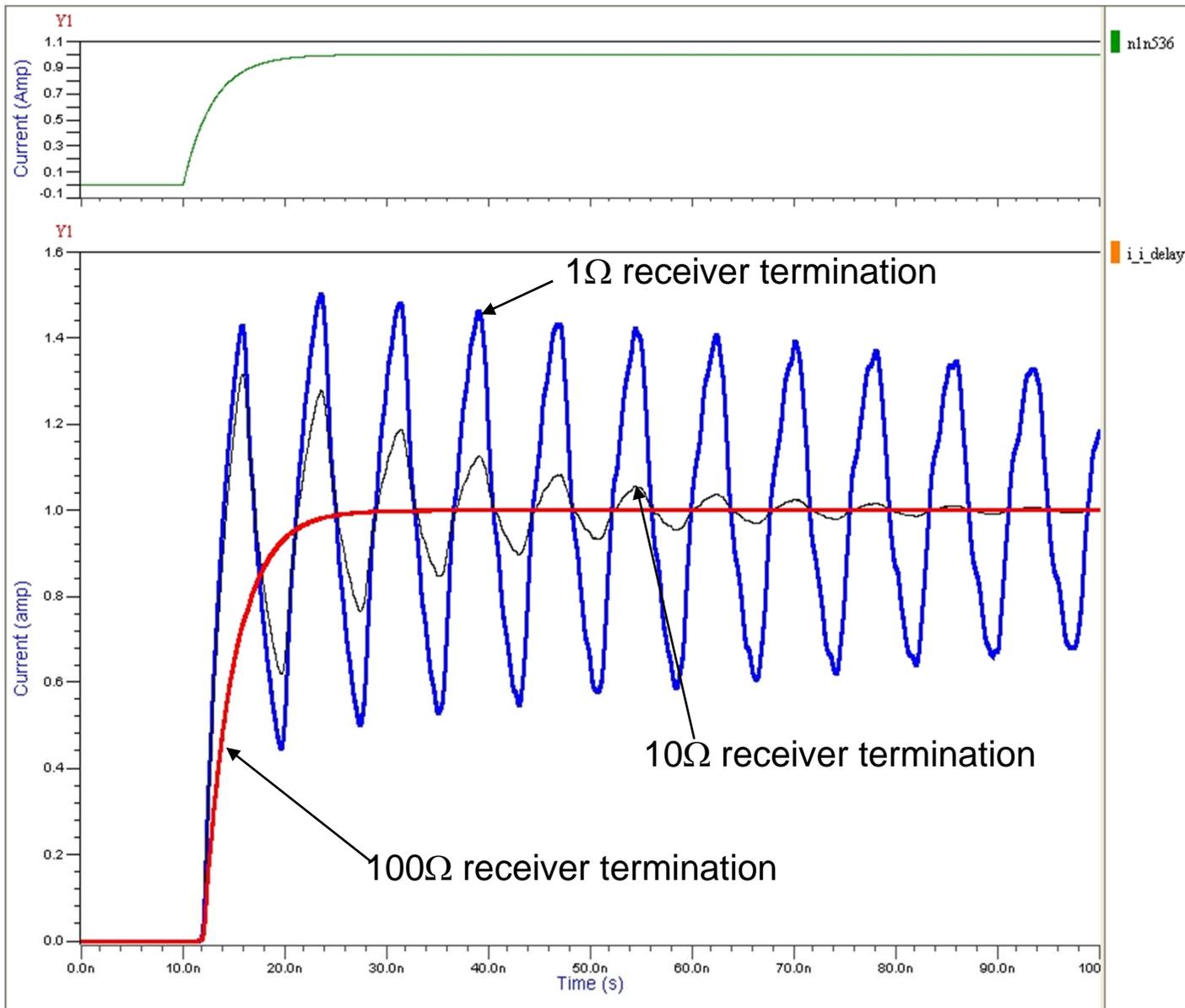
Termination at the source allows freedom at the receiver.

Normally:

Source termination for a wide frequency range is more difficult than receiver termination
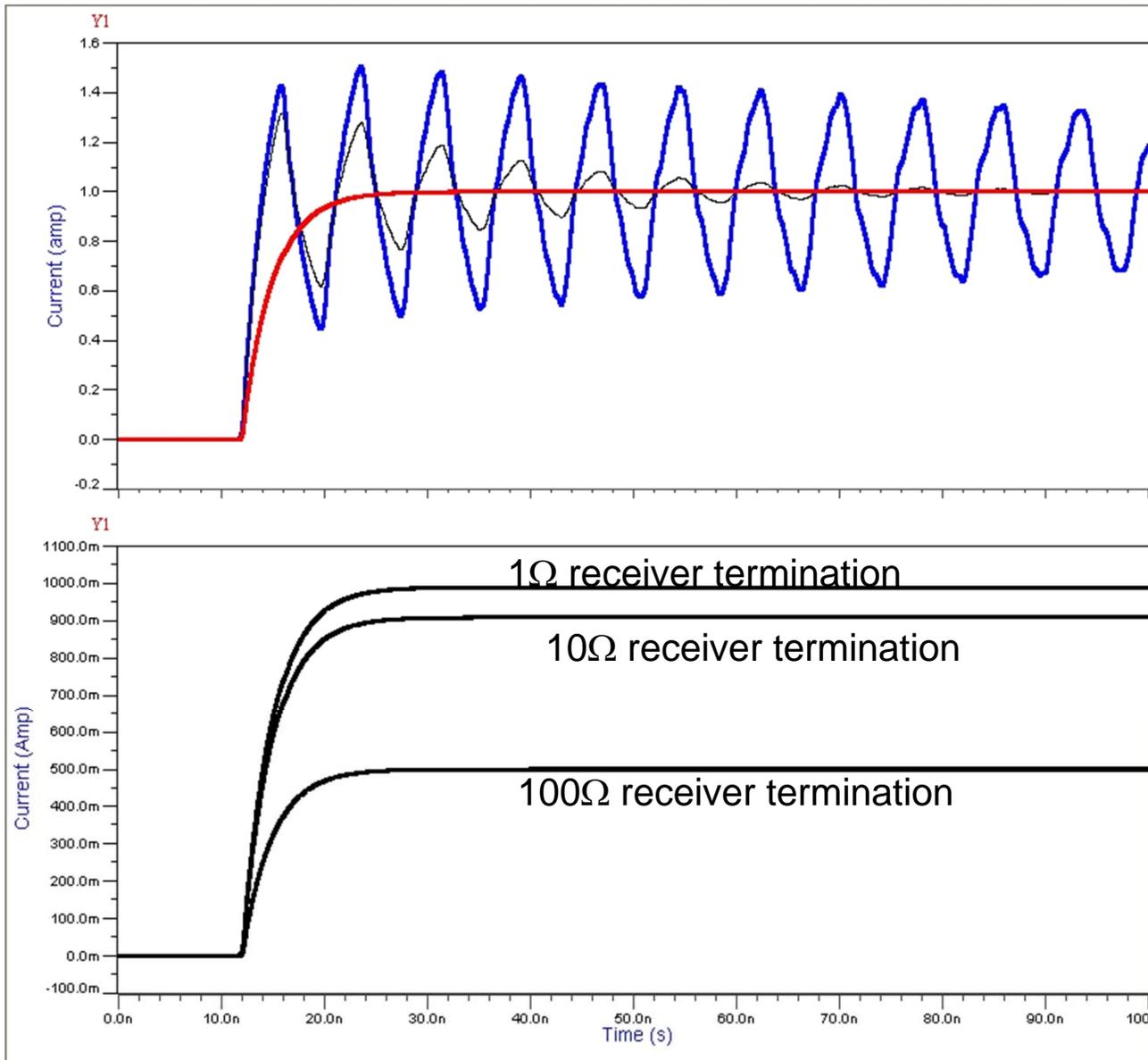
Driver strength needed

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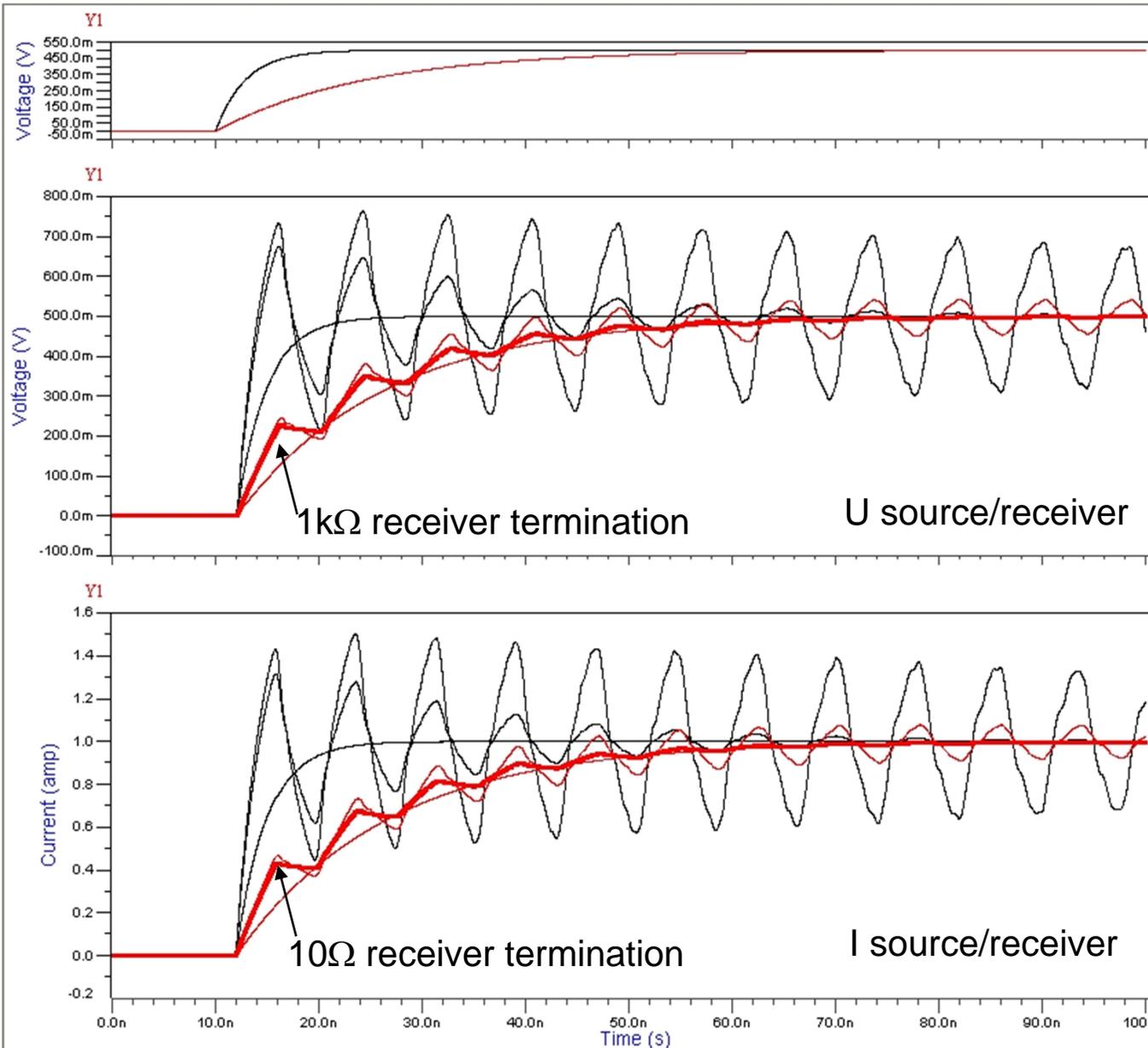
Termination at the source allows freedom at the receiver.

Normally:

Source termination for a wide frequency range is more difficult than receiver termination

Driver strength and voltage range needed

1Ω receiver termination

10Ω receiver termination

100Ω receiver termination

Black:
Still slew rate 2.89ns

Red: 14.45ns for 10MS/s

Sampling rate will reduction help only, if also the slew rate

Filters are easier, since only 10MHz is needed. But cross talk and noise are a risk. "Peaks with rectifying effects.

1kΩ receiver termination

U source/receiver

10Ω receiver termination

I source/receiver

Drawback or best compromise?

- Good storage behaviour:

Can it be used to increase the number of storage cells?

400 Cells @ 50MS/s needs 16.4ms for digitizing.   10MS/s possible

But: Giving "just" up the option for 30Hz train rate.

Giving up 512 Cells @ 10Hz train rate, just not possible.
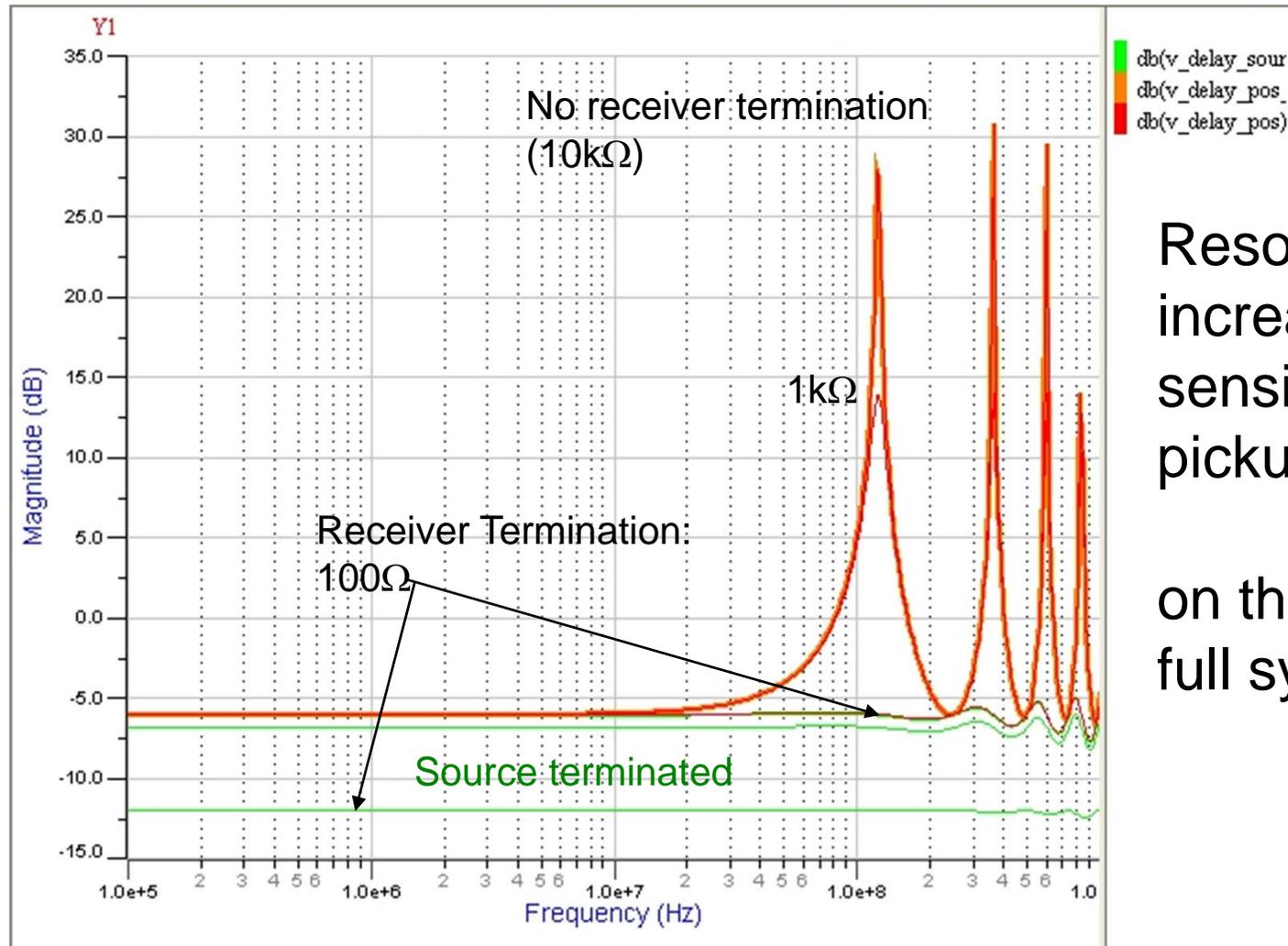
Would smaller storage cell needs less storage time?

To stay with 50MS/s the interface might need a design like:
Transferring a start address and doing than ASIC-internal increments for 16 (32) pulses while digitizing.

Digital part of interface would get a little bit easier, for lower sampling rate.
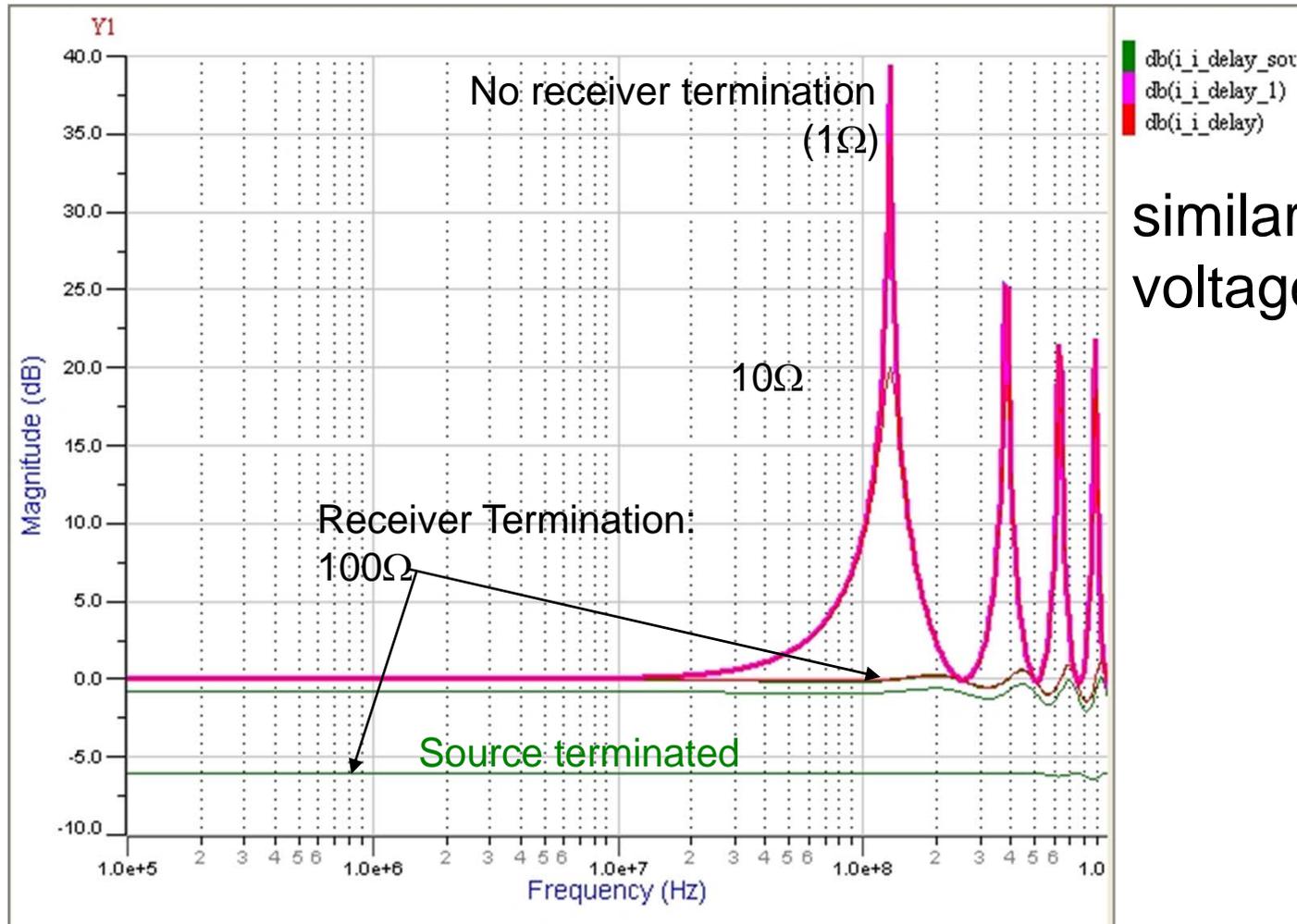
Resonances increases sensitivity to pickup noise

on the full system level

similar to
voltage driver/receiver
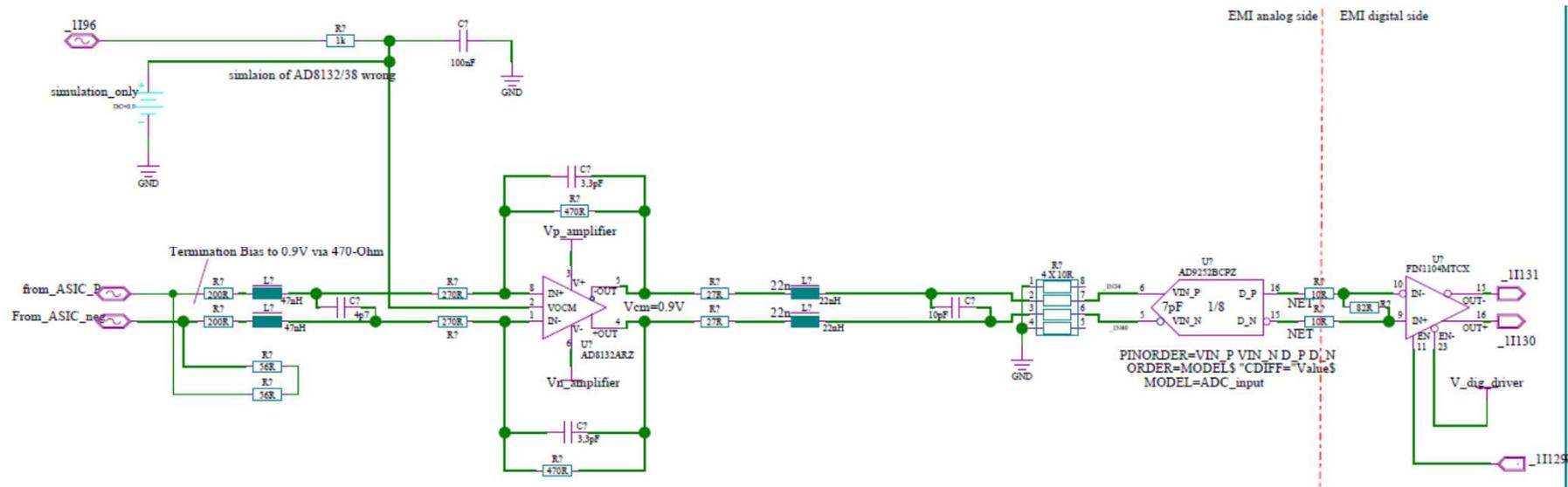
Power consumption requires ONE amplifier solution

Filtering : e.g. Noise picked up between ASIC and Interface electronics:
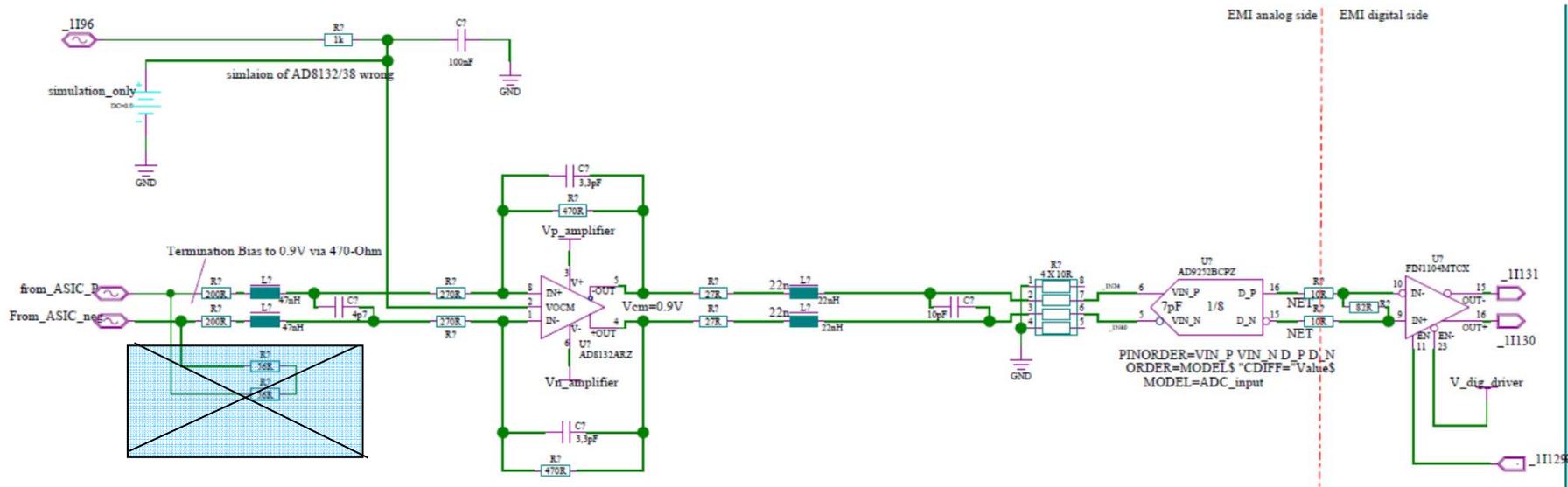- Before amplifier
- In feedback
- Between Amplifier and ADC

Need DC-coupling: During long digitizing sequence for a train
Best with pedestal samples delivered from ASIC.

Baseline from ASIC as pull to one side: -0.9V or just above -1.0V
ASIC handles, that the feedback delivers common mode: 0.9V, 470Ω

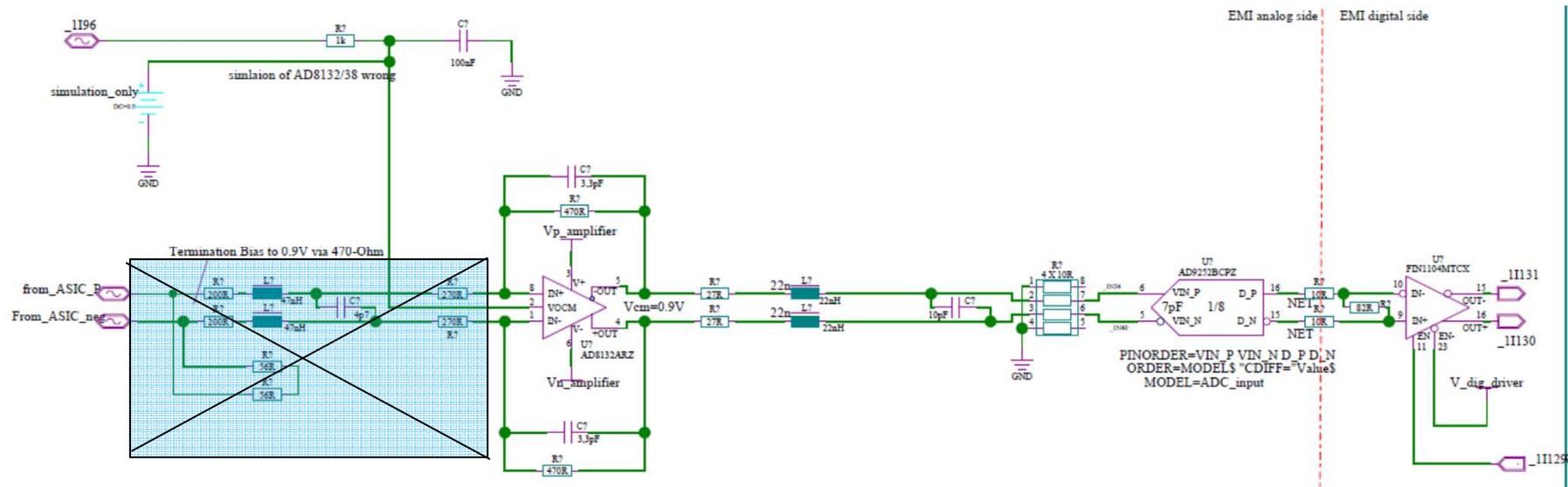Remaining impedance keeping the rest like it is: around 1kΩ

Whole part of the input filter disappears

Two small resistors to the input pins to limit long antennas on the input pins.

But all the reflection problem.

Trans-impedance: 1kΩ is possible.

Table 11. Recommended Resistor Values and Noise Performance for Specific Gains

Gain	R_G (Ω)	R_F (Ω)	Bandwidth −3 dB (MHz)	Output Noise AD8132 Only (nV/√Hz)	Output Noise AD8132 + R_G, R_F (nV/√Hz)
1	499	499	360	16	17
2	499	1.0 k	160	24.1	26.1
5	499	2.49 k	65	48.4	53.3
10	499	4.99 k	20	88.9	98.6

What about doing the termination, but
reducing the dynamics of the ASIC
  50MHz: Noise: 0.35mV
100MHz: Noise 0.53mV
    400mV needed to keep 9-10bit
  instead of the 2V foreseen.
>-200mV for baseline
<+200mV for full scale

More noise pickup between
  ASIC and receiver.

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ADA4938-1/ADA4938-2

Table 10 and Table 11 list several common gain settings, associated resistor values, input impedances, and output noise densities for both balanced and unbalanced input configurations. Also shown

Table 10. Differential Ground-Referenced Input, DC-Coupled; See

Nominal Gain (V/V)	R_F (Ω)	R_G (Ω)	$R_{IN, dm}$ (Ω)	Differential Output Noise Density (nV/√Hz)
1	200	200	400	6.5
2	402	200	400	10.4
3.16	402	127	254	13.4
5	402	80.6	161	18.2

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More noise pickup between
  ASIC and receiver.

Lower Noise would be available:

Cost: Higher power ~300-500W for 1Mpixel

  No similar for same footprint

  Different project searches ended
  up with same chip: Alternative in
  concept?

  Higher bandwidth: (?) more sensitive to
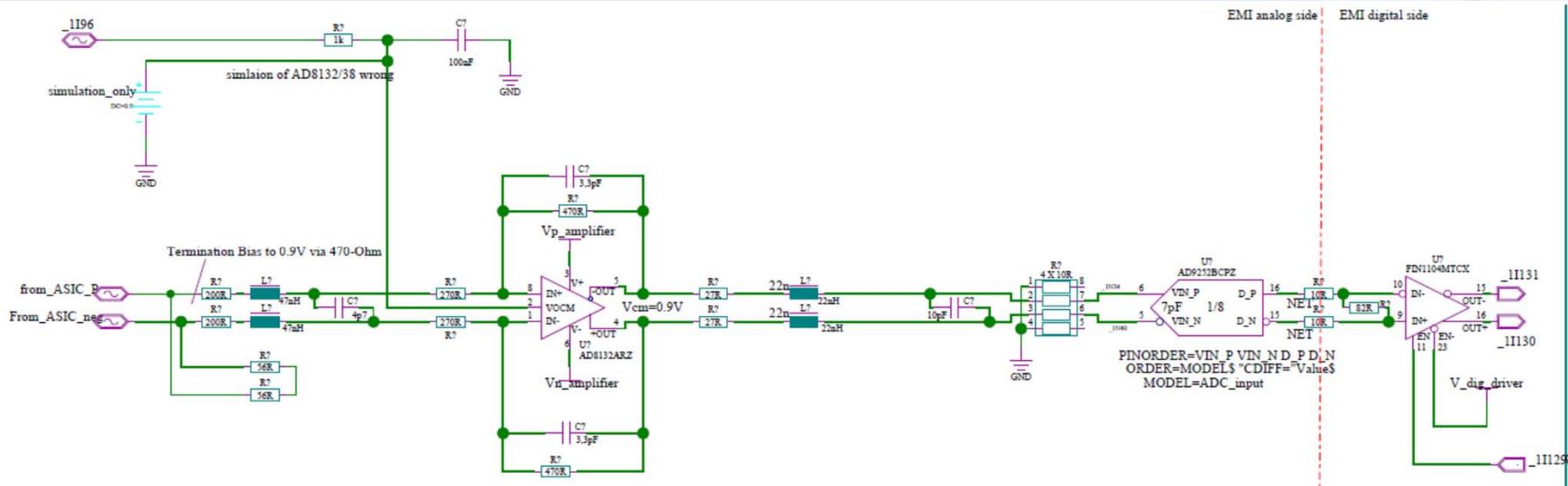 couple input lines with low impedance:
  (?) No ideal I-receiver

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LT1993-10:   1.8nV/sqrt(Hz)-eq-input
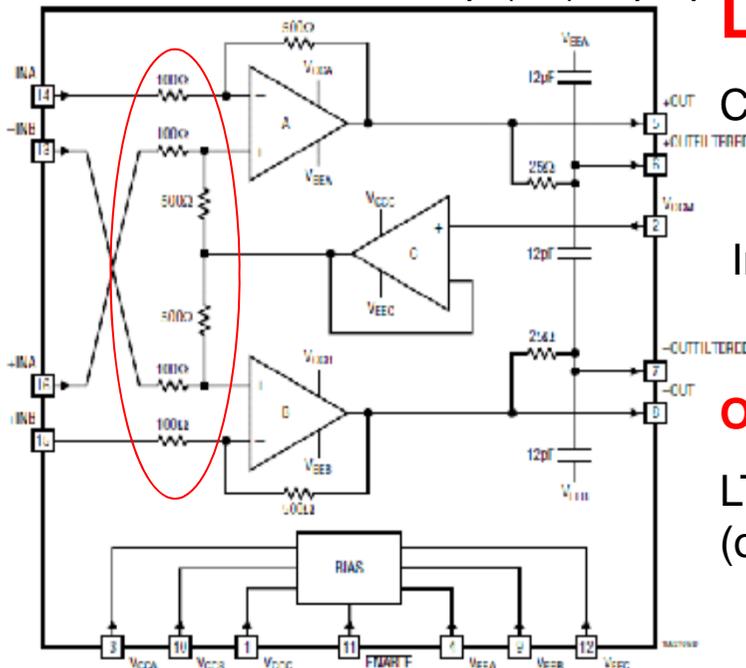
Lower Noise would be available:

Cost: Higher power 100A: ~500W-700W for 1Mpixel

+ Few centimeters.

Input impedance is external resistor

Internal virtual "infinity" to "200Ω"

ONLY chip noise: not power or pickup

LT6411 would offer an option for gain 3 gain
(only input 8nV/sqrt(Hz), gain 2) 60W/1Mega-Pixel
+ few cm's

!

Personal view

➢ I would not go the way of reflections and the according oscillations

➢ "Huge"power will change the mechnaical concept:
 Add as in first option: Water-cooling onto the module and not only
onto the frame.

➢ What are the drawbacks of an impedance controlled driver?
 what about a limited amplitude?

➢ I would like to keep the option of maximized the frame rate
 That is not a statement, that somebody is not fighting for it.
 Does it need short storage times?