



AGIPD Readout Amplifier Test Chip

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Outline

- Overview of the test chip
- Readout amplifier
- Simulation results
- Noise analysis
- Radiation hard bandgap reference
- Other test circuitry and development on the designkit
- Conclusion
- Future work

Overview of the chip

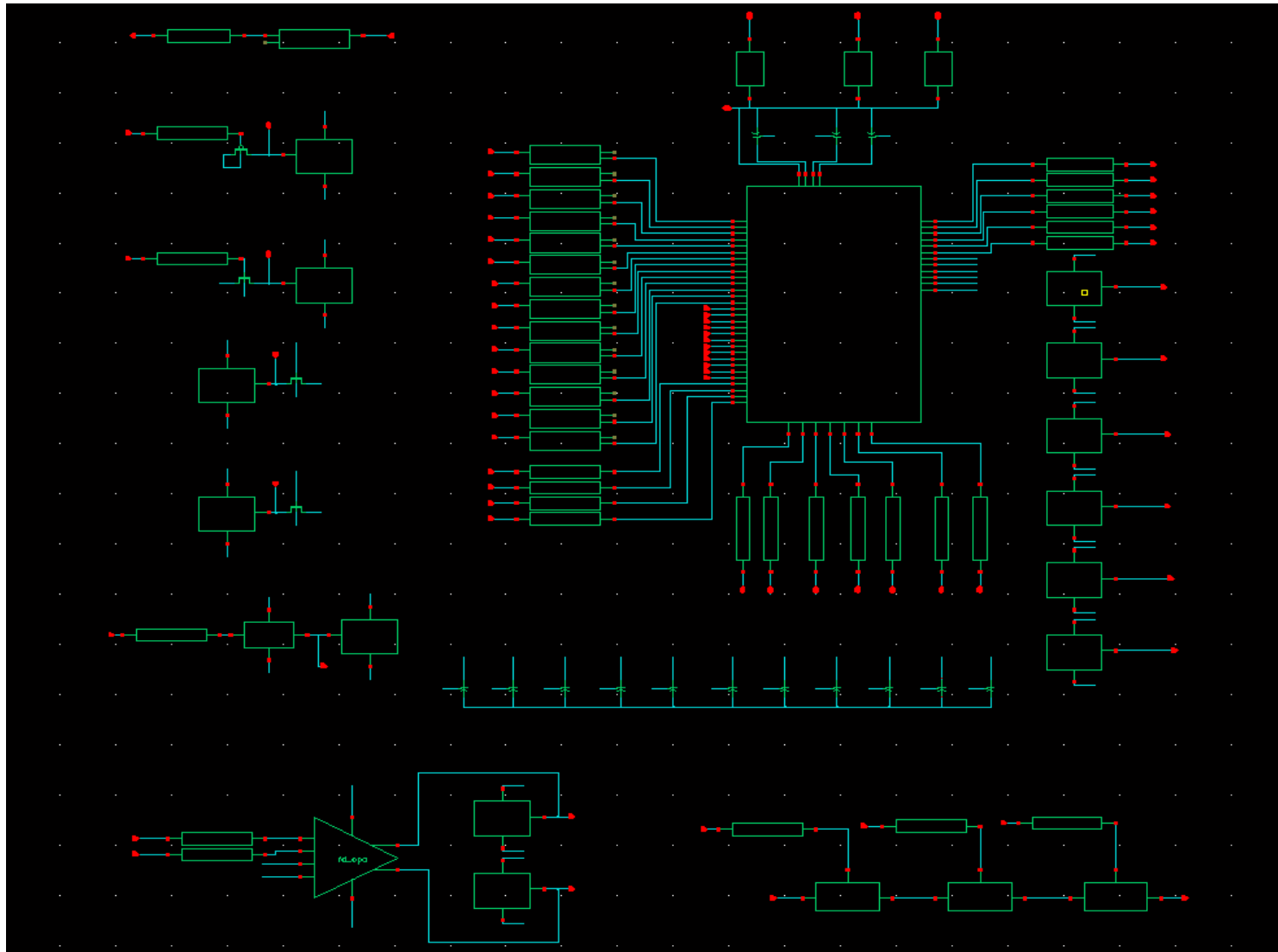
The 1st test chip was taped out in March. The main features of the chip are:

- Three different readout amplifiers:
 - No leakage current compensation
 - Static leakage compensation
 - Dynamic leakage compensation

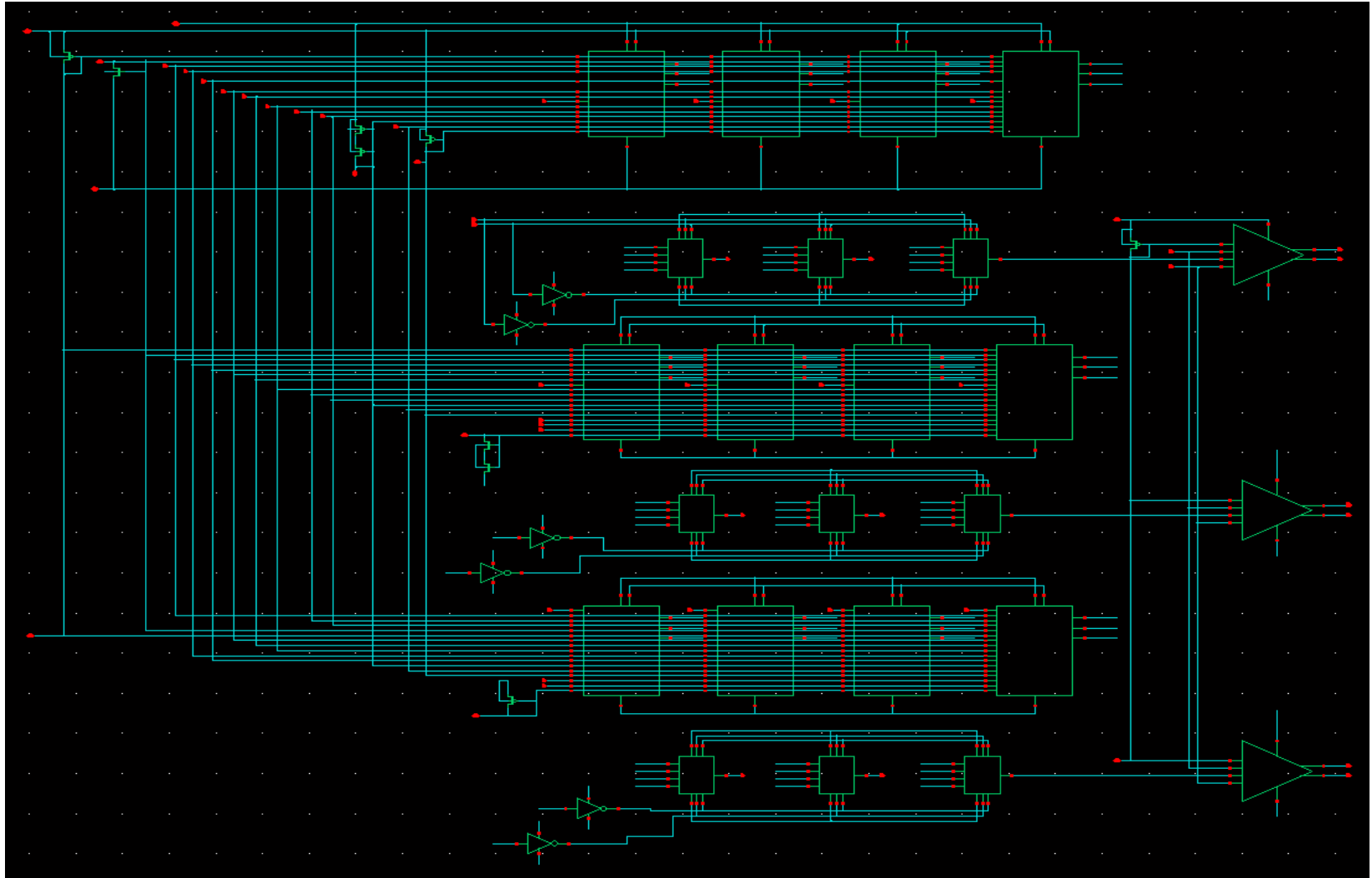
- Readout amplifier with:
 - Adaptive gain charge integrating amplifier (CIA).
 - Correlated double sampling (CDS) buffer
 - A storage capacitor
 - Single-ended to fully-differential converter

- Special test circuitry:
 - A radiation hard bandgap reference
 - A fully differential opamp
 - NMOS or PMOS transistors with enclosed gate and different sizes
 - Ring oscillator

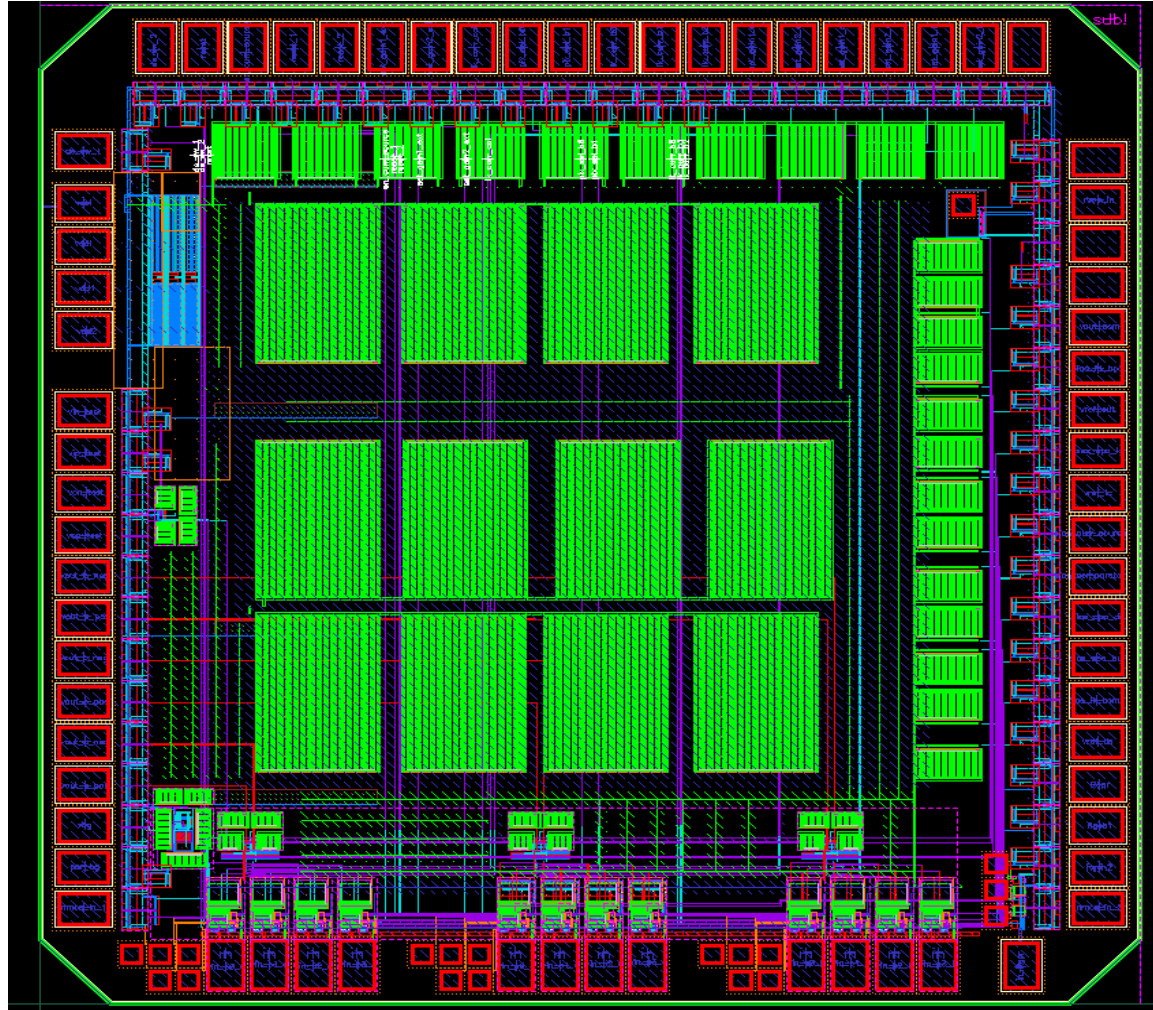
Schematic



Schematic

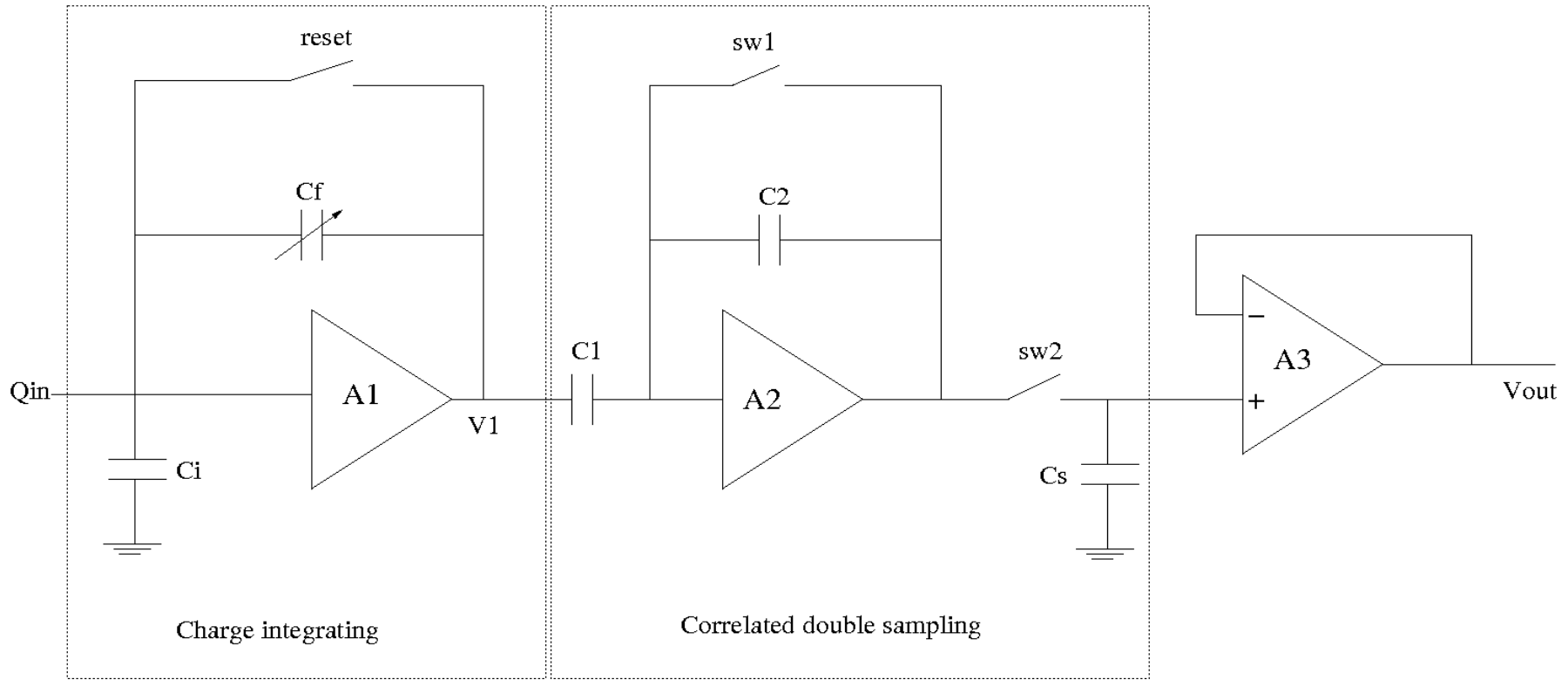


Chip layout



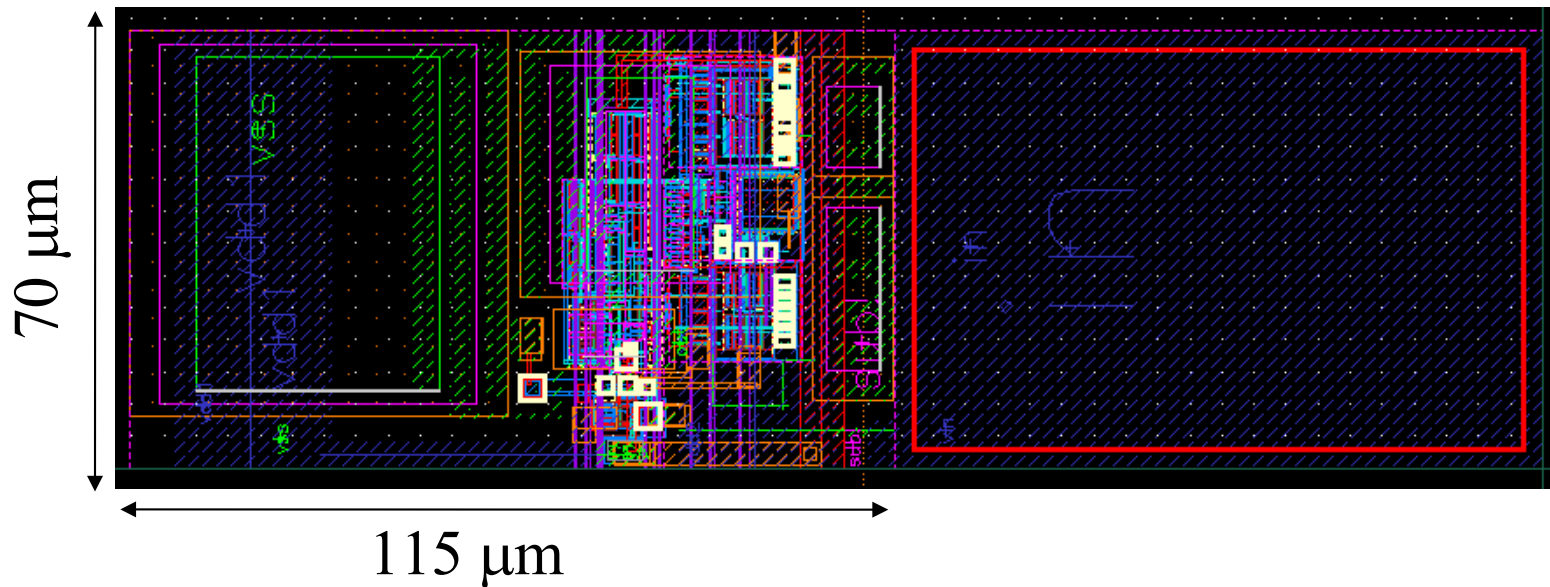
IBM 0.13 μm technology, size = $2 \times 2 \mu\text{m}^2$

Readout Amplifier



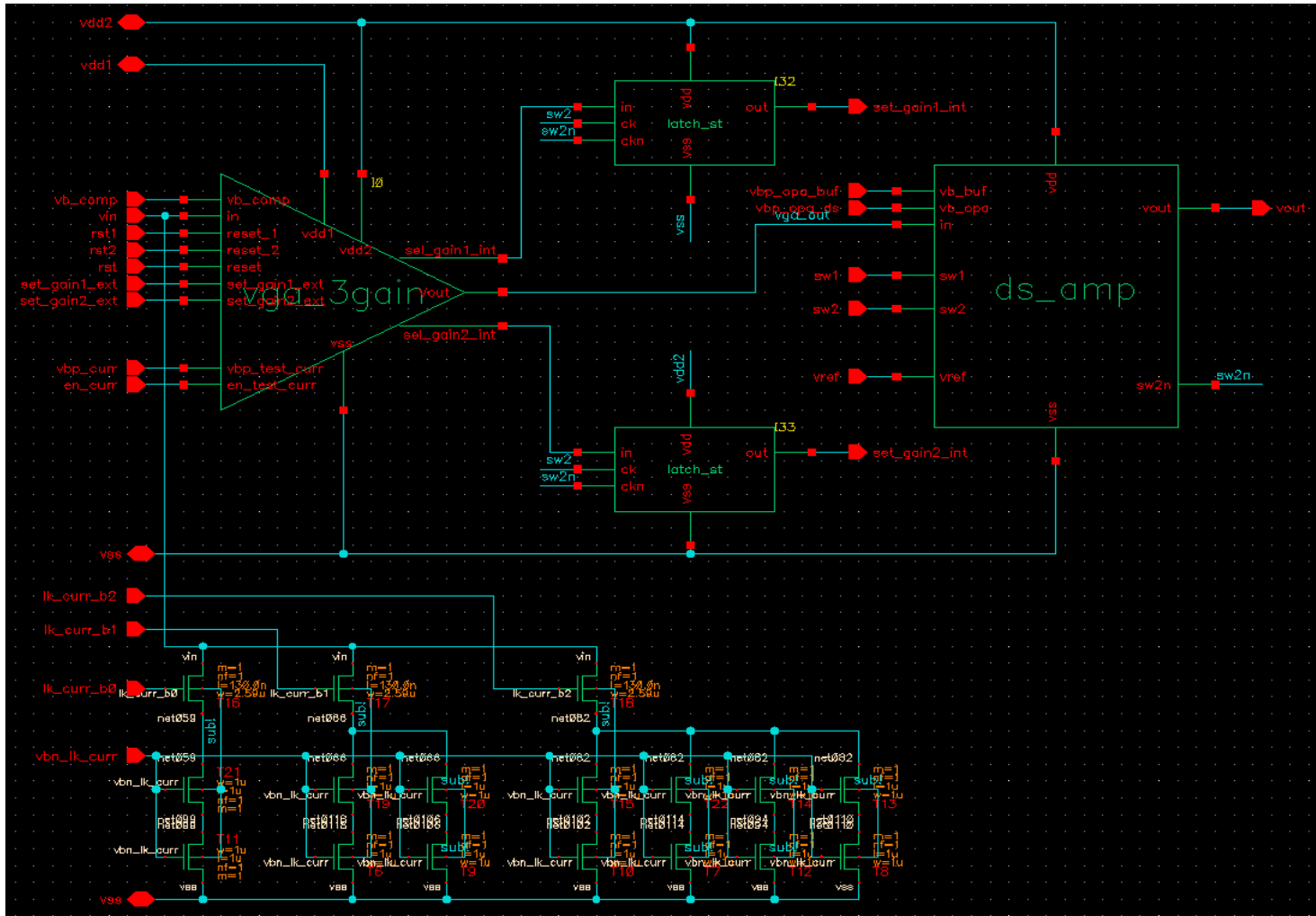
$$\frac{V_{out}}{Q_{input}} = \frac{A1_{dc}}{C_i + (1 + A1_{dc})C_f} \frac{C_1}{C_2}$$

Layout of the readout amplifier

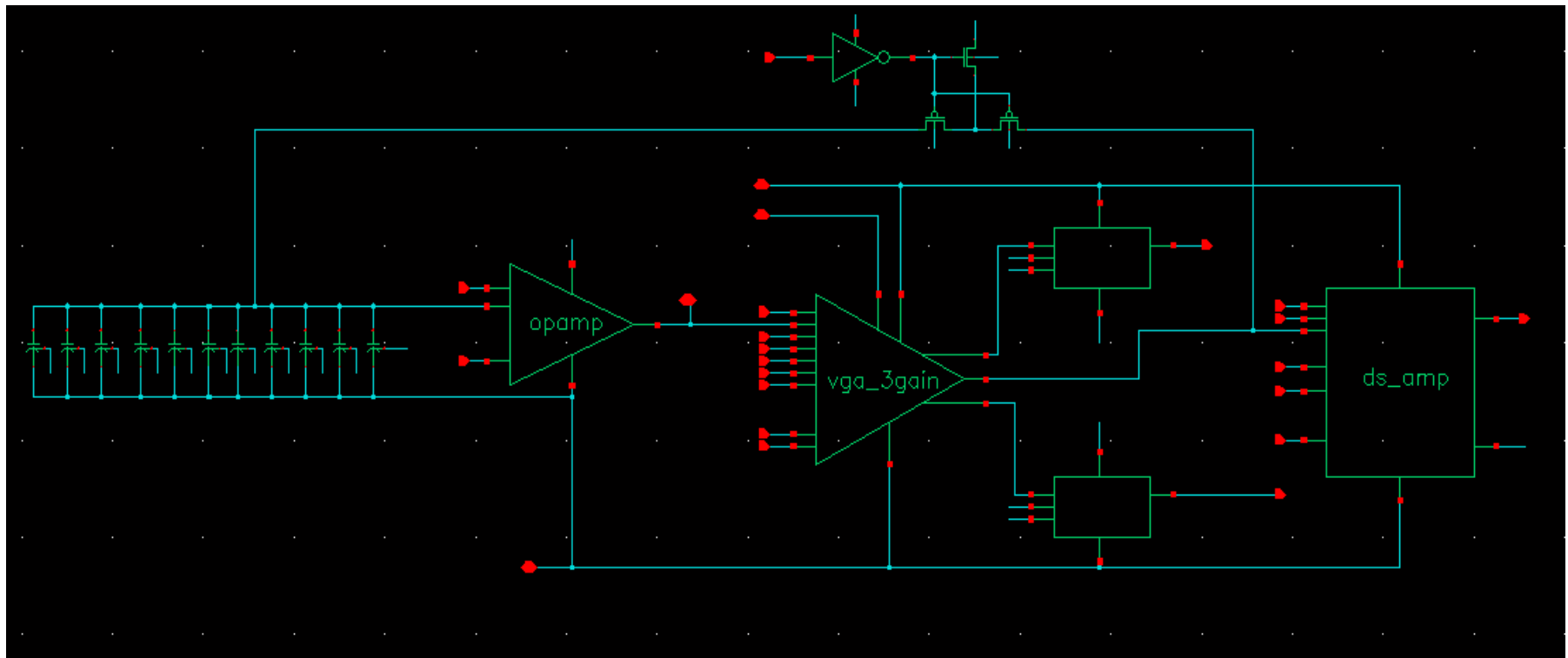


Static current consumption: $\sim 250 \mu\text{A}$

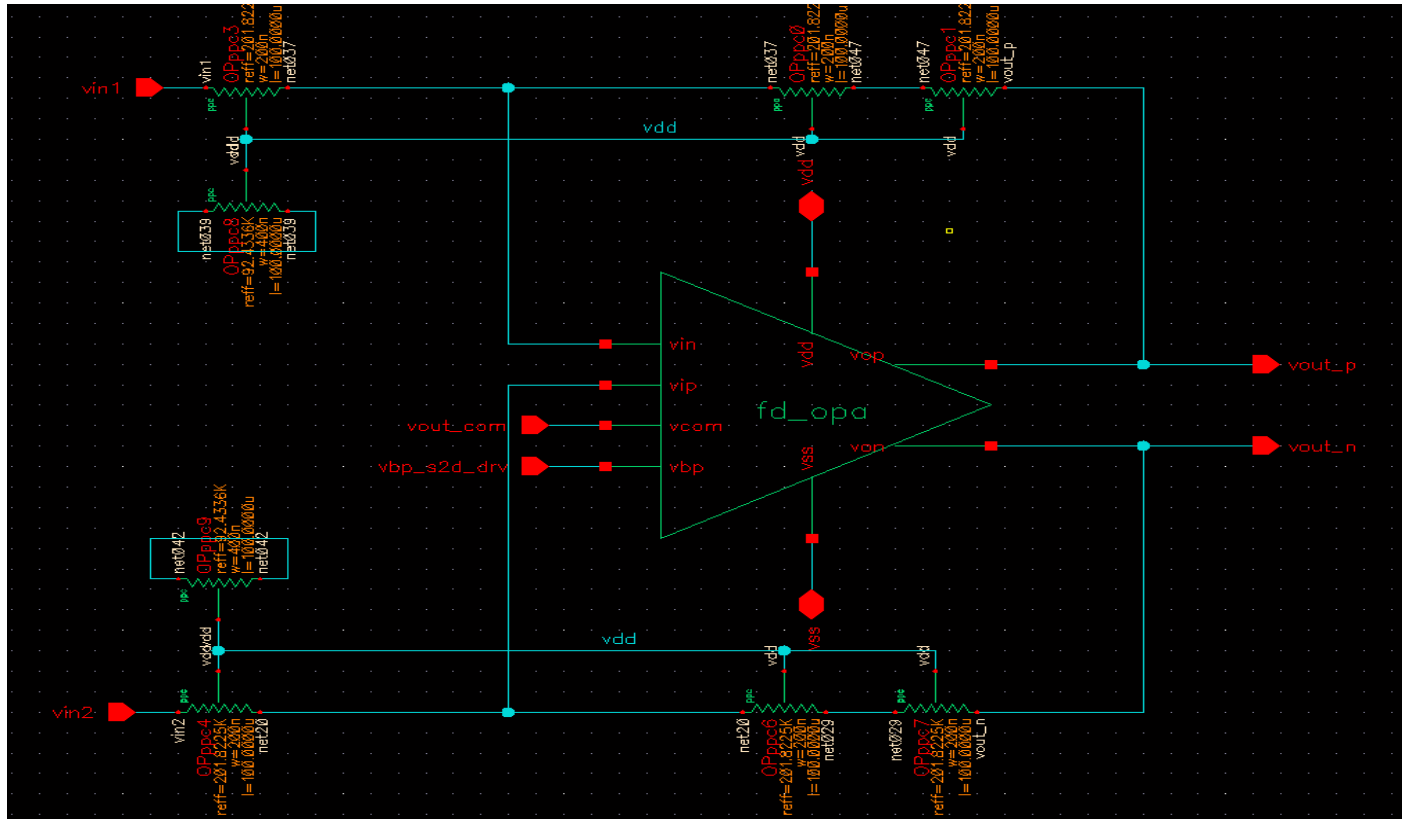
Static leakage current compensation



Dynamic leakage current compensation



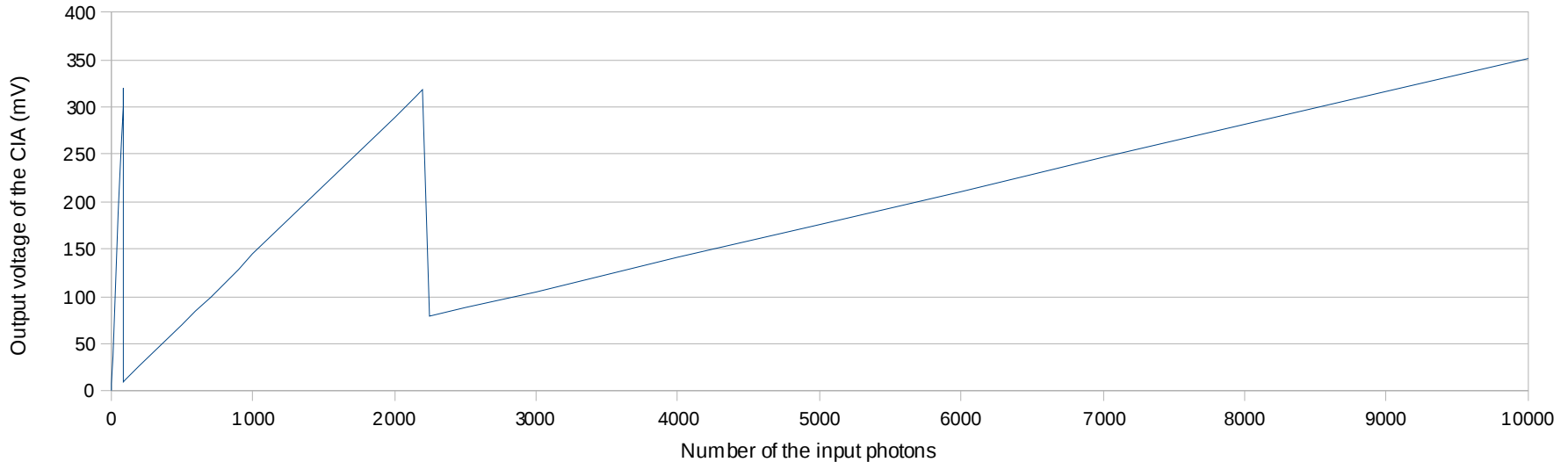
Single-ended to differential converter



- › Doubling the output dynamic range.
- › Improving the noise rejection ability (especially for the off-chip signal processing).

Simulation results

The output voltage of the CIA vs the number of the input photons



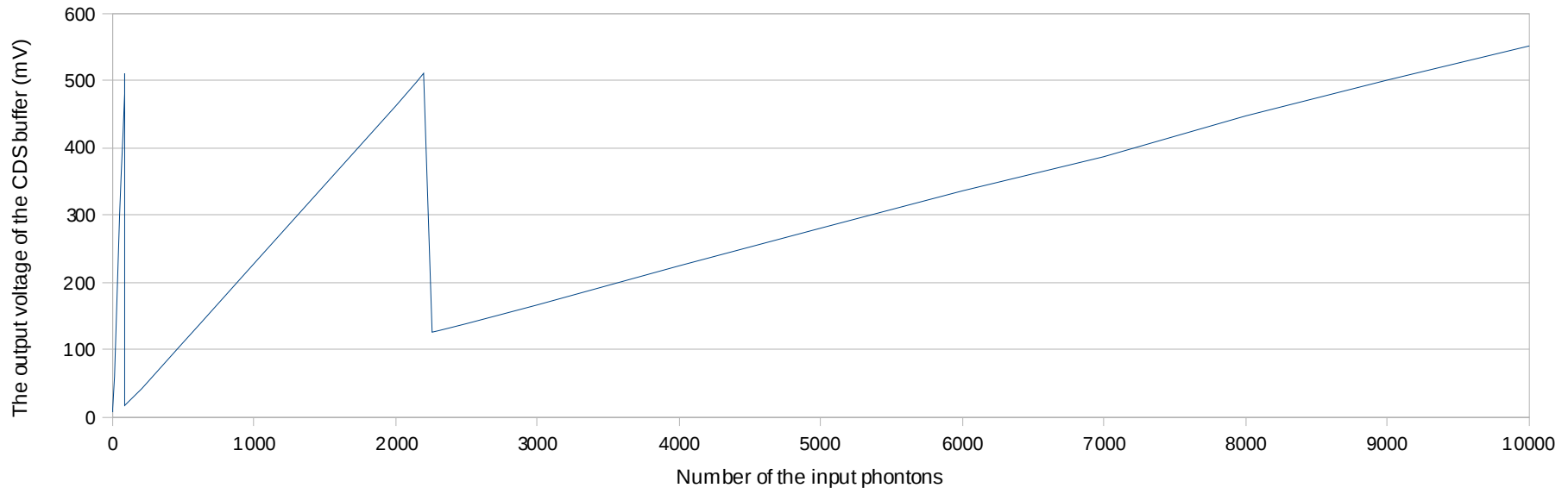
Gain 1: 3.78 mV / photon, linearity error < 0.8%

Gain 2: 0.145 mV / photon, linearity error < 3%

Gain 3: 0.035 mV / photon, linearity error < 0.9%

Simulation results

The output voltage of the CDS buffer vs the number of the input photons



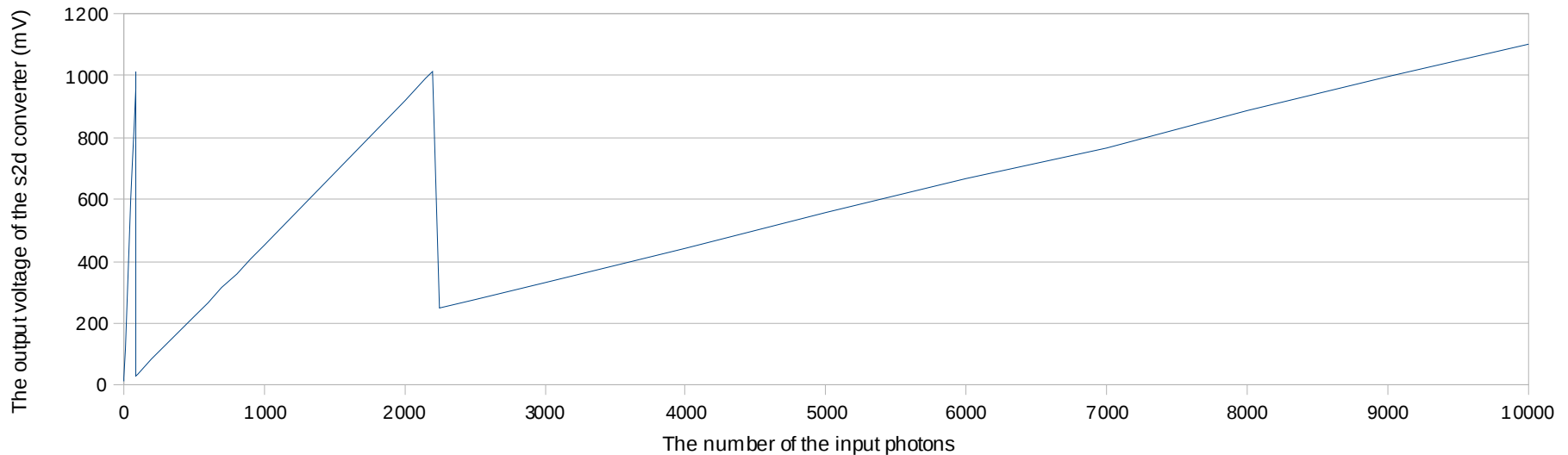
Gain 1: 5.99 mV / photon, linearity error < 0.6%

Gain 2: 0.23 mV / photon, linearity error < 1%

Gain 3: 0.055 mV / photon, linearity error < 1.4%

Simulation results

The output voltage of the single-ended to differential converter vs the number of the input photons

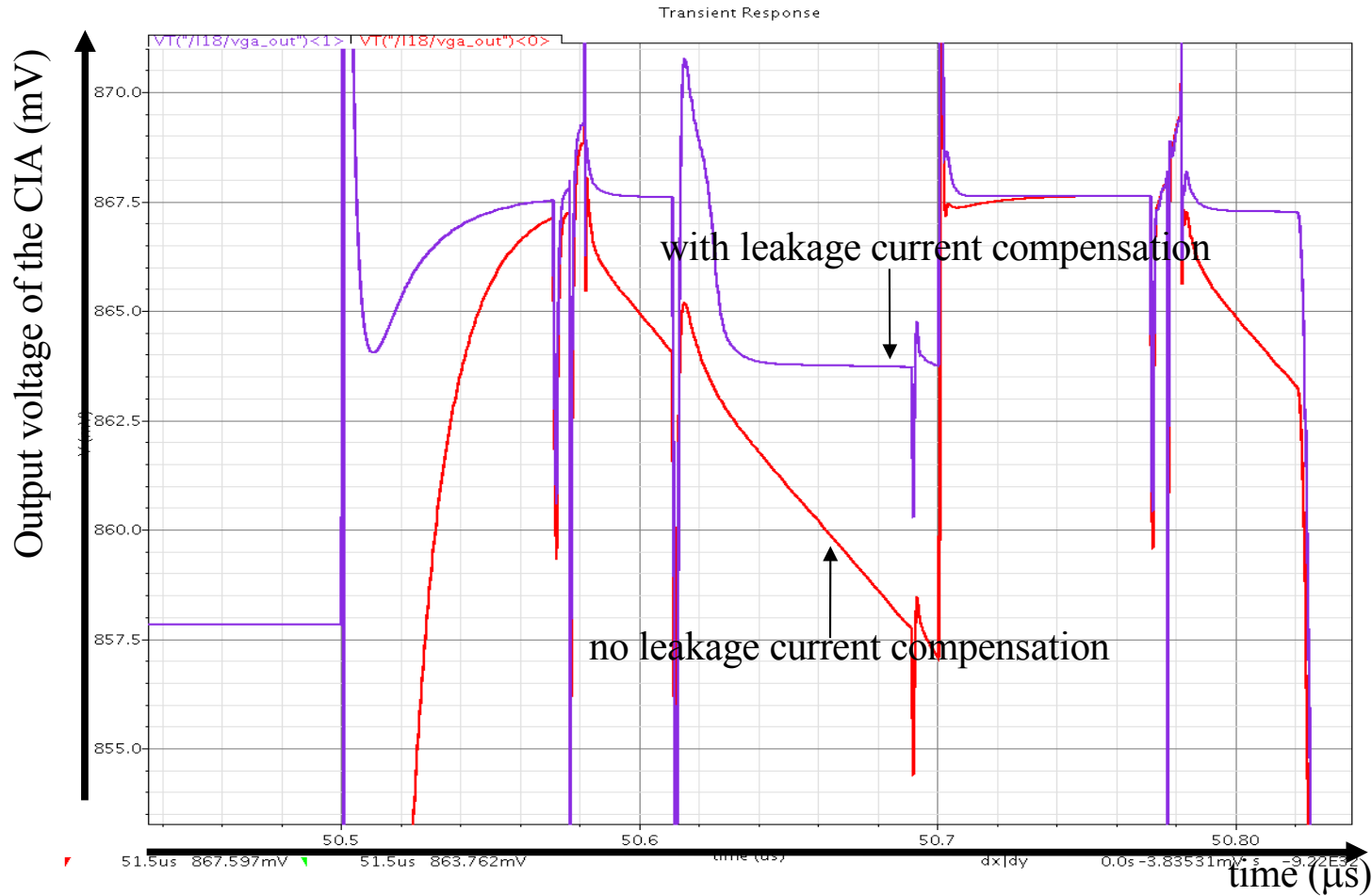


Gain 1: 11.9 mV / photon, linearity error < 0.8%

Gain 2: 0.46 mV / photon, linearity error < 1%

Gain 3: 0.11 mV / photon, linearity error < 2%

Simulation results

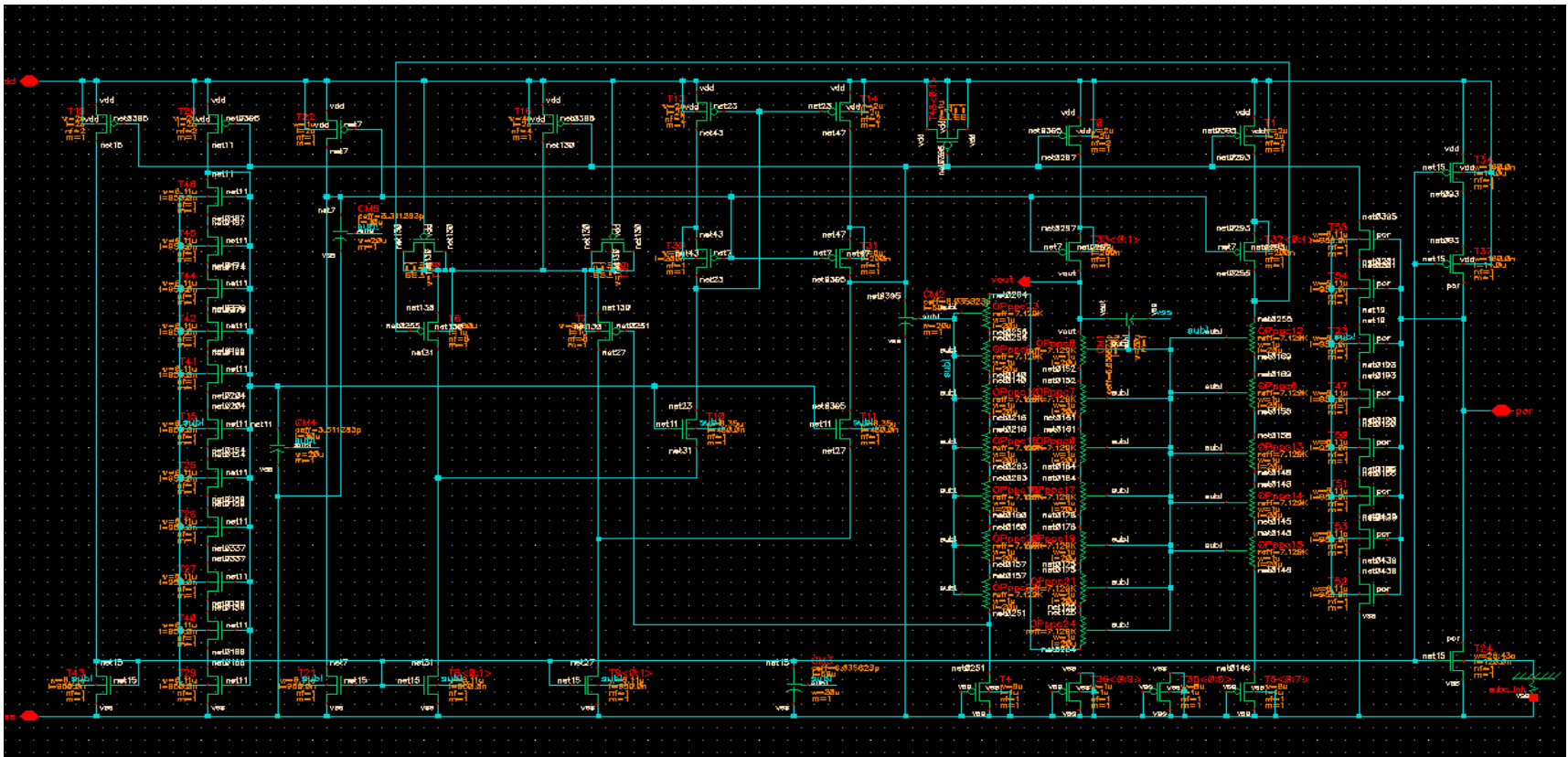


Transient simulation of the CIA with and without dynamic leakage current compensation with 10 nA leakage current and single photon at the input.

Noise analysis

- › The CIA filters the high frequency noise at its output.
 - › The CDS stage functions as a high pass filter. It removes the low frequency noise caused by the CIA and the sensor leakage current.
 - › High DC gain of the CIA increases the bandwidth and output noise.
 - › The simulated CIA output voltage is 3.78mV @ single input photon.
 - › The simulated output noise of the CIA
 - For gain1 < 0.181 mV (equivalent to 143 input e⁻).
 - For gain2 < 0.179 mV (equivalent to 2350 input e⁻).
 - For gain3 < 0.178 mV (equivalent to 15440 input e⁻).
- with 1 photon -> 3000 e⁻

Radiation hard bandgap reference



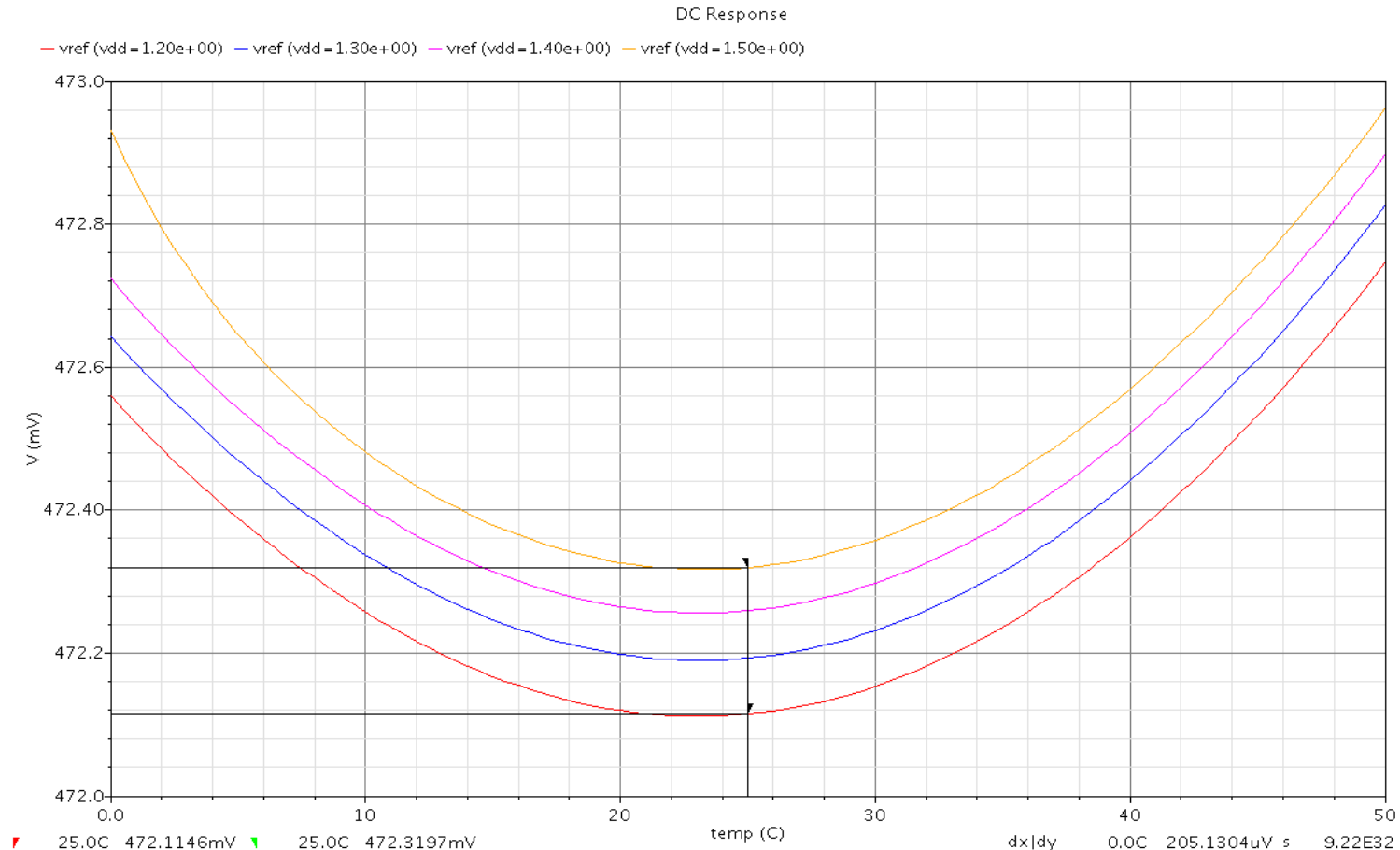
Schematic of the bandgap

Radiation hard bandgap reference

- › Using dynamic threshold MOSFET (DTMOS) instead of diode for improving radiation tolerance [1].
- › Simulated output voltage: 472 mV.
- › Simulated output voltage variation $< 700 \mu\text{V}$ for $0^\circ\text{C} < T < 50^\circ\text{C}$.
- › Simulated output voltage variation $< 300 \mu\text{V}$ for $1.2\text{V} < V_{\text{DD}} < 1.5\text{V}$.

[1] V. Gromov et al., “A radiation hard bandgap reference circuit in a standard $0.13 \mu\text{m}$ CMOS technology”, IEEE Trans. Nuclear Science, Vol. 54, pp. 2727-2733, Dec. 2007.

Radiation hard bandgap reference



Simulation results of the bandgap output voltage.
Variation < 1 mV over temperature and VDD range

Other test circuitry and development on the designkit

- We implemented new design kit features for precise simulation and extraction of enclosed gate transistors. Four enclosed gate transistors (3 NMOS and 1 PMOS) are drawn for characterization and verification of the new features.
- A fully differential opamp.
- An inverter-based ring oscillator.

Conclusions

- Taped out test chip with:
 - 3 different readout amplifiers
 - Radiation hard bandgap amplifier
 - Enclosed gate transistors for characterization
- Simulated performances of the readout amplifier:
 - High dynamic range
 - High linearity
 - Low noise
 - Dynamic leakage compensation
- Simulated performances of the radiation hard bandgap reference:
 - Very small variations over temperature and VDD ranges.



Thanks for your attention !