Capacitor and switch arrays included in the HPAD_0.1 chip and proposed tests

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Capacitor and Switch Arrays

Essential requirement leakage currents as small as possible in order to avoid the degradation of stored data (~1fA)

Leakage currents occur

- at source and drain nodes of FETs in the sub-threshold region
- through the SiO_2/Si_3N_4 dielectric of capacitors and transistor gates (tunneling electrons)

Capacitors

- MIM capacitors
- Dual MIM capacitors
- DGN capacitors

Switches

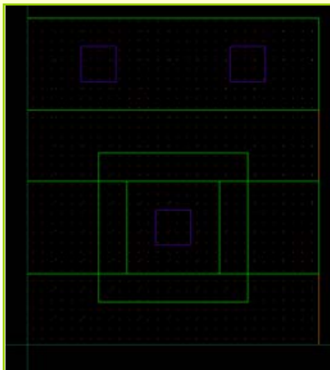
- Long DGPMOS
- Dual DGPMOS

Capacitor Arrays

MIM capacitor array

Single capacitor characteristics:

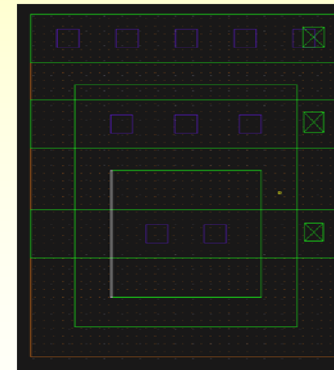
- **Area: 5.24 µm x 5.24 µm**
- **Capacitance: 59.57 fF**
- **Number of cells: 8400**



Dual MIM capacitor array

Single capacitor characteristics:

- **Area: 5 µm x 5 µm**
- **Capacitance: 680.17 fF**
- **Number of cells: 876**



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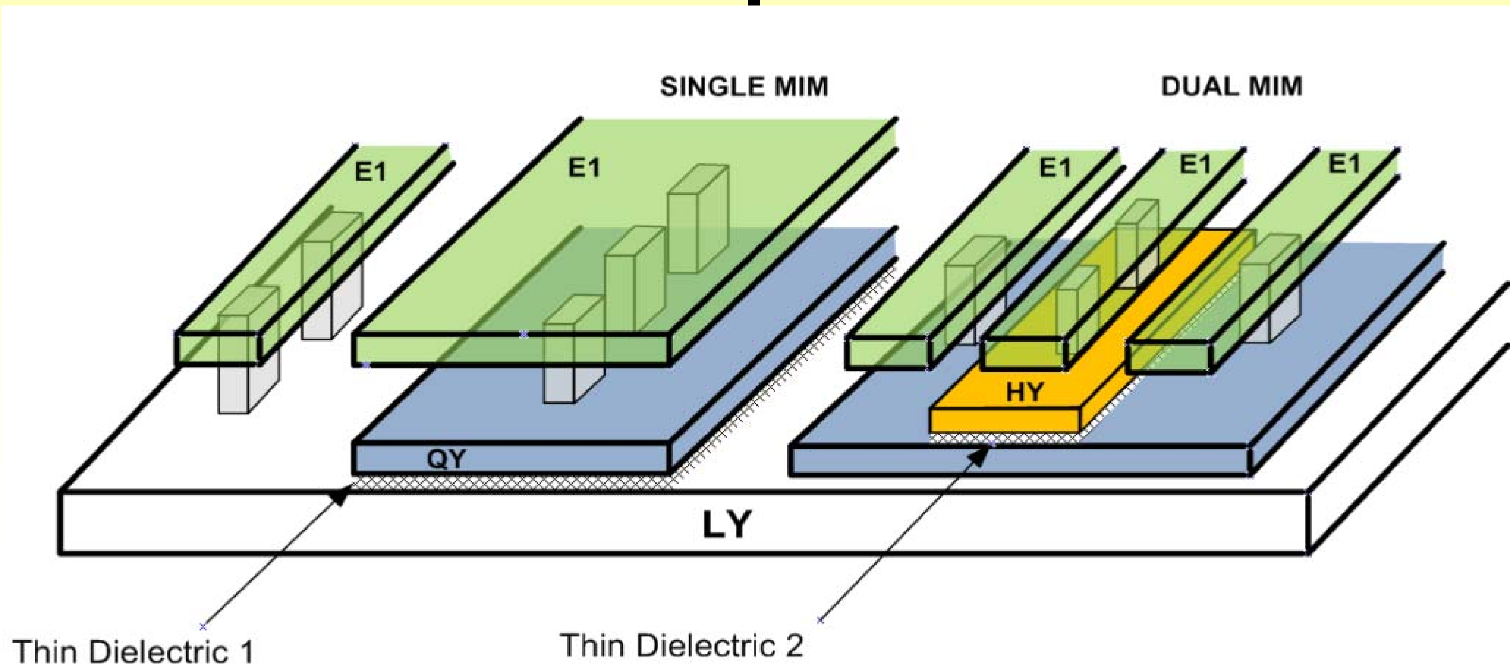
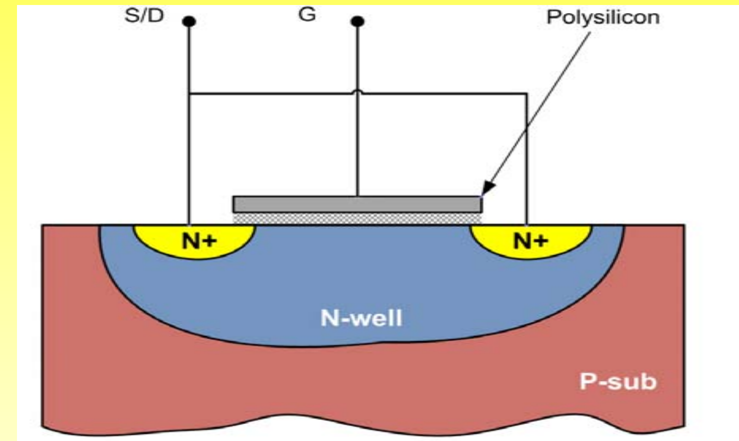


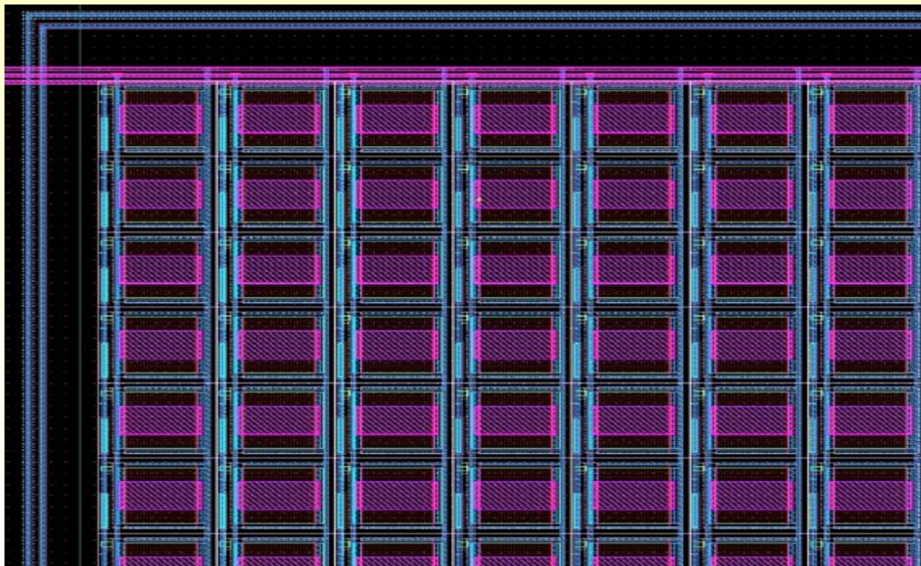
Capacitor Arrays

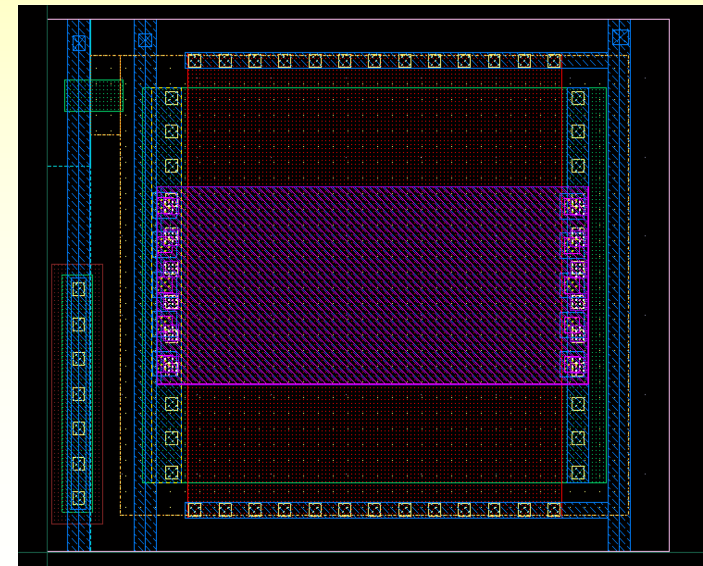


DGN capacitor array

Single capacitor characteristics:

- Area: 5 µm x 5 µm
- Capacitance: 51.1 fF….147.7 fF
- Number of cells: 8880

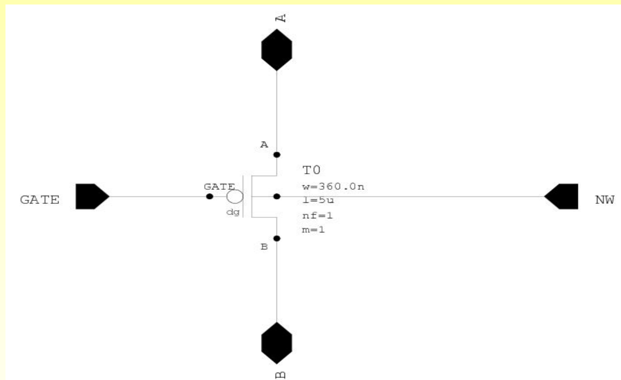


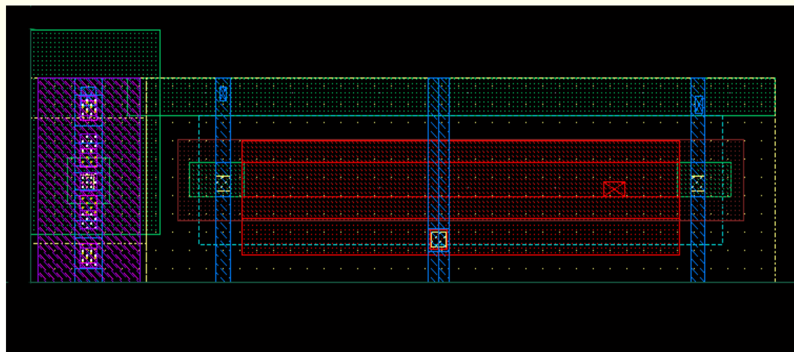


Switch Arrays

Long DGPMOS array
(thick-oxide PMOS)

- Width: 0.36 µm
- Length: 5 µm
- Number of cells: 27060



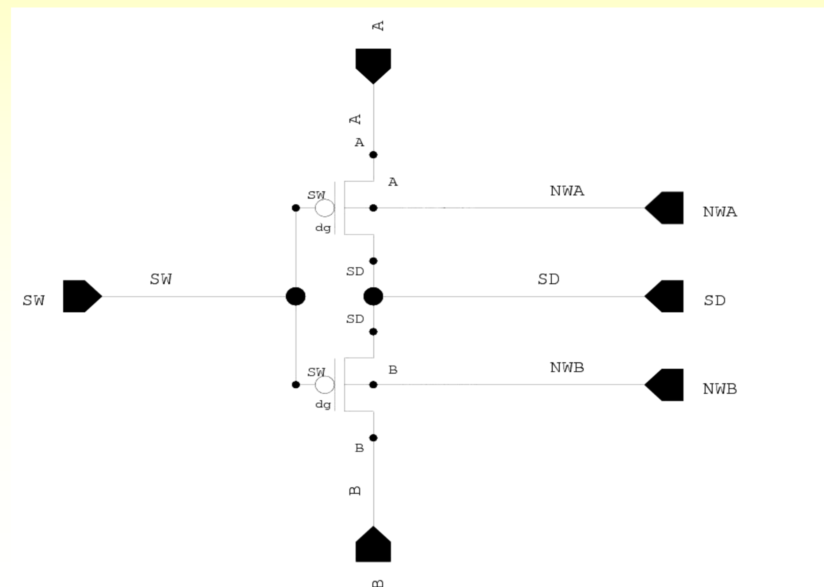


Dual DGPMOS array
(thick-oxide PMOS)

Linear

ELT

Same schematic



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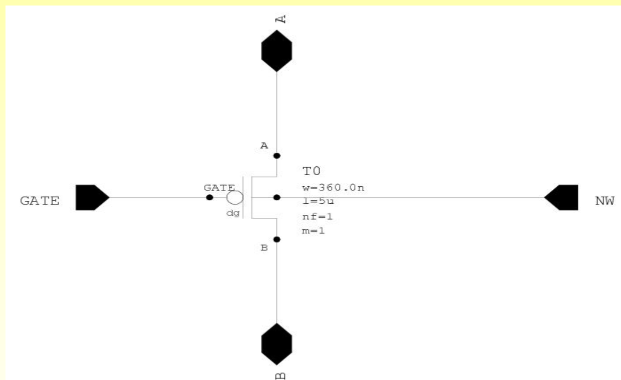

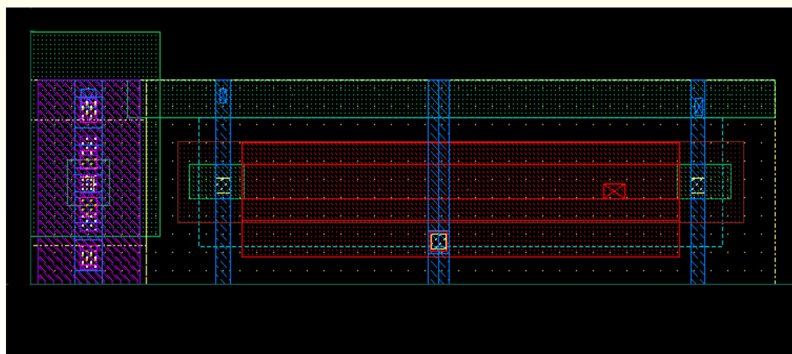

Dual DGPMOS array (thick-oxide PMOS)

Linear

- W/L_A: 0.36 µm / 0.24 µm
- W/L_B: 0.36 µm / 2 µm
- Area: 8.19 µm x 4.2 µm
- Number: 27060

ELT

- W/L_A: 2.4 µm / 0.24 µm
- W/L_B: 2.4 µm / 0.24 µm
- Area: 7.65 µm x 2.98 µm
- Number: 27060

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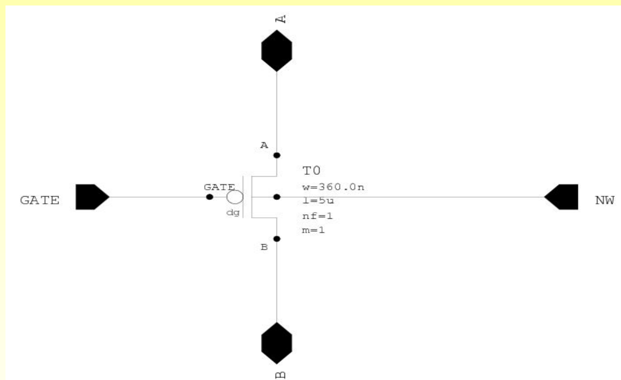
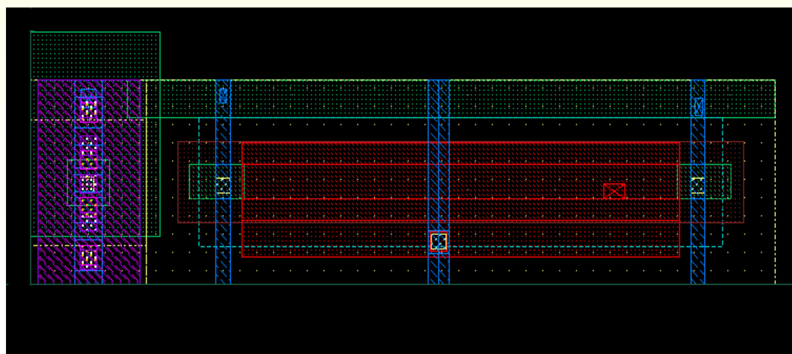
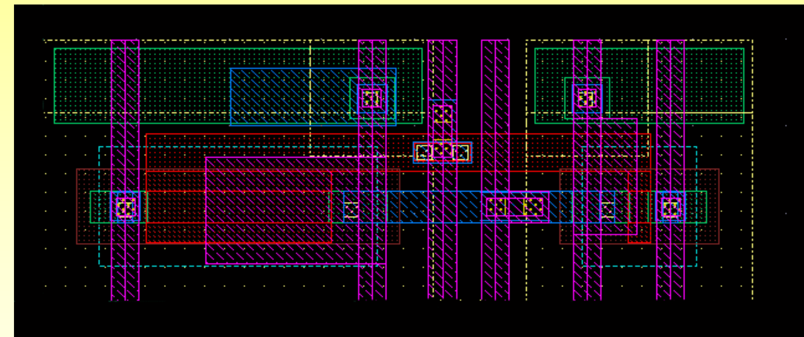


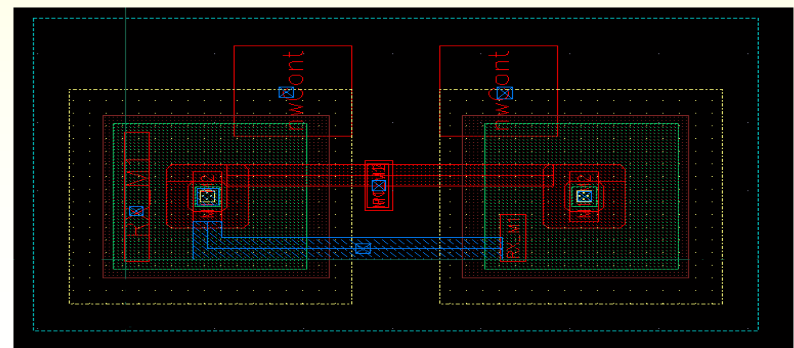


Dual DGPMOS array (thick-oxide PMOS)

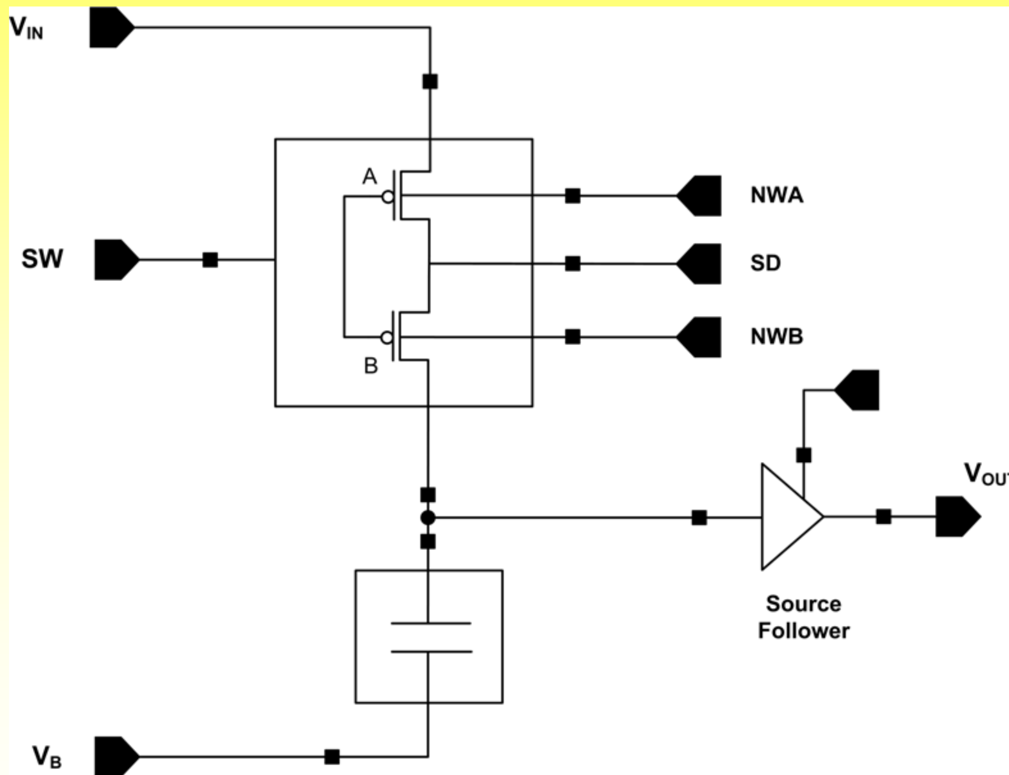
Linear



ELT



Sampling Cell

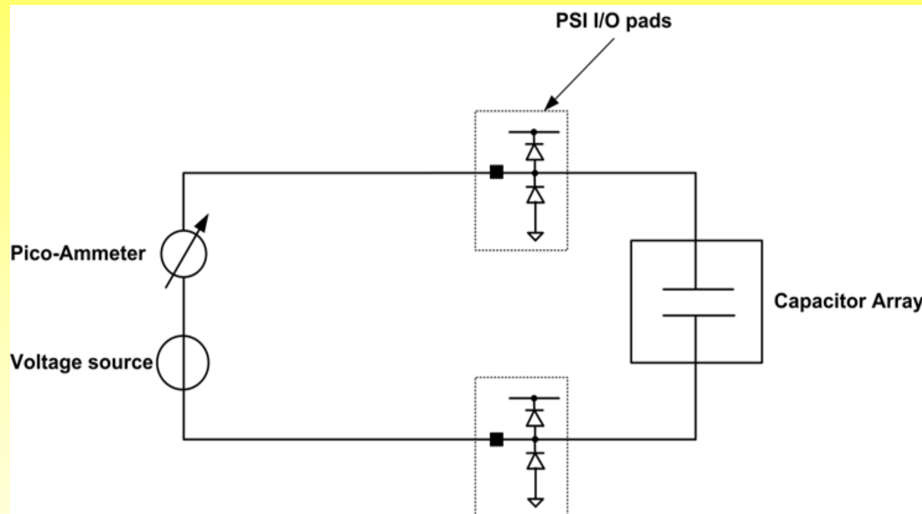


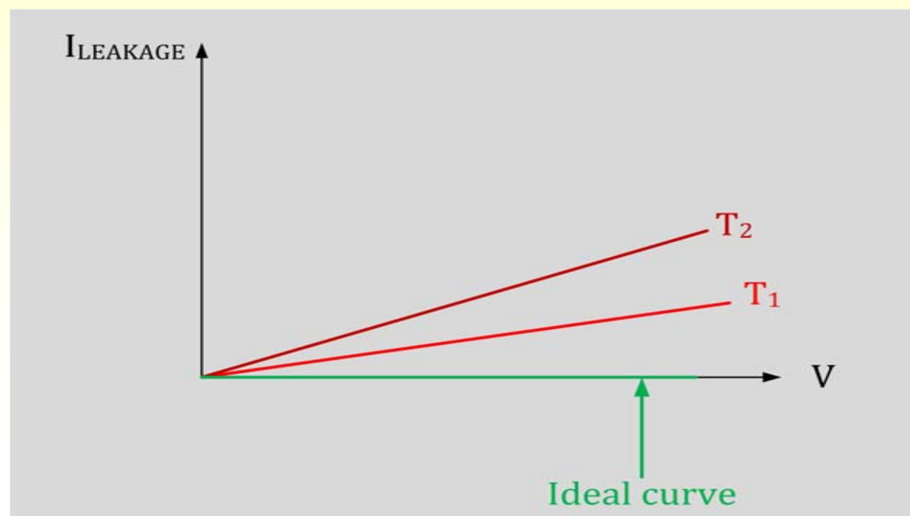
Connections which can reduce the leakage:

- N-well connected to the highest potential (V_{DD})
- Unity gain buffer which bootstraps bulk and the intermediate SD node

Test Plan

Capacitor Arrays





Measurement Circuit

- Pico-Ammeter
- Voltage source which biases the array

Considerations

- Leakage current due to the oxide leakage
- PSI I/O pads are minimum size ESD structures. Leakage introduced by these pads is unknown

Parameters

-» Temperature (climate chamber)

-» Radiations (before and after irradiation)

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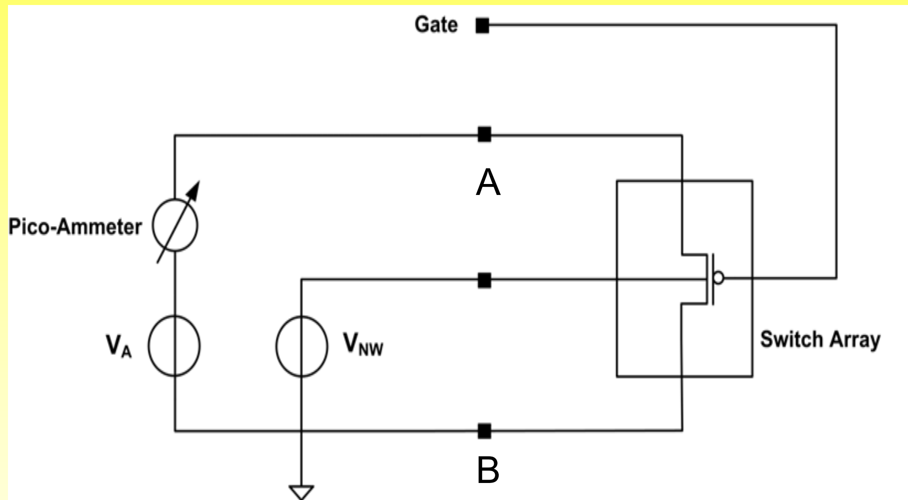
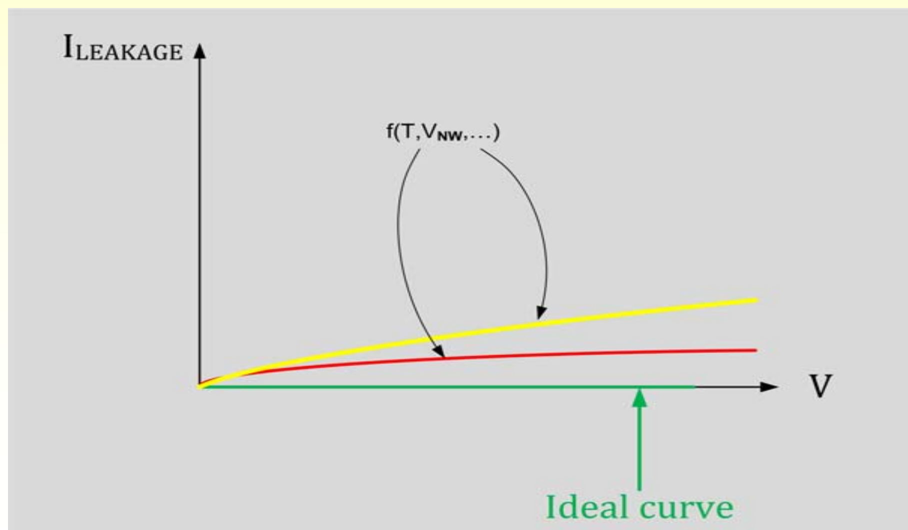
Test Plan

Switch Arrays: LONG DGPMOS





Measurement Circuit

- Pico-Ammeter
- Voltage source across source-drain

Considerations

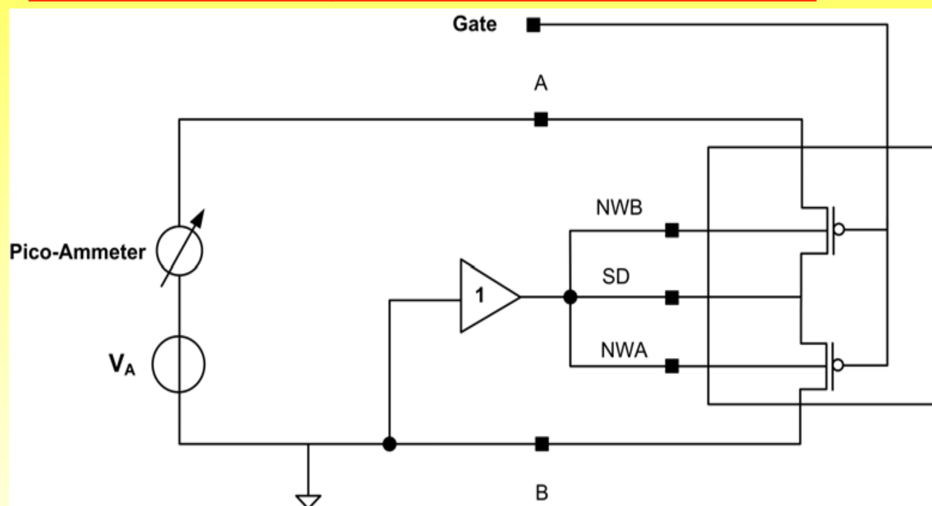
- U_B=0, $U_A \geq 0$, U_{gate} as high as possible

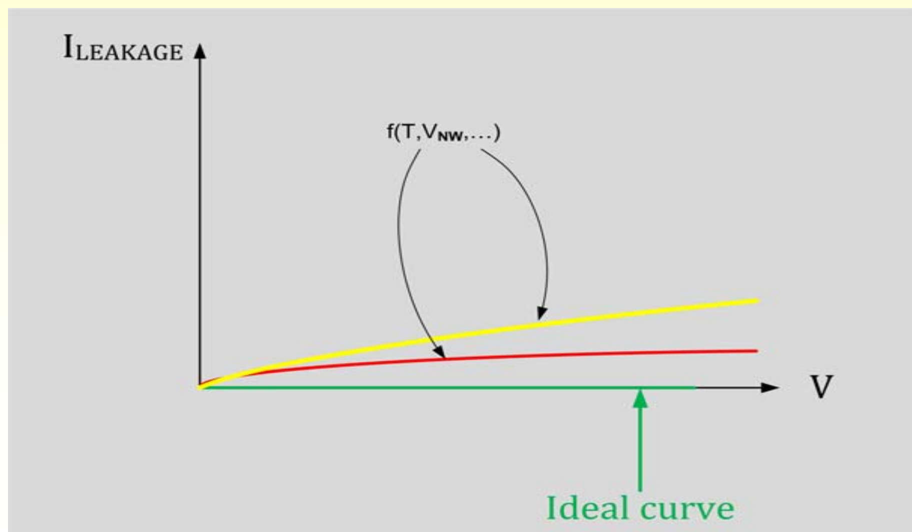
Parameters

-» Temperature (climate chamber)
-» Radiations (before and after irradiation)
-» V_{NW}

Test Plan

Switch Arrays: DUAL DGPMOS





Measurement Circuit

- Pico-Ammeter
- Voltage source across source-drain
- Unity Buffer for enhanced bootstrapping

Considerations

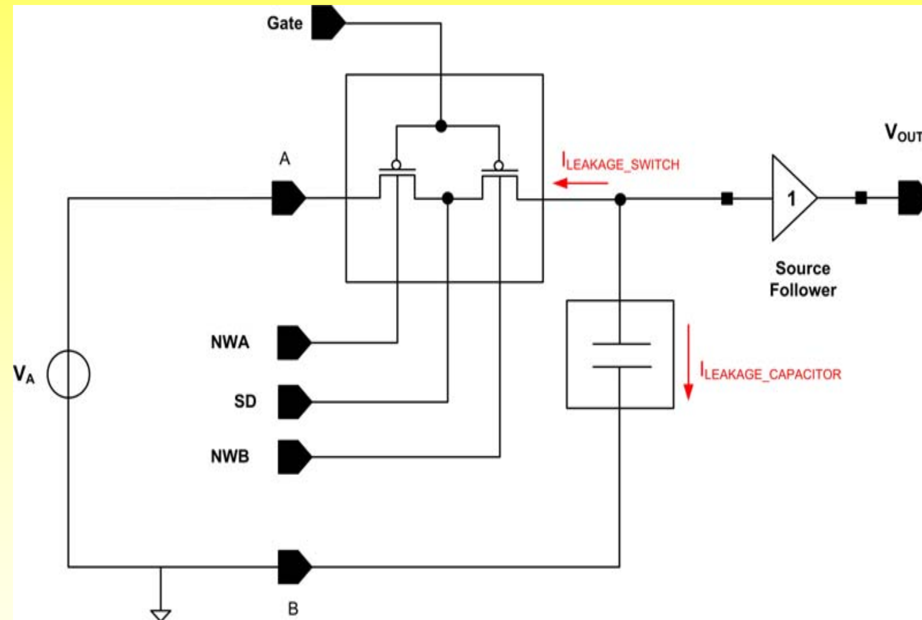
- Buffer introduces an additional power consumption (only if strictly necessary)

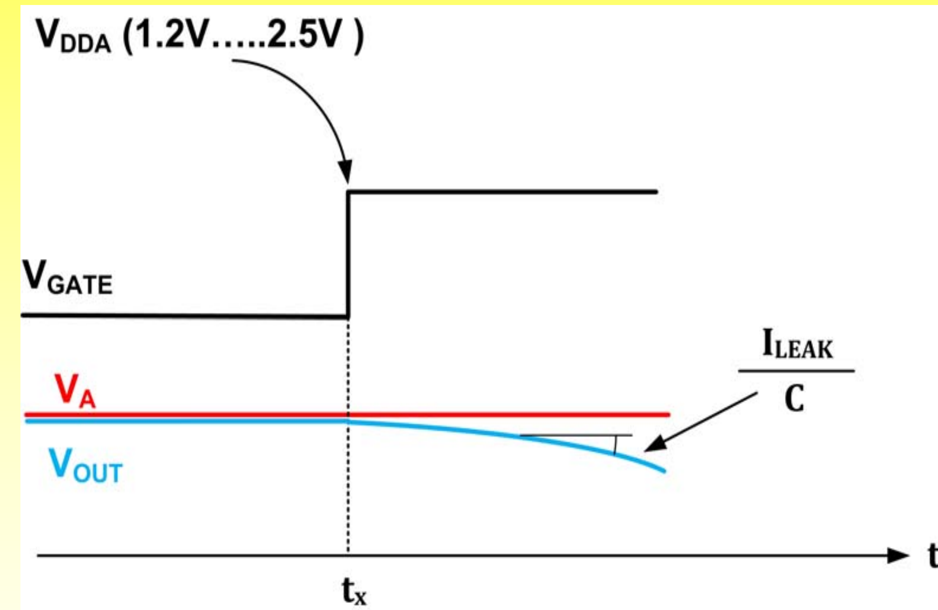
Parameters

-» Temperature (climate chamber)
-» Radiations (before and after irradiation)
-» V_{NWA} , V_{NWB}, V_{SD}

Test Plan

Sampling Cell: dynamic measurement





- Voltage measurement (V_{OUT})
- Indirect measure of the leakage

Parameters

-» Temperature (climate chamber)

-» Radiations (before and after irradiation)

-» V_{NWA}, V_{NWB}, V_{SD}

Conclusions

- The hpad_0.1 chip consists mainly of test structures (MIMCap, DualMIMCap,DGNCap, DGPMOS)
- All these structures will be tested to characterize leakage currents
- Leakage currents can be reduced by means of different connections of the sampling cell pins (bulk effect to decrease sub-threshold currents)
- The proposed leakage measurements are essentially static measurements for each single array and dynamic for the sampling cell