# WP 2.4 Interface electronics

Status of different boards
Status of the firmware
Information from WP2.3 “vacuum board”, S.Smoljanin

Summary and Outlook

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DESY-FEB, May 8th 2015

Summary for all contributors to WP2.4

# General Status: Module boards

Analogue mother board: 16 needed

- 3 in hand with old gain
- 17 in hand with up-to-date gain

Analogue daughter: 16 needed

- 23 in hand

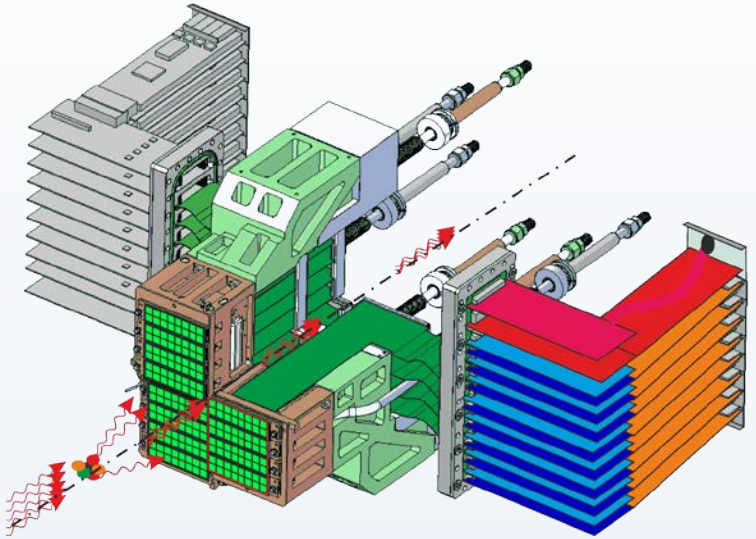
2 slot backplanes

12 in hand (basic tests)

8 slot backplane: 2 needed

2 in hand and

3 in workshop for population



Digital Carrier: 16 needed

- 3 in hand old layout
- 3 in hand modified layout
- 17 more prepared for population after tests

Digital Mezzanine: 18 needed

- Many as multi-project

# Analogue boards

Experience while more usage in slow control programming:

- Minor modifications on $I^2C$ bus devices needed
  - all done for most modules
  - remaining are the modules in use
- Power up sequence for external devices needed:
  - First module than µC-board
  - Fix in detector head to be tested with more power supplies
  - " Reverse diode to prevent $I^2C$-bus to power to ½ -level"
- One bus repeater used outside data sheet, but finally not the problem. Only next generation boards,
  - harder fix by misplacement of IC disfavored
- Positive supply slightly increased ~ 4V: Within XFEL-agreement

With quantitative feedback from calibration:

- Gain mismatch mother/daughter 20% understood and fixed.

# Control boards

busses

- **Micro controller:**
  - 2x SPI-bus to FPGA control board
  - $I^2C$ branches to interface modules, vacuum-boards, FPGA control
  - Ethernet to external control system
  - SD-card, RS232, JTAG for internal debugging

Lately changed to modern:
Vybrid with
ARM cortex A5/M4
as SOM (system on module)

functions

- 8 isolated voltage supplies 5V/100mA for the 8 Vacuum boards
- 12 fans with each 300mA/-12V
  can be put in parallel for fewer stronger fans.
  I-settable, turn and U monitored
- Internal U, I, T, humidity monitored

layout

- mechanical options to put connectors straight or parallel to digital boards. Prices mechanics items/wires

# Micro-Controller

5 boards in hand, all modified,  2 needed for 1 Mega-Pixel

- Some hardware bugs found, fixed by wiring
  - SPI-> LVDS driver: mismatch to get double termination
  - Boot-device misleading documentation: Now SD-Card
  - Power-up in dead loop
- Programming: Fighting with misleading and faulty descriptions

  Status of hardware access:

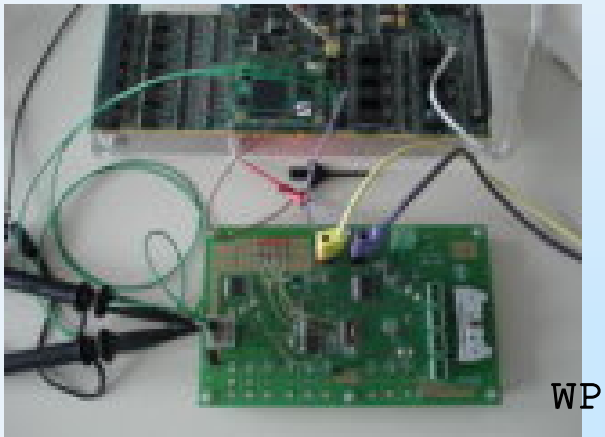
  LAN in use

  Both $I^2C$ in use

  Both SPI busses in use
- Ready to get to procedures
- LED's can be switched from LAN

➔ XFEL is informed about:

Hardware at start-point for KARABO.



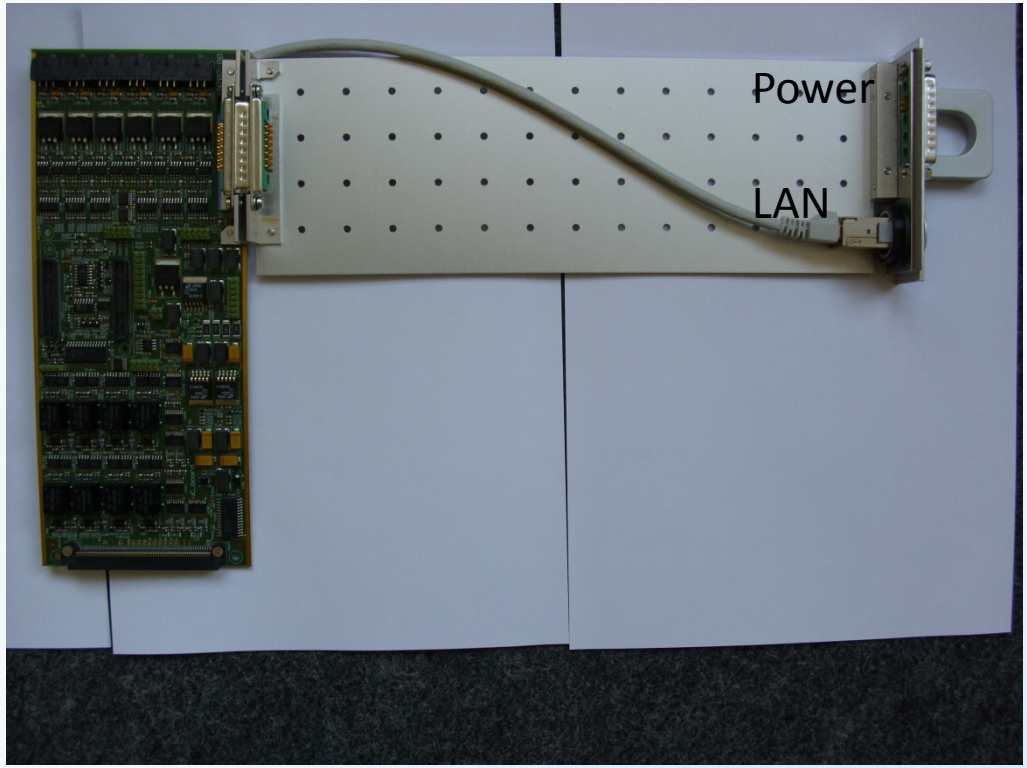
# Micro-Controller mechanical integration

Micro-controller will be similar to analogue board of module

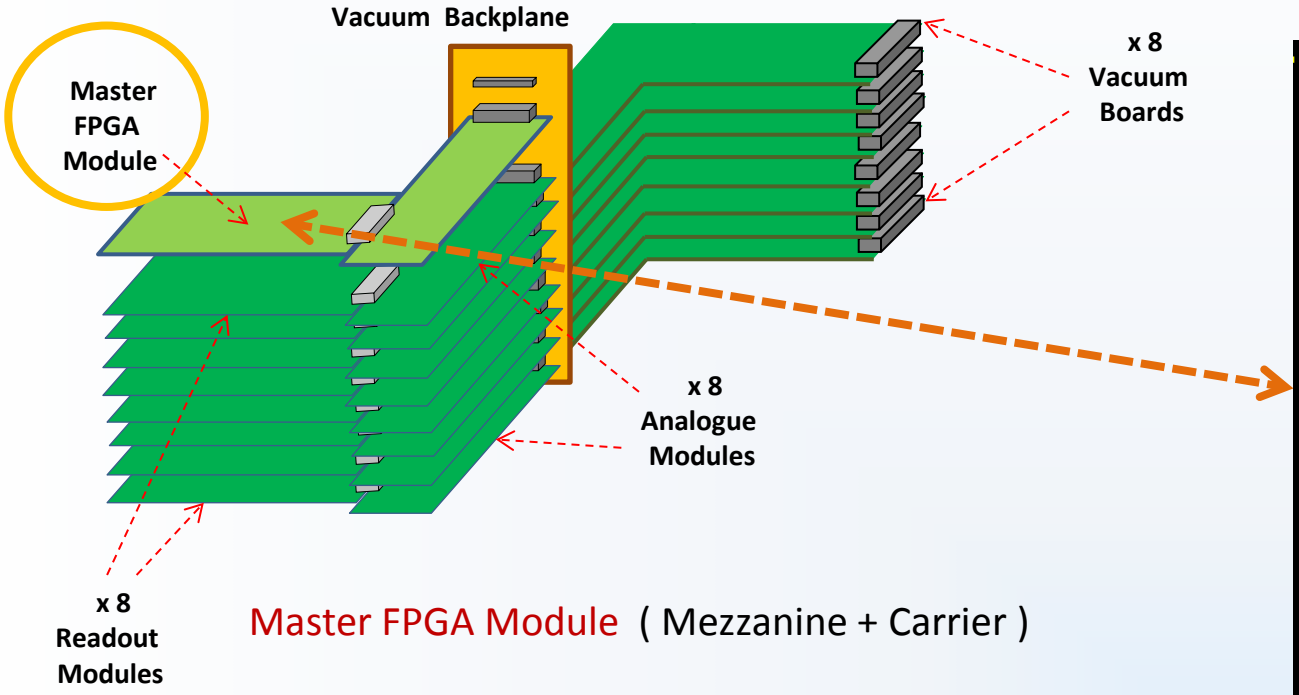
Mechanical extension with option for straight mounting.

Two systems needed, just wired and allowing hybrid-GND:
Open GND-loop for low-frequencies

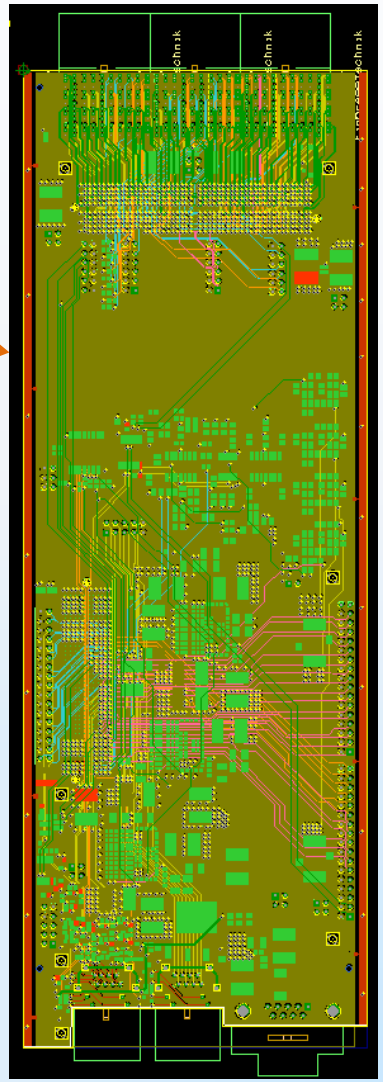
Just idea as start point for discussion
With mechanical engineering team



# Master FPGA Module




Master FPGA Carrier

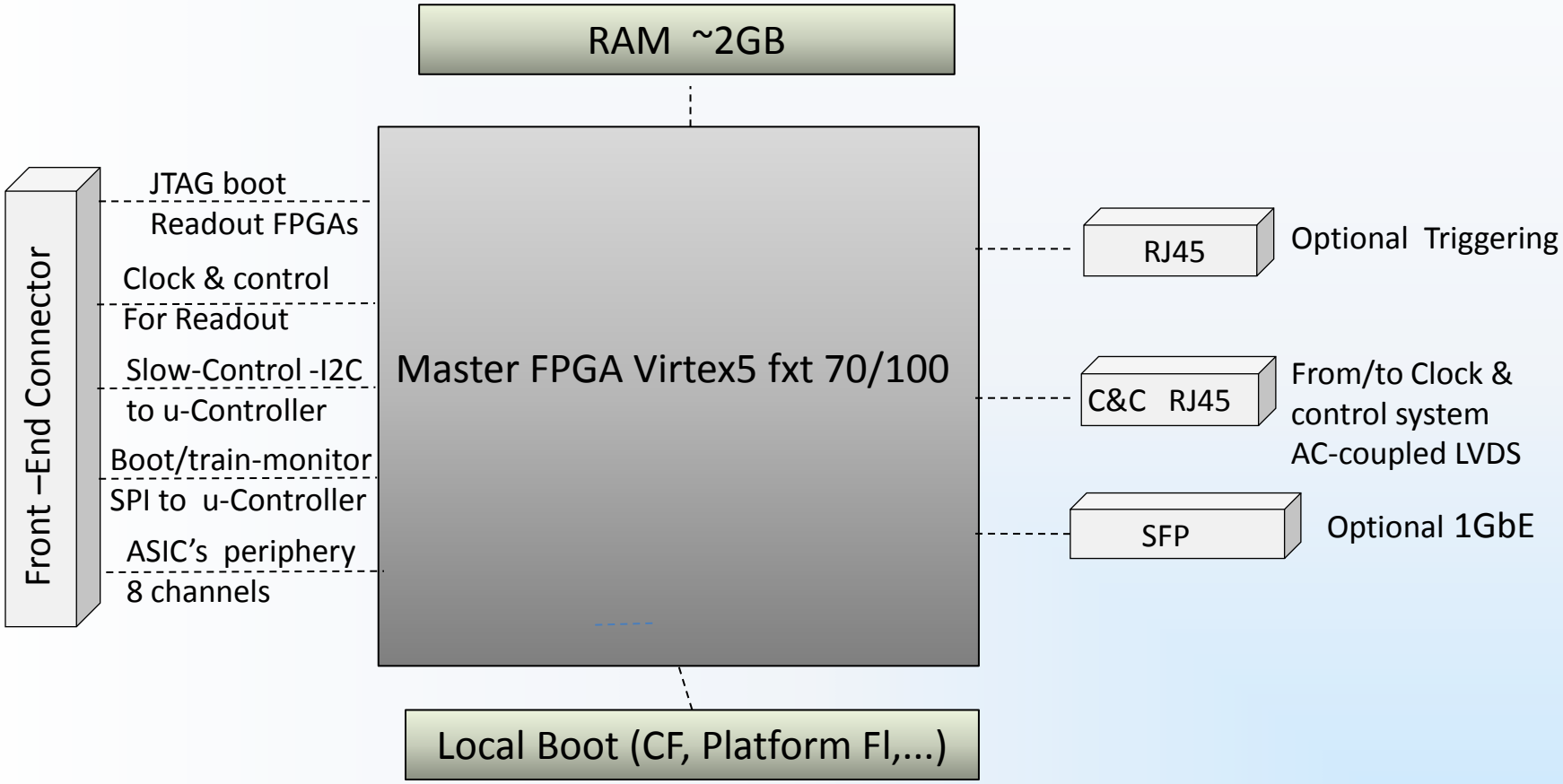


Master FPGA Module ( Mezzanine + Carrier )

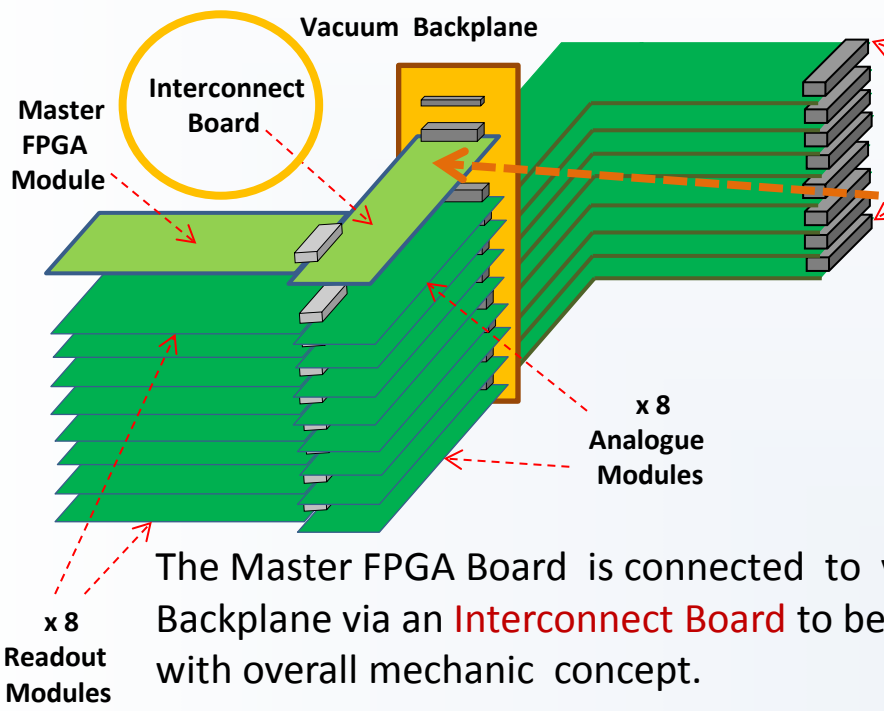
Basic functionalities:

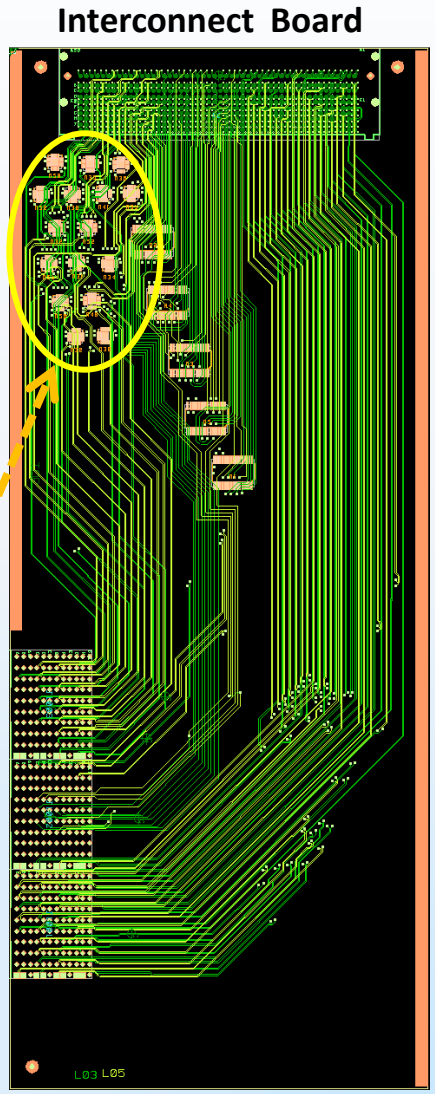
- Synchronization with Clock and Control system
- Configuration and control the ASICs through
- "AGIPD 1.0 ASIC periphery commands".
- Deliver synchronization data to Readout Modules. " data and sync. for ADC clock to ASIC"
- Re/boot Readout FPGAs

# Master FPGA Connections



# Interconnect Board




The Master FPGA Board is connected to vacuum Backplane via an Interconnect Board to be compatible with overall mechanic concept.

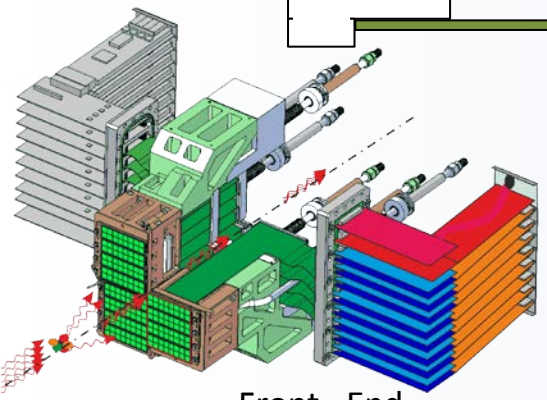
ASIC's periphery signal integrity requires FPGA-output(LVDS) translated to CML for ASIC/vacuum

Two options: By hardware modification possible:

- Fully differential transmission within data sheet
  at common mode of > 1.4V
- Two-opposite single ended
  or fully differential, but outside datasheet
  at common mode down to 0.8V…. Old vacuum boards

# Master FPGA Module

Mechanics integrates as the module electronics



Front –End Connector

Readout Carrier-Mezzanine assembly

FPGA

10 GbE

A

-5V, 4V, +12V

11.0

64.0

10GbE

30.0

Defined by Mezzanine - Carrier stack up

~ 105.0 , defined by whole construction

Front –End Connector

Master FPGA Carrier-Mezzanine assembly

FPGA

SFP+

B

C&C RJ45

+12V

95.0

# Vacuum backplane

Two boards needed and in hand

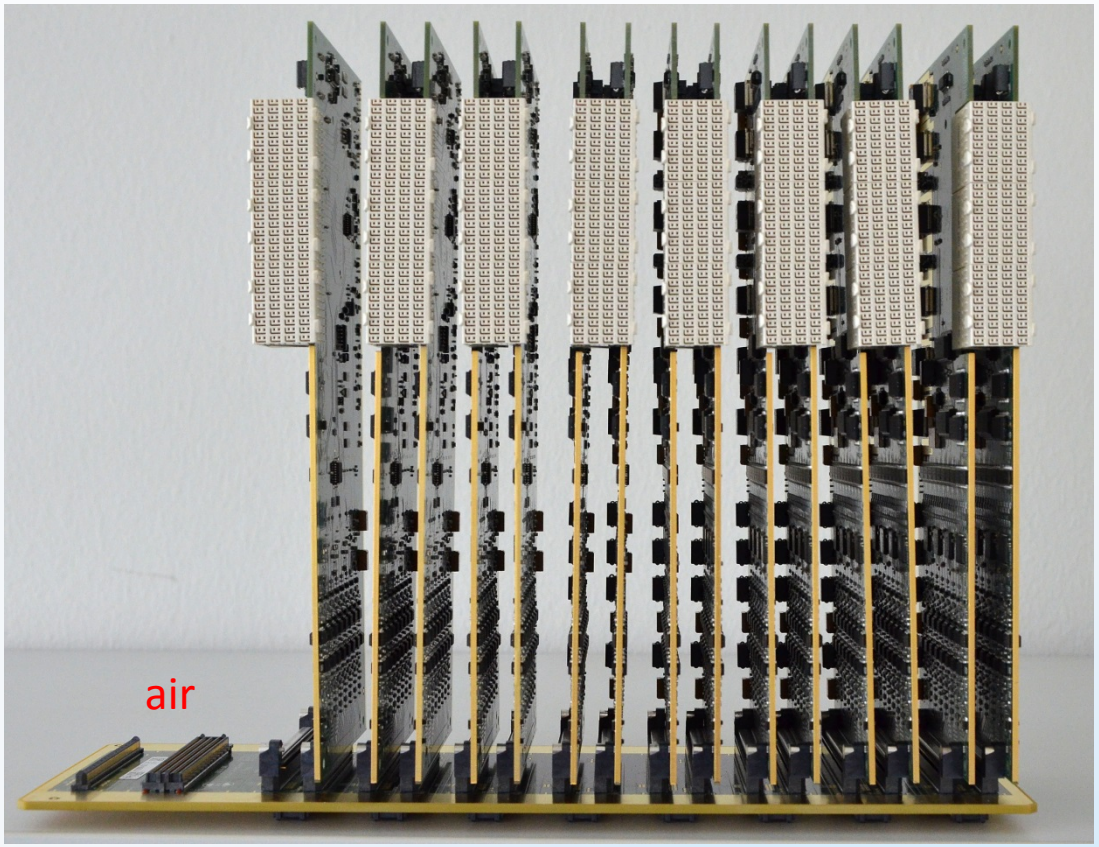
$I^2C$-bus to all slot operated

SPI not tested

Module operation only on
two-slot backplane tested

Vacuum test not yet done
… need design of mechanical support

➔ Population of three more started.



# Firmware micro-controller

Two development chains followed up:

Final board with CORTEX-SOM system and local slow control for
own monitoring and fans (no more auxiliary power for vacuum board)

➔ Field busses are configured and debugged

➔ LAN access established

➔ XFEL is informed about “LED”-switchable,
but not yet started to set up operation from control-software-package

Temporary System on ARM9 on evaluation system:

- Full branched $I^2C$ bus system operated
for analogue board and one vacuum board
- Not yet tested integration of the sub-branch for digital board
- Not possible SPI-busses:
(fall back is the usage of 1GbE to digital board directly from PC)
- $I^2C$-devices in vacuum can be set: “ Selection of ASIC”, Power up of ASIC
➔ If needed the power on of module electronics can be jumpered
to be always “ ON”

# Micro-Controller: Next steps

Building full sensor table in memory of µC.

Install „Level 1“ command for field bus access via KARABO

XFEL investigates: How to translate TANGO-software from existing PC→FPGA into KARABO
as start point for PC-software for PC→µC communication

Followed by common effort to get KARABO→µC communication established

Level-1: Command-structure ……. Level-4

“ data streamed to fieldbus “ “Procedures”

Command-counter

Command-ID Power-ON/Power-OFF

Address of fieldbus read sensor table

Number of data words write parameters

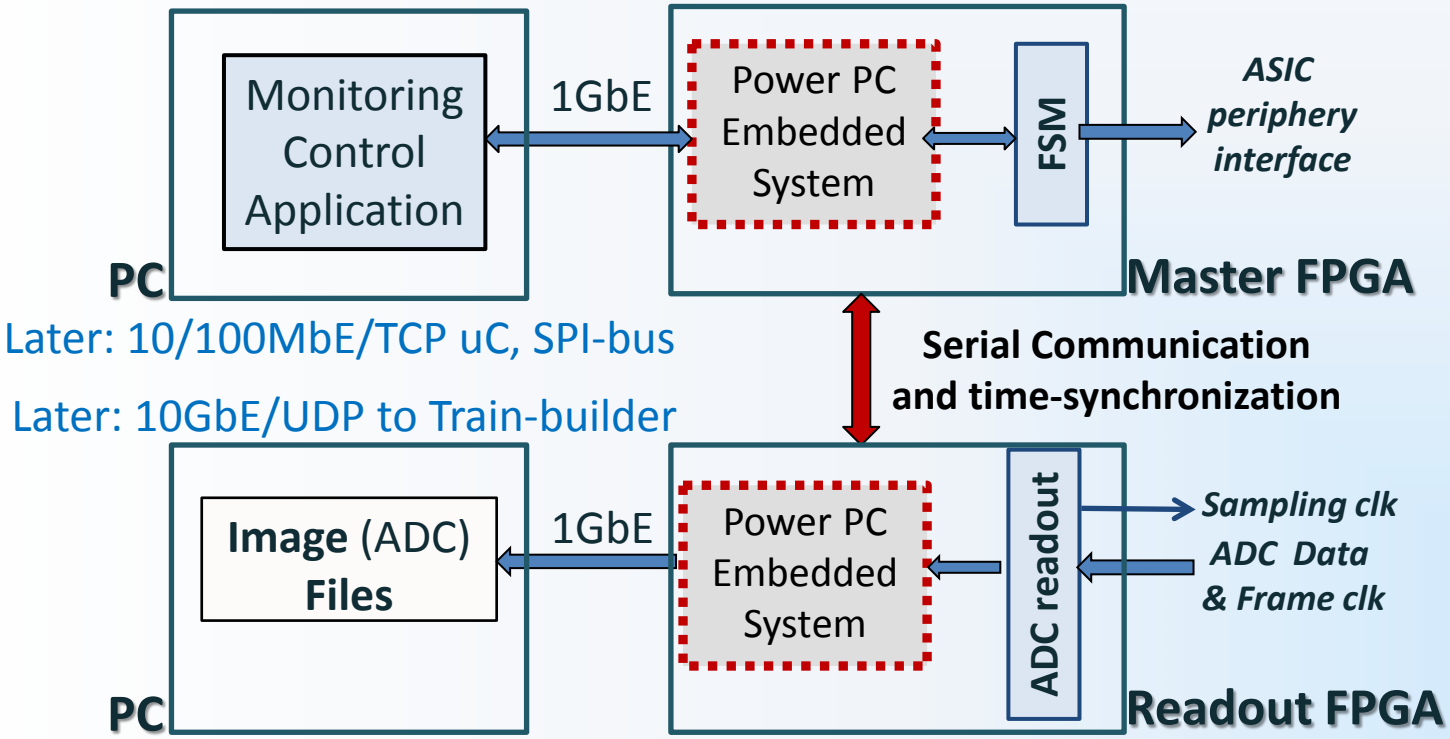
Data words

Consistency check

# Firmware Development for 1M Module

- Hardware test bench setup
  - Two FPGA boards: Master FPGA & Readout FPGA
  - Communication lines: free pins on the pin header of each board
  - Understanding and automation of ADC-FPGA timing problems
- Two individual firmware projects

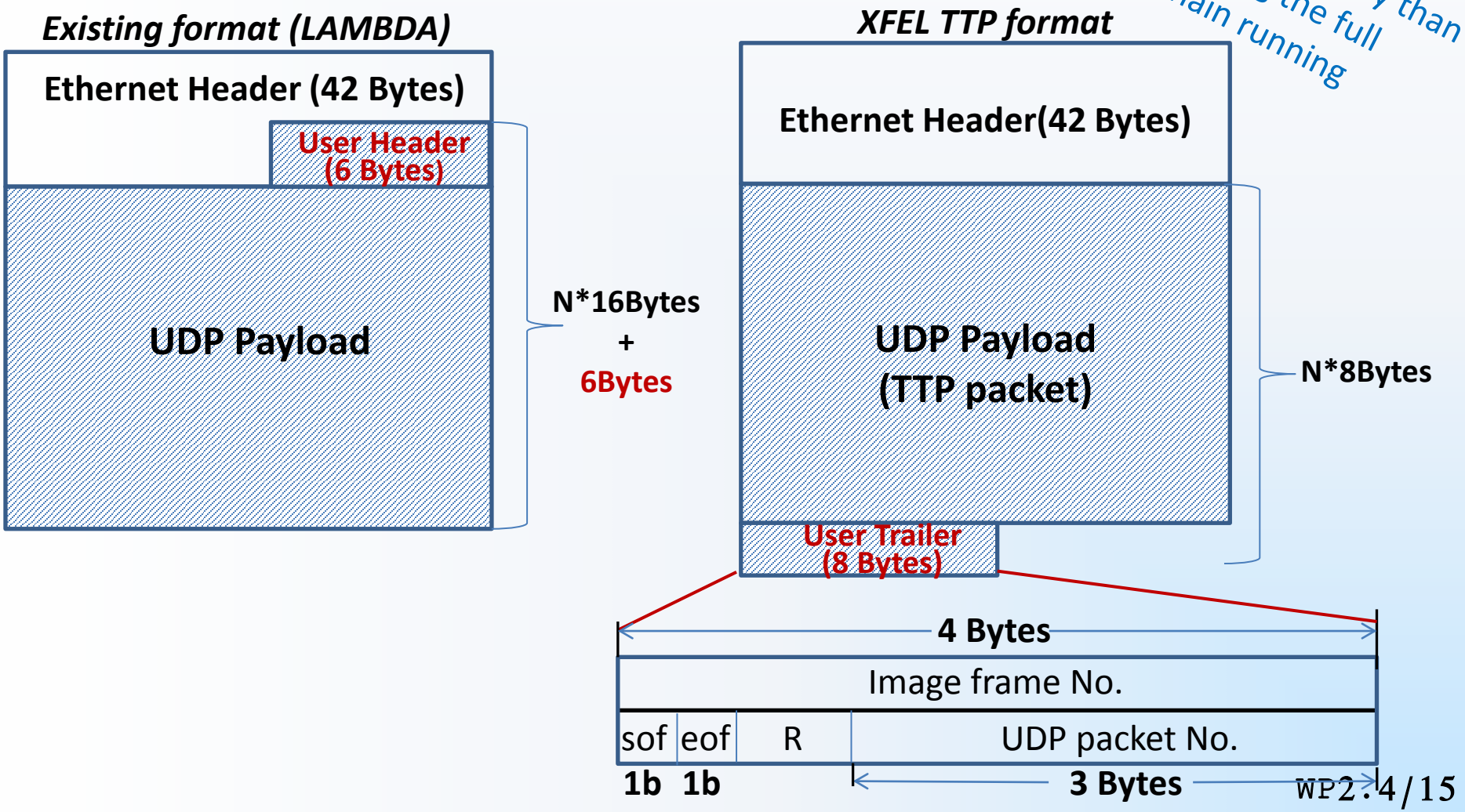
Priority in Firmware to get the full data chain running into a PC.



# 10GE Packet Format(TTP) and Train Format (XFEL)

- XFEL TTP: Train Transfer Protocol (**Train Builder**)
- Adaptation from the earlier project with same digital mezzanine

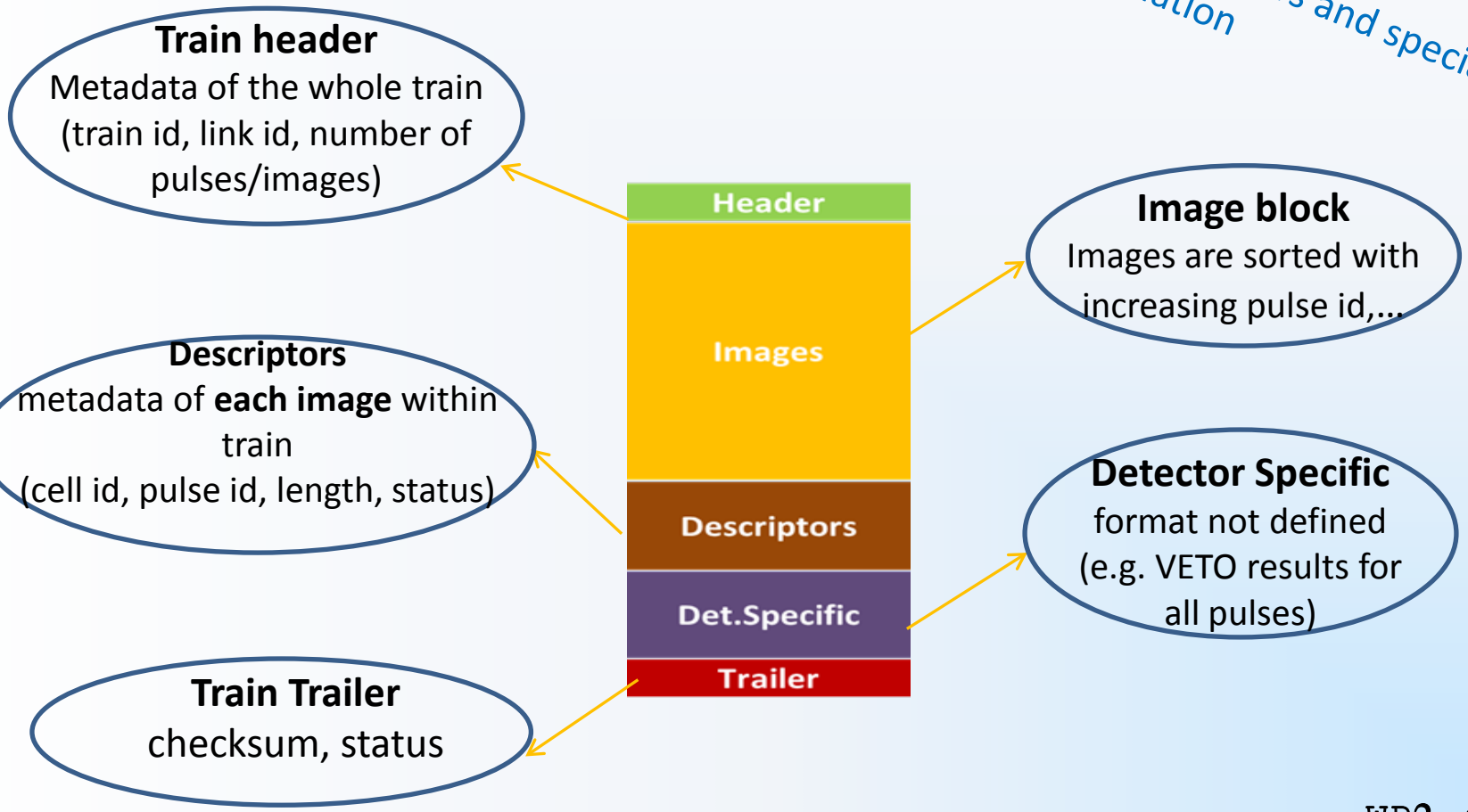
Lower priority than getting the full chain running



# 10GE Packet Format(TTP) and Train Format (XFEL)

- Train Format: **five** data blocks in the train
- Applied to AGIPD, LPD, DSSC

Starting with image data adding with time the descriptors and special information

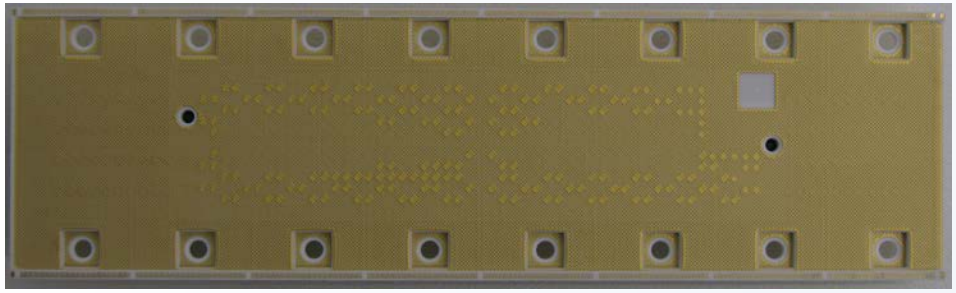


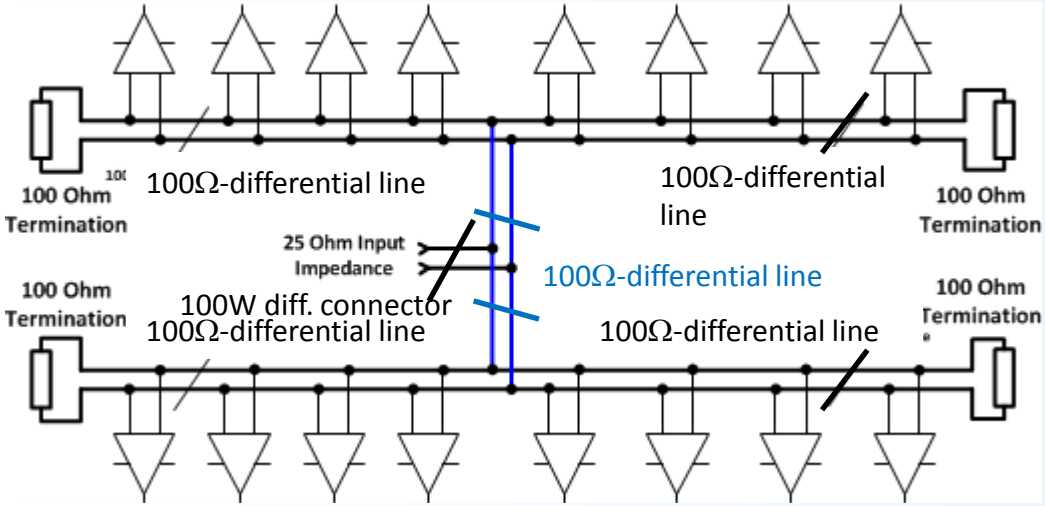
# FPGA Firmware : Development plan

- Short term
  - 1M/Quadrant firmware test with Quadrant setup
  - Automatic reliable IO-Delay (ADC, ASIC, FPGA) configuration (64 channels x 16 for 1M)
  - Further test of pixel descrambling (FW & SW)
  - Speedup readout → Integration of 10GE readout module
- Mid term
  - Table build-up for bunch-keep and reject.
  - Communication with uC board (tasks, I2C/SPI interface,..)
  - Gain bits reduction to 2 Bits (three Gains + error state)

# The Bus Structure of the Sensor-Board



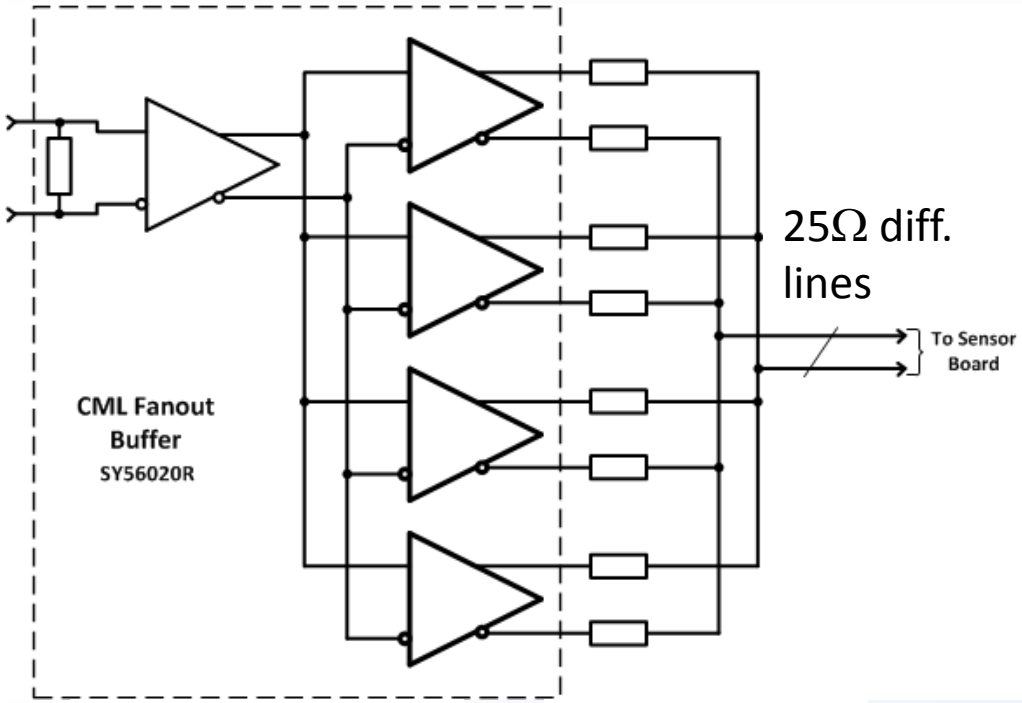





- Three H-Shaped differential Multi-drop-Buses on Sensor-Board minimise propagation time of the signals, but causes signal reflections
- All Lines have 100Ω impedance and are terminated with 100Ω resistor
- Connection of four 100Ω branches gives 25Ω input impedance
- Four Receivers on each branch

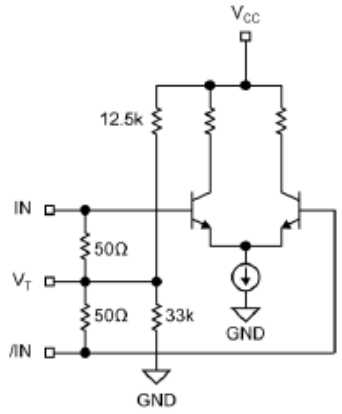
# CML-Drivers on Vacuum Board



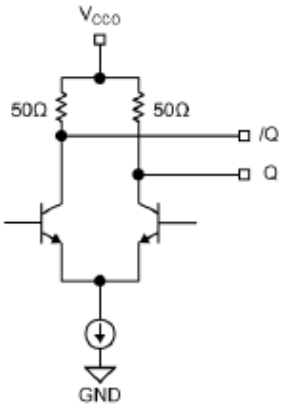



- Solution with four CML Output Buffer matches 25 Ohm Impedance
- 25 Ohm diff.-lines on the Vacuum Board connecting CML Buffer to the Sensor Board
- Usage of CML Buffer reaches suitable common mode voltage for AGIPD ASICs

Choice of driver voltage VCCO defines the common mode of signal.
Tested to get stable operation of ASIC's with low VCCO and differential termination




Simplified Differential Input Buffer




Simplified CML Output Buffer

# Signal Integrity

Workpackage WP2.3

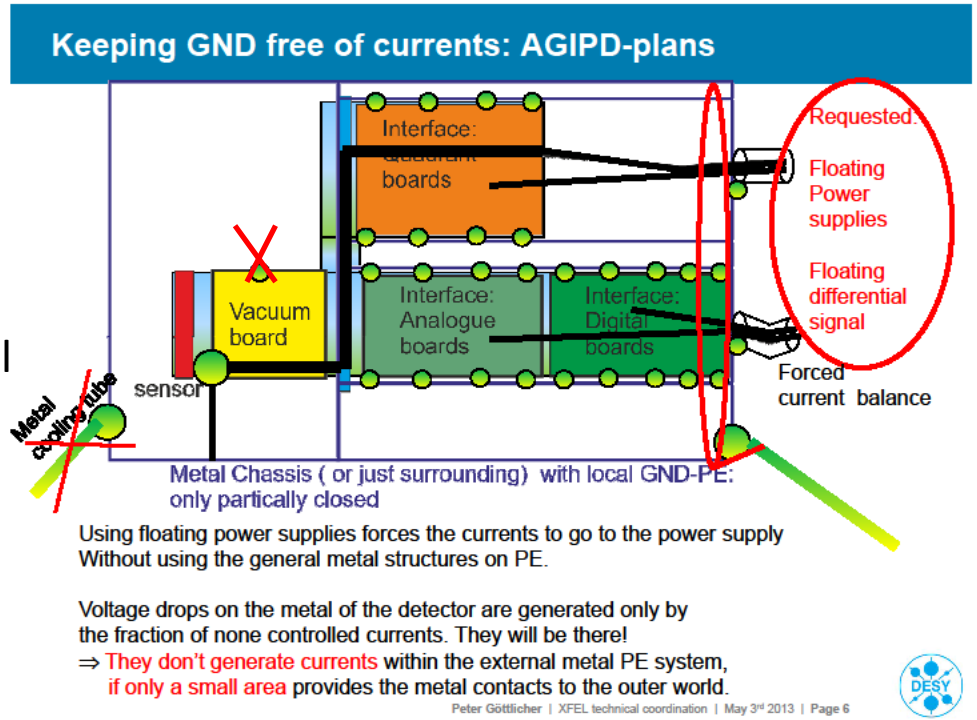

- All signals were measured using differential probes
- Cyan: Signal measured at the ASIC input on the sensor board
- Green: CML buffer output
- Magenta: CML buffer input

16 new vacuum boards are in production

# WP2.3: Impact to others

**The auxiliary power of Vacuum board has increase from few 10mA to ~ 800mA**

- No more able to power from WP2.4
- Additional power lines from external system (XFEL)
- Additional space on vacuum flange




**Compromise:**

- Take the vacuum boards as groups of four. (quadrants)
- Tolerate increase in compensation currents in metal structure, signal shields and GND lines.

# Summary

- -All necessary boards for 1 Mega-Pixel are ordered
  Most are available including spares (small on site test stands)
  - Under investigation how many additional boards are needed for test stands and single modules.
  - Faults have been correctable, but get into layouts before reproduction.

Steps:

- micro-controller: Concentrate on needs for ASIC-boot
  Power-up can be set to always ON, but no watch
- FPGA: Will concentrate of code for operation of ASIC,ADC to PC.
  Fast followed by train-builder and basic clock&control connection with lower priority.