open issues

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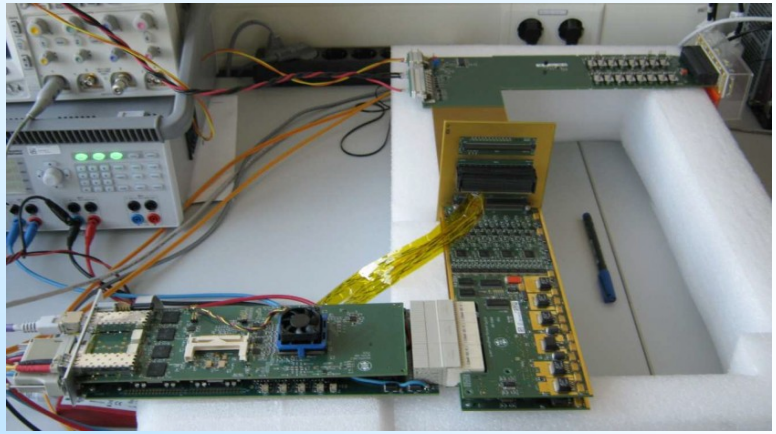
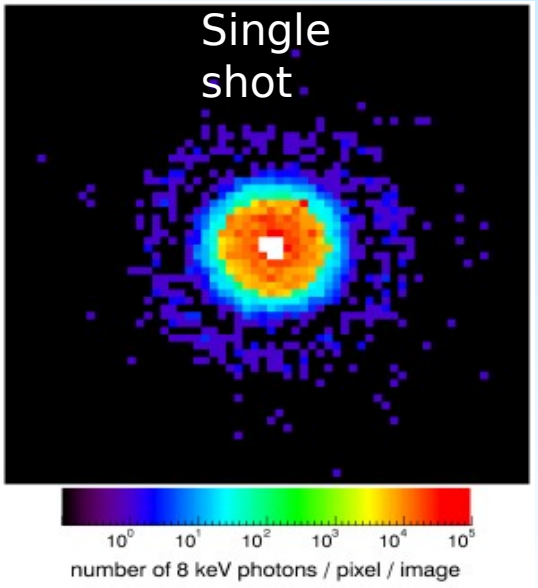
AGIPD 1.0 meeting 01.04.14

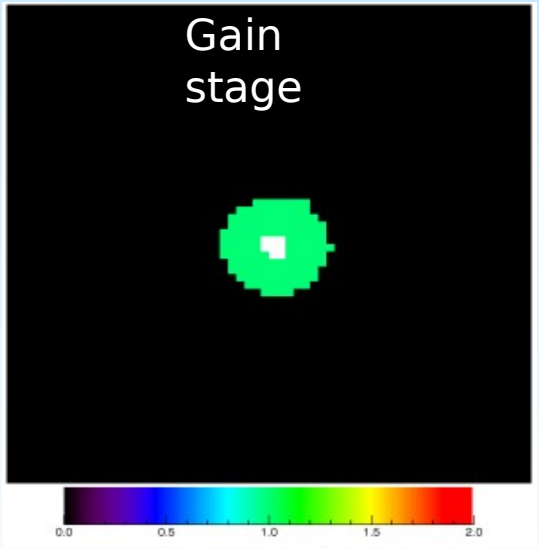
status

Test on single chip assembly performed at P10 12/13.1.14

full module system with proper readout assembled, under test







however, there are some issue that have to be understood (and improved)

open issues

Issue	*Potential impact*	*Comment*	*A real issue? Fixable in resubmit?*
Output drivers have different delays	Output sampling would be slower than planned	droop could worsen if slow outputs	Investigated / understood fixable by respin (1 mask) or redesign
bias/DAC setting vary noticeably from chip to chip	N/A	trivial mistake in testing:non-issue	Not an issue
Truncated last line	None, corrected by reading a dummy line	Essentially a non-issue.	Not an issue

open issues: output delays

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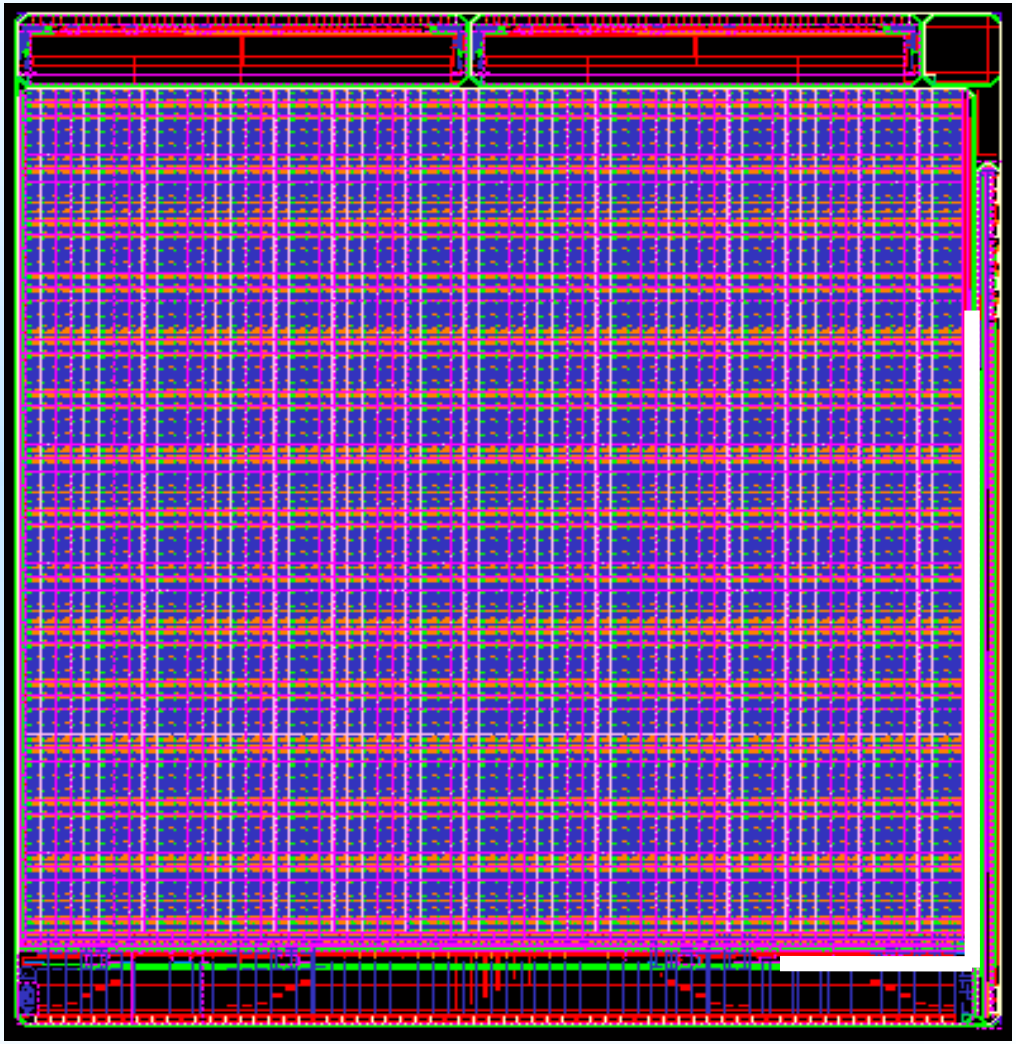
output delays

observed: output signals coming from different ”quarters” of the chip have different delays.
Slowest ones need a readout rate slower than expected

attributed to: capacitance of the (long) lines is too big for the colbuffer to drive them in the expected times

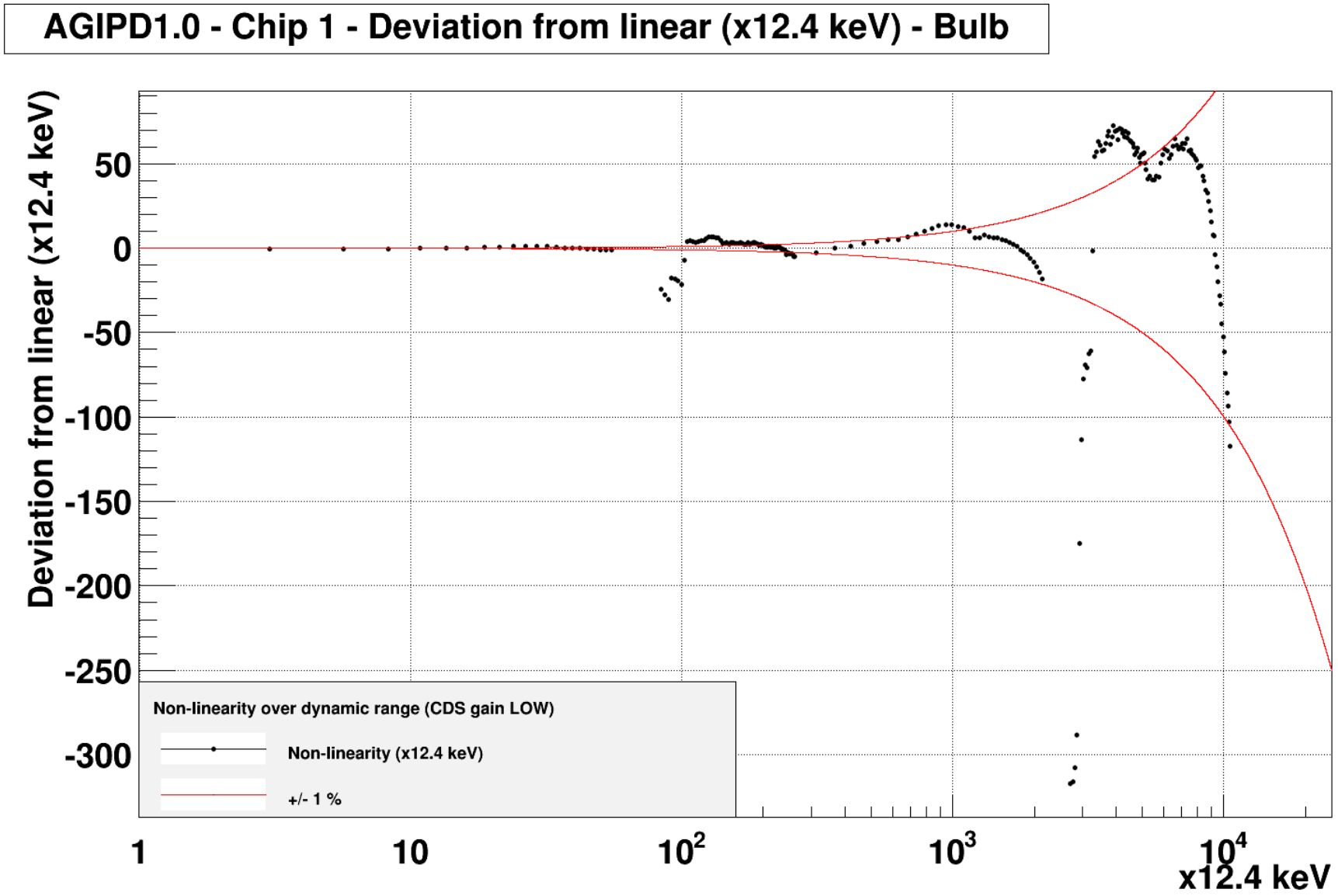
several possible fixes have been identified
1) reduce capacitance load of lines by resizing them. This would be the cheaper (1 mask respin) but the least effective solution
2) increase driving power of colbuf
3) relocate mux (shorten path of fast signals)



open issues: deviation from linearity

Issue	*Potential impact*	*Comment*	*Is it a real issue? Fixable in resubmit?*
deviations from linearity just before gain switching	potentially avoidable by earlier switching	optimal bias & switching ponts points are being measured (former presentation)	under investigation
deviations from linearity just after gain switching	Medium-high. Most pixels: small monoton. deviations, but non-monotonous responses were observed		under investigation

deviation from linearity

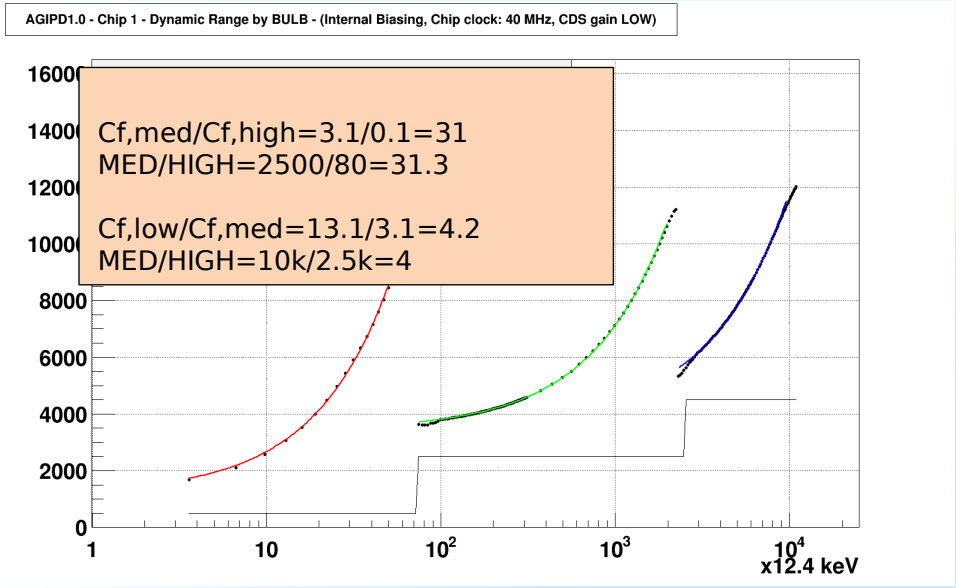


open issues: test current source

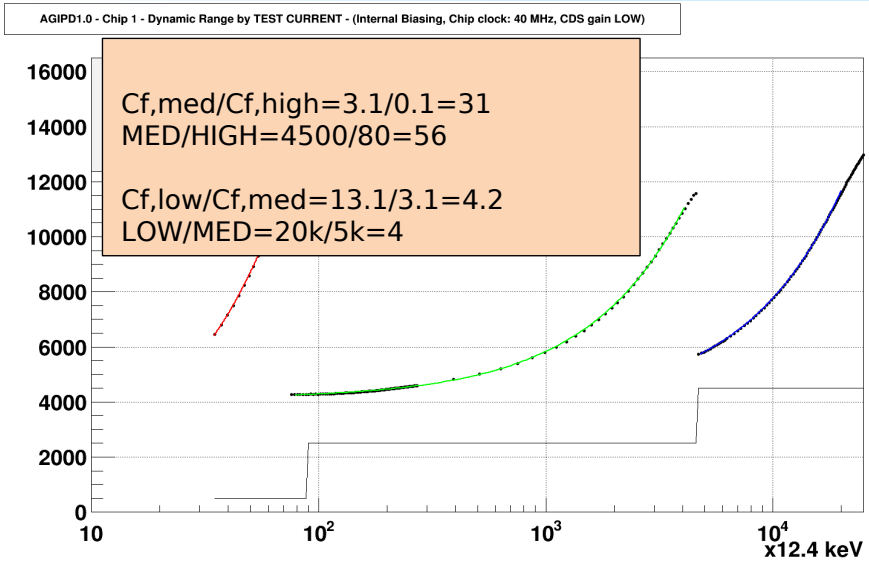
Issue	*Potential impact*	*Comment*	*A real issue? Fixable in resubmit?*
Non- monoton. response vs input value	limit CS use to fixed current / integration time		under investigation
anomalous current variation between high an medium gain	limit CS use to Med/Low gains (as planned)		probably fixable (cross-coupling in layout)
Current source: systematics of memcell row 3	would require ad hoc cross-calibration for this memcell row		probably fixable (cross-coupling in layout)

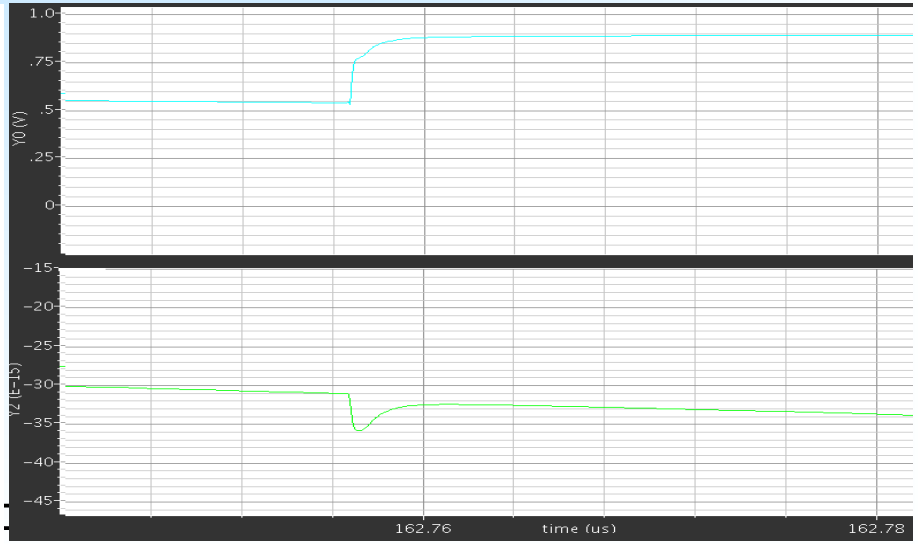
it remains to be seen if the current source (as is now) can be used for calibration

test current source

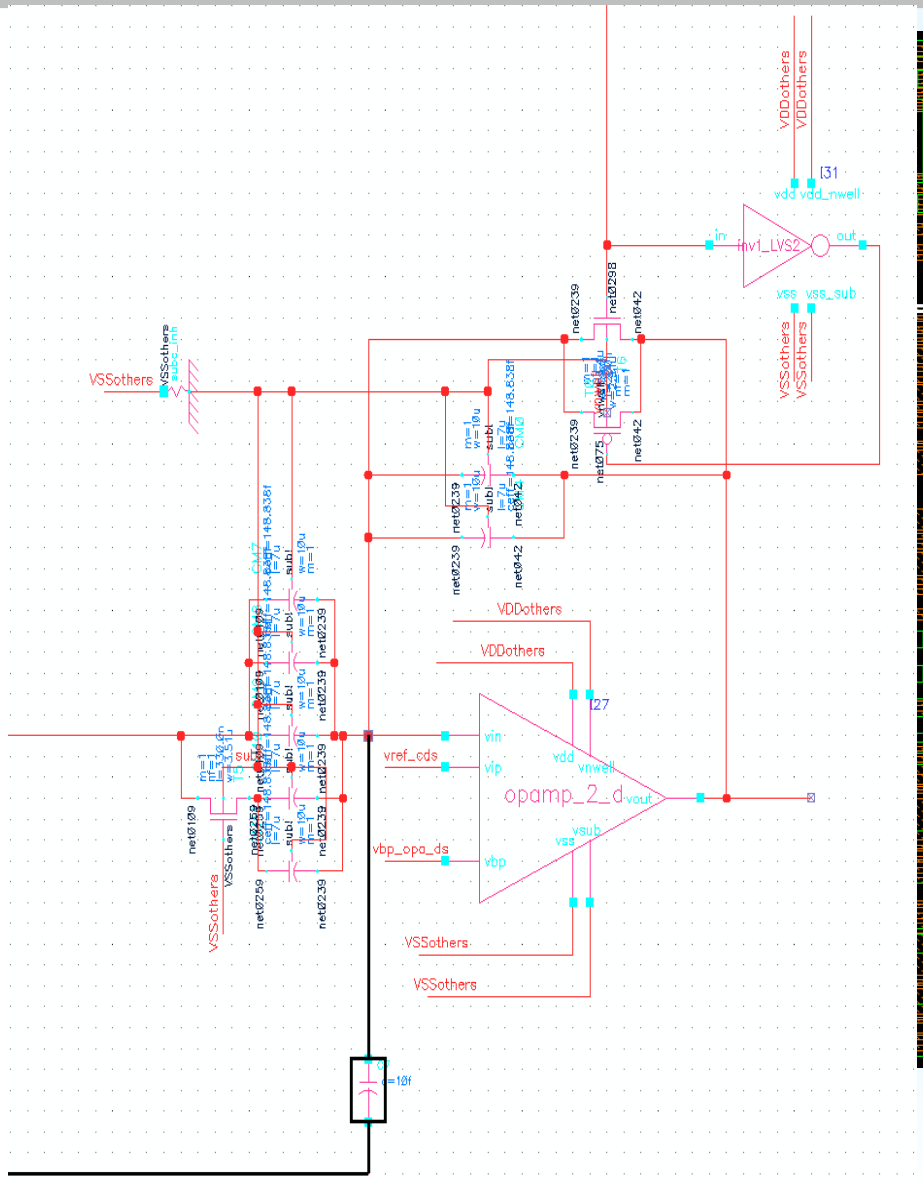


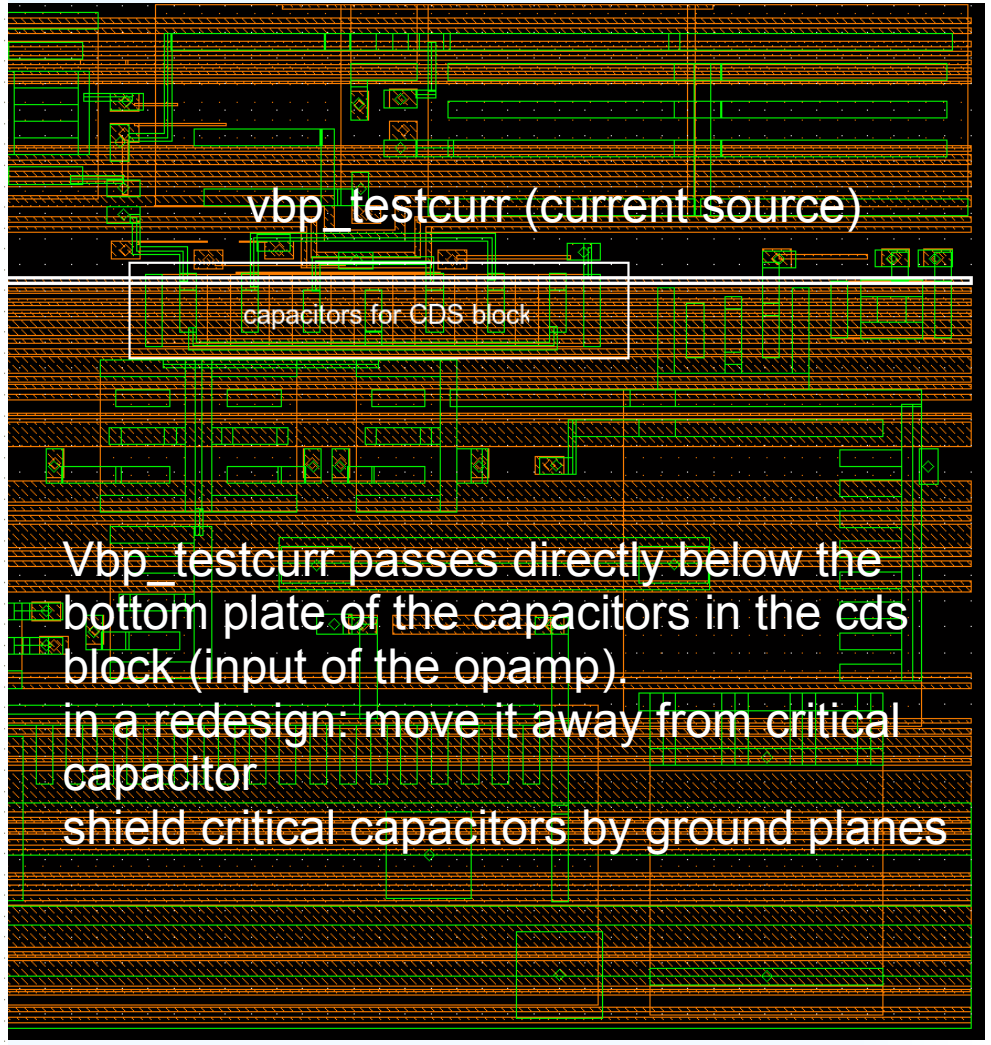
There seems to be an anomalous current variation between high and medium gain.
The current erogated by the current source is the same between medium and low gain, but it is different between high and medium gain.
The variation observed is roughly by a factor of 2; simulations predict a variation much less relevant than that





test current source





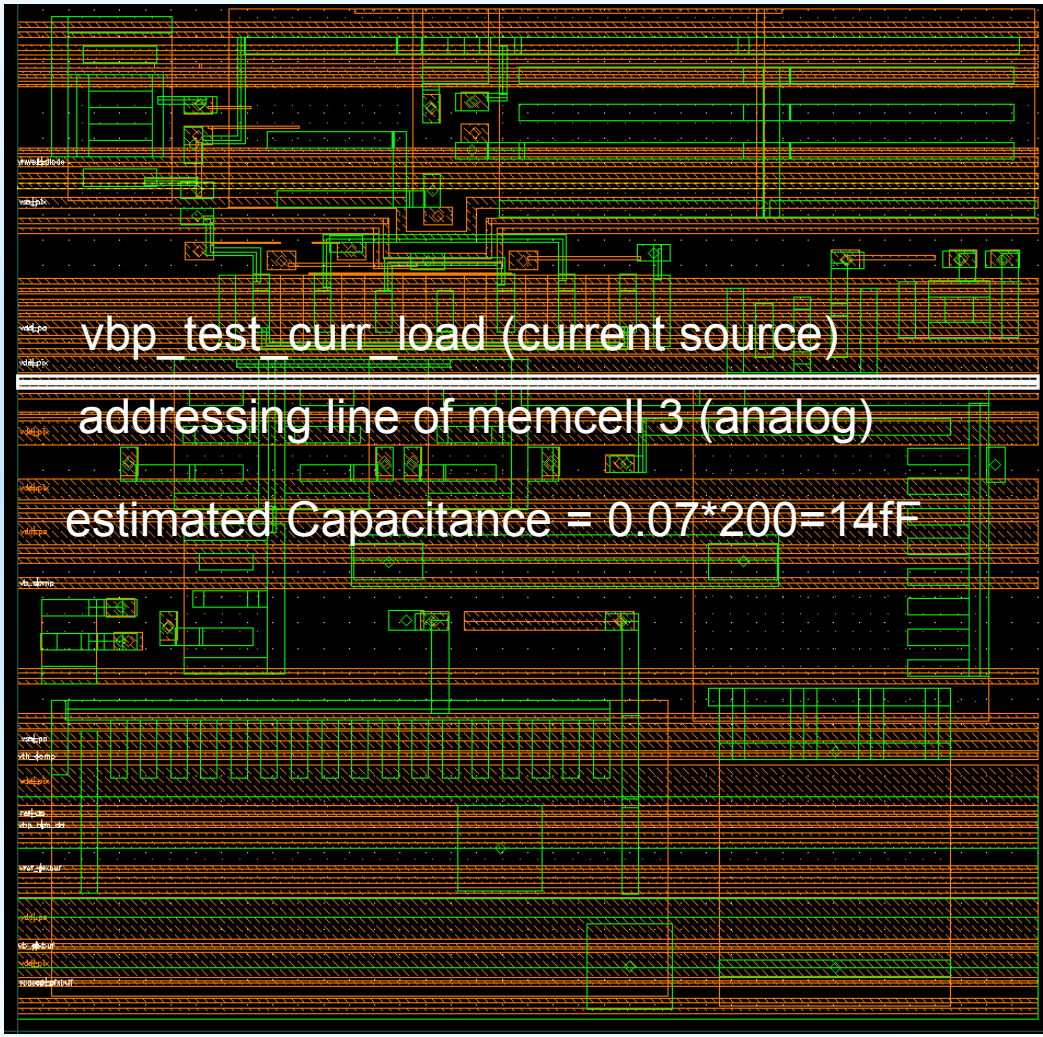
AGIPD 10 pixel layout

et al.

test current source

digital line (addressing the memcell row) is adjacent to the analog voltage line determining the current level → likely crosstalk

need further investigation and testings with the proper biasing& timings

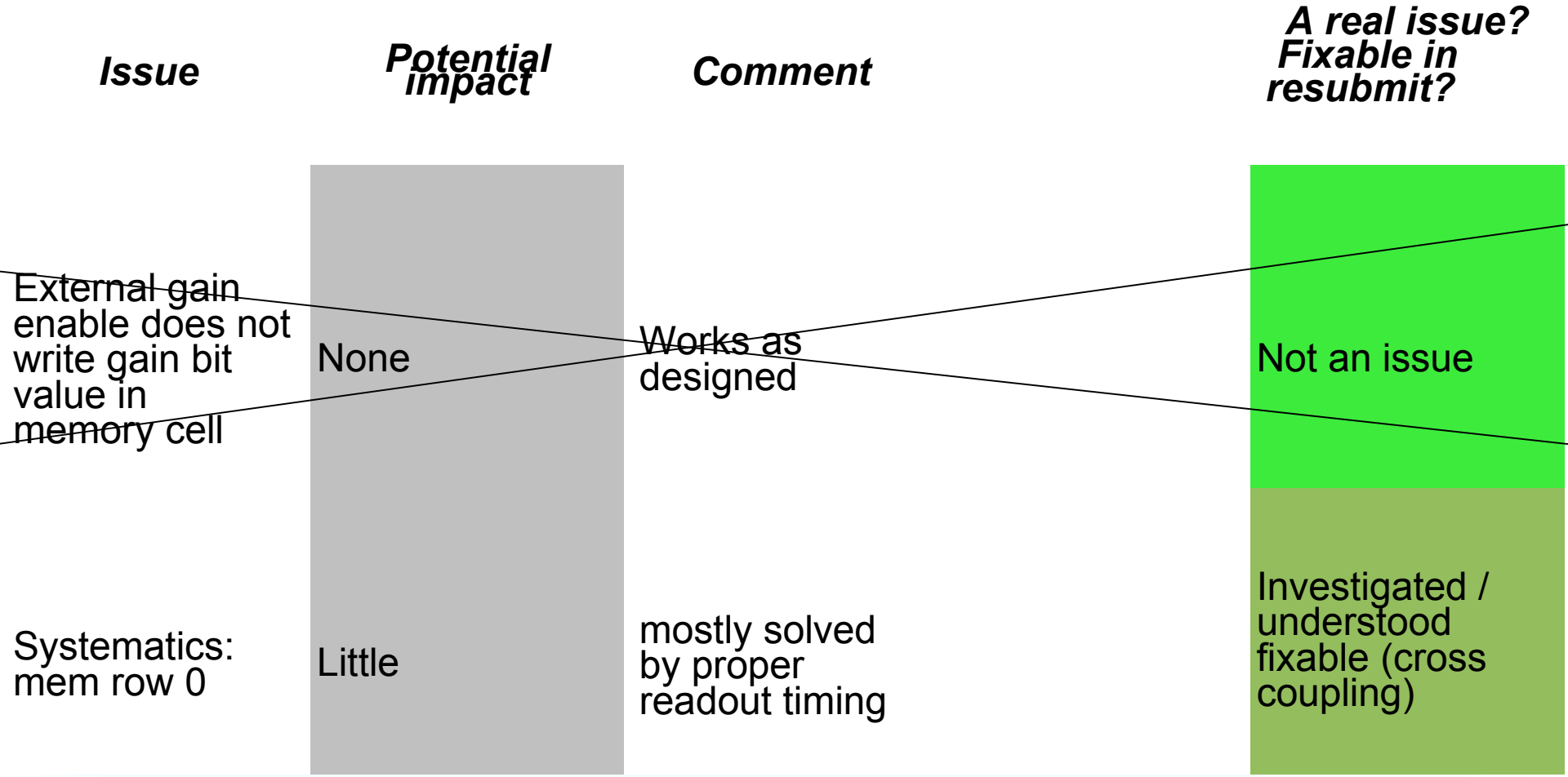


AGIPD 10 pixel layout

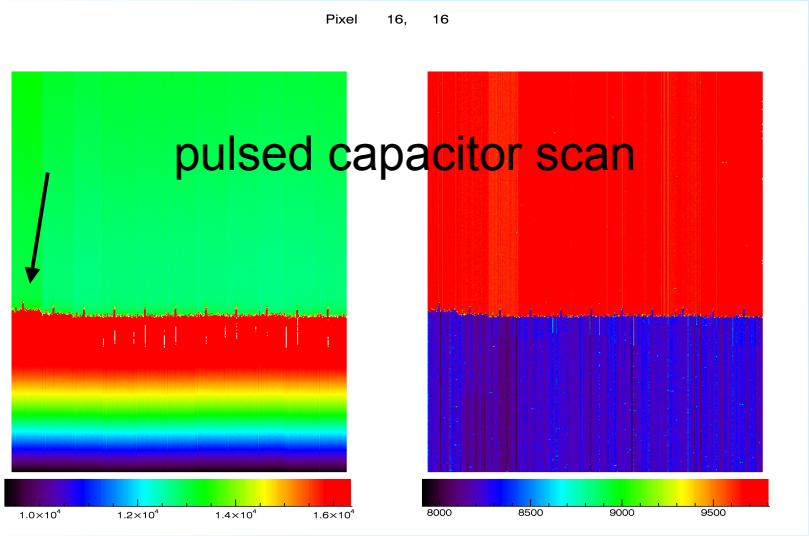
open issues

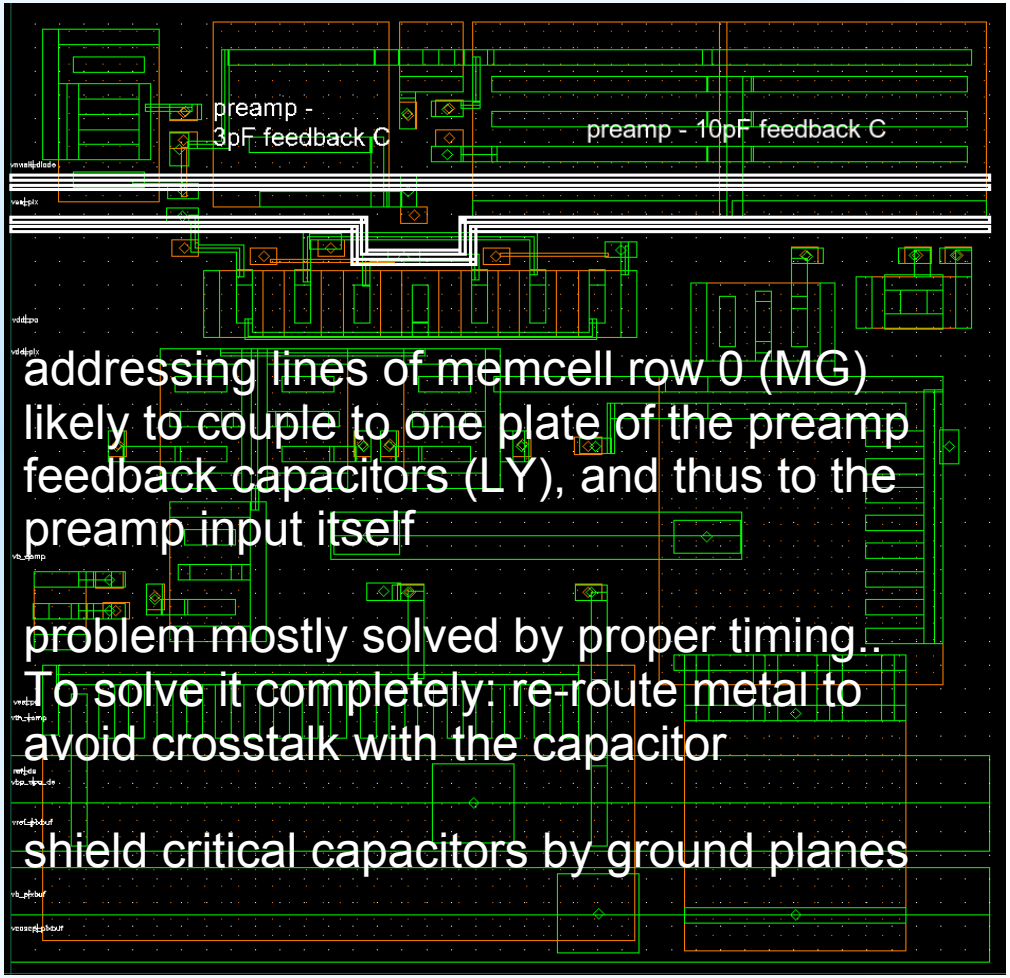
Issue	*Potential impact*	*Comment*	*A real issue? Fixable in resubmit?*
External gain enable does not writes gain bit value in memory cell	None	Works as designed	Not an issue
Systematics: mem row 0	Little	mostly solved by proper readout timing	Investigated / understood fixable (cross coupling)

open issues: memcell systematics



memcell systematics





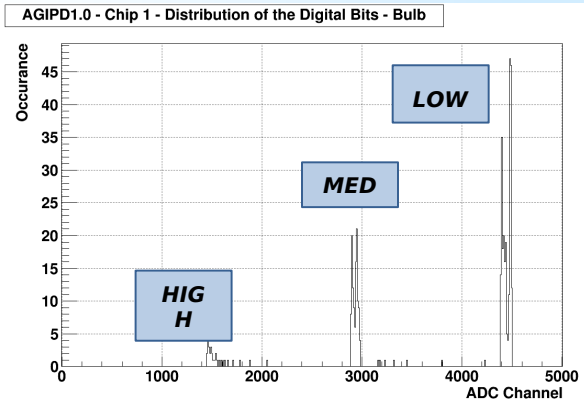
AGIPD 10 pixel layout

open issues: digital bits

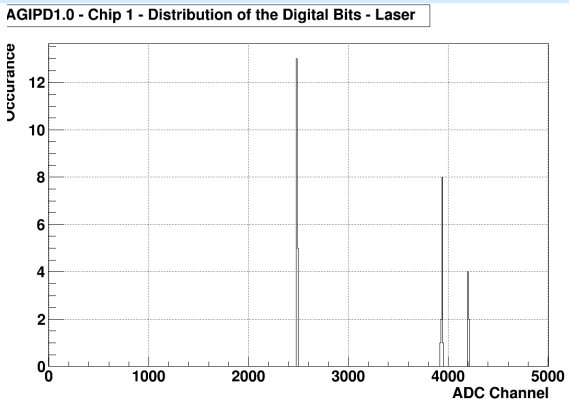
Issue	*Potential impact*	*Comment*	*A real issue? Fixable in resubmit?*
analog-encoded digital values: for some cells are separated by less ADU than their respective noise	Medium, the affected storage cells cannot store digital information reliably, so far 3/4096 ~0.1 % were observed	Might be a yield related problem; measured with not-optimal voltages	under investigation
analog-encoded digital values: somewhat depending on the signal source	Medium-high., affected storage cells cannot store digital information reliably		under investigation

open issues: digital bits

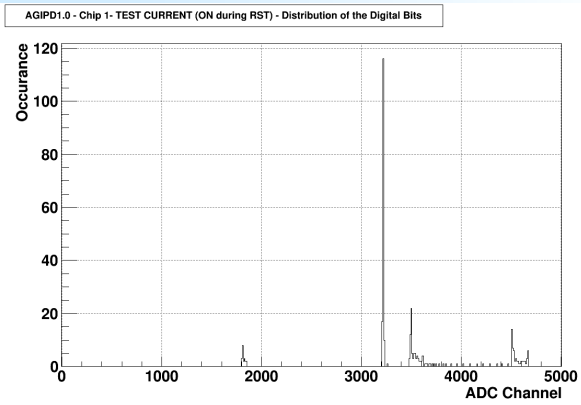
Bulb



Laser



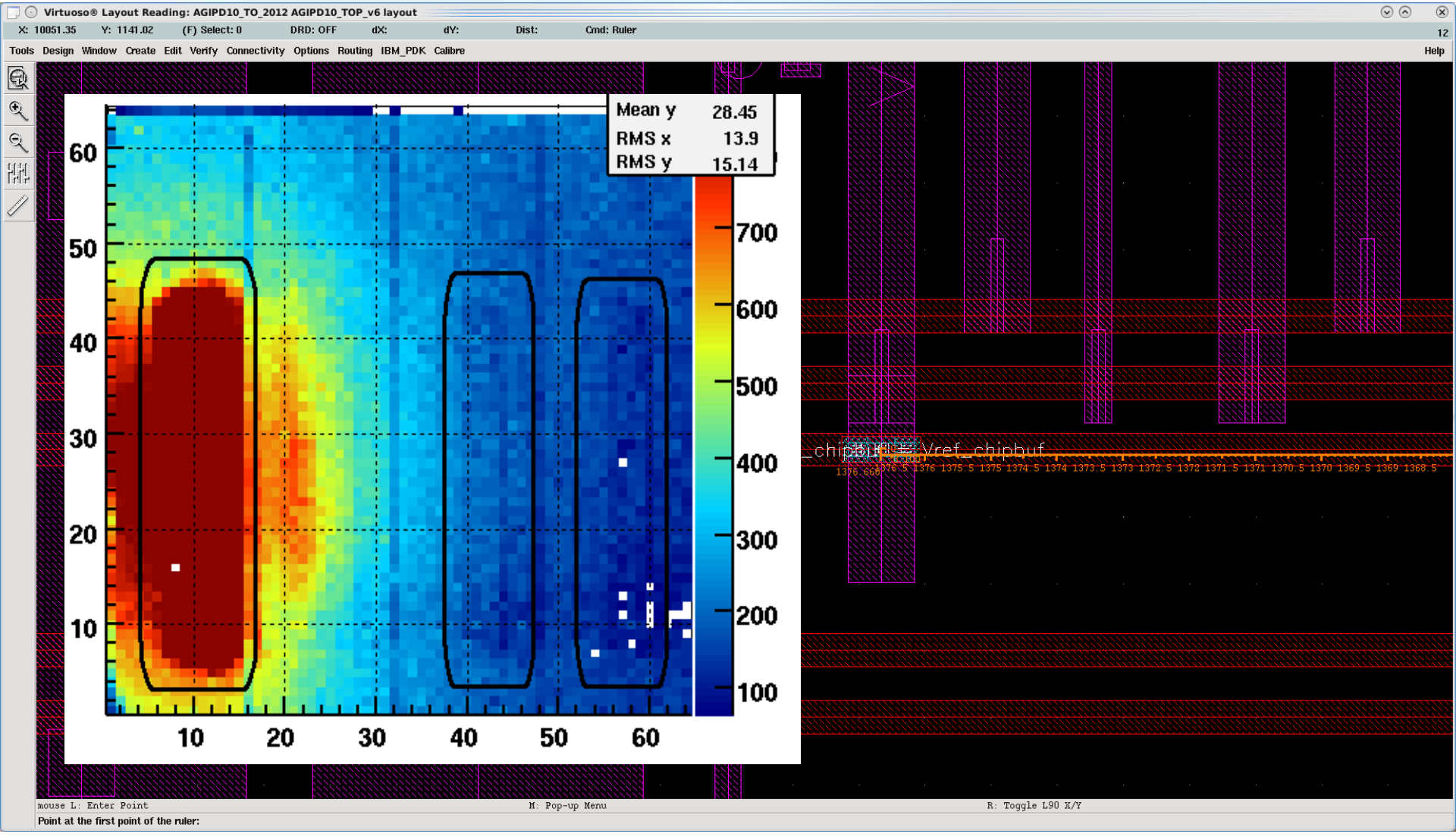
Test current



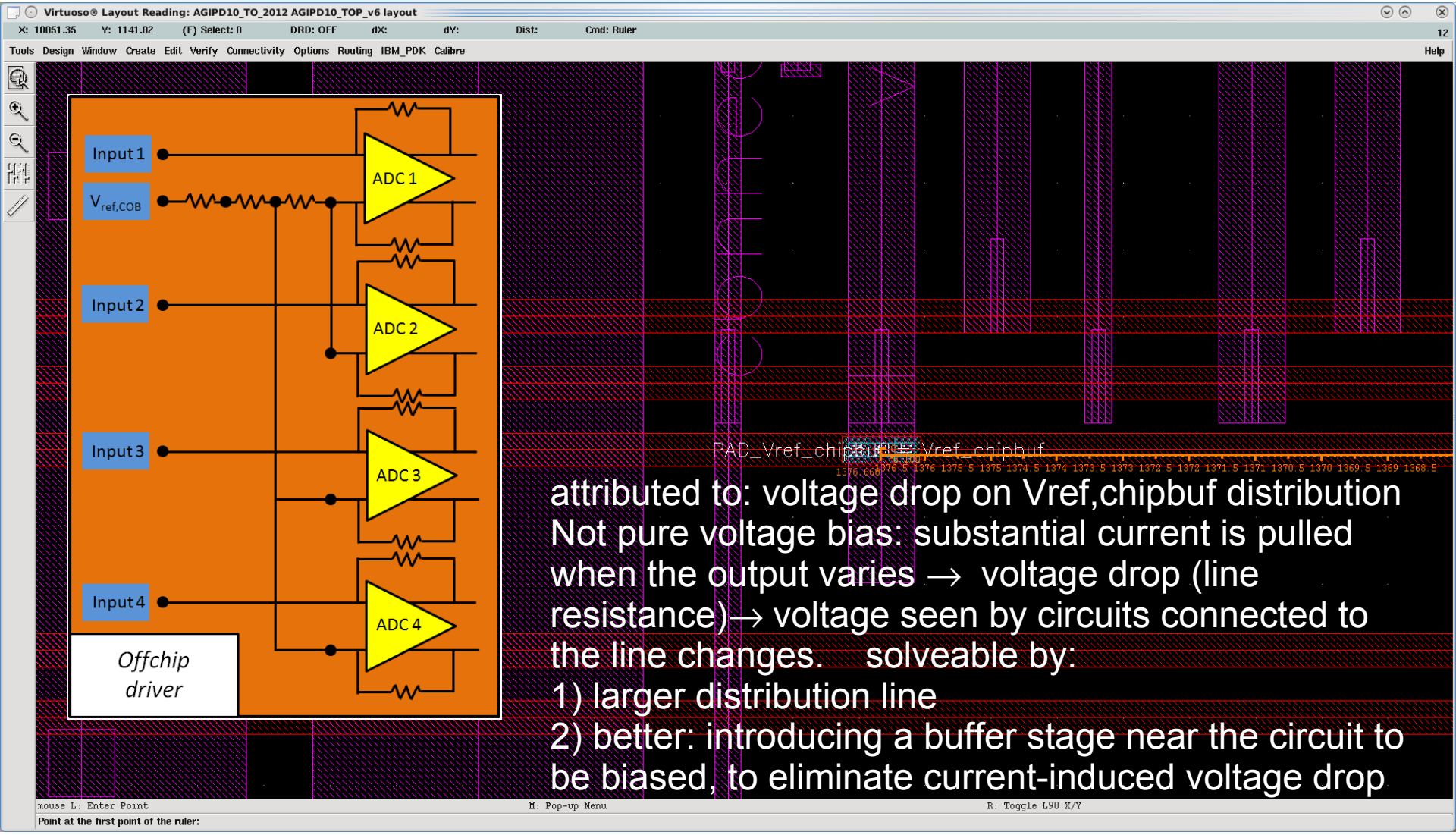
open issues: output cross talks

Issue	*Potential impact*	*Comment*	*A real issue? Fixable in resubmit?*
Sometimes positive spikes are observed on the first pixel read and negative spikes on all others	Depends on reason for this cross talk. avoidable by proper sampling	This is probably a chiptester box timing problem coupled with non-optimal DAC settings	Initial observation probably
Cross talk between outputs	Severe/none, would require fix or additional corrections in the data evaluation chain	voltage drop on a bias distribution line	Investigated/ understood fixable

Cross talk between outputs



Cross talk between outputs



attributed to: voltage drop on Vref,chipbuf distribution
Not pure voltage bias: substantial current is pulled when the output varies → voltage drop (line resistance)→ voltage seen by circuits connected to the line changes. solveable by:
1) larger distribution line
2) better: introducing a buffer stage near the circuit to be biased, to eliminate current-induced voltage drop

What we are achieving