AGIPD Software/Firmware Development

- **Test Bench Set-Up**

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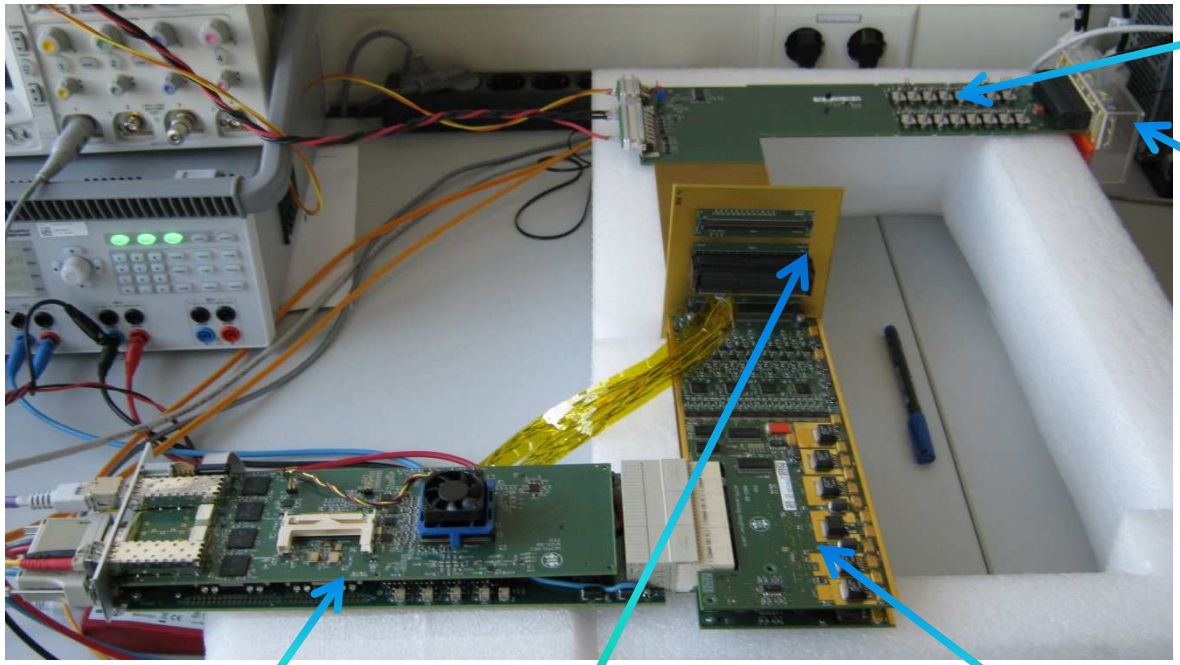
DESY Hamburg, 15 Oct, 2013

DESY

Outline

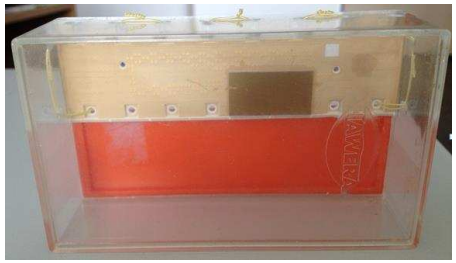
- Test bench hardware set-up
- Software/FPGA firmware development
  - Concept
  - Software: Command editor
  - FPGA firmware
- Summary and Outlook

Test Bench Hardware Set-Up



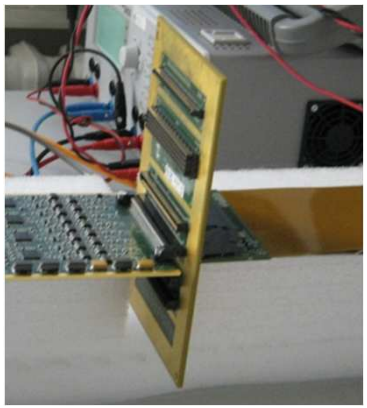
Vacuum board

ASICs ceramic board



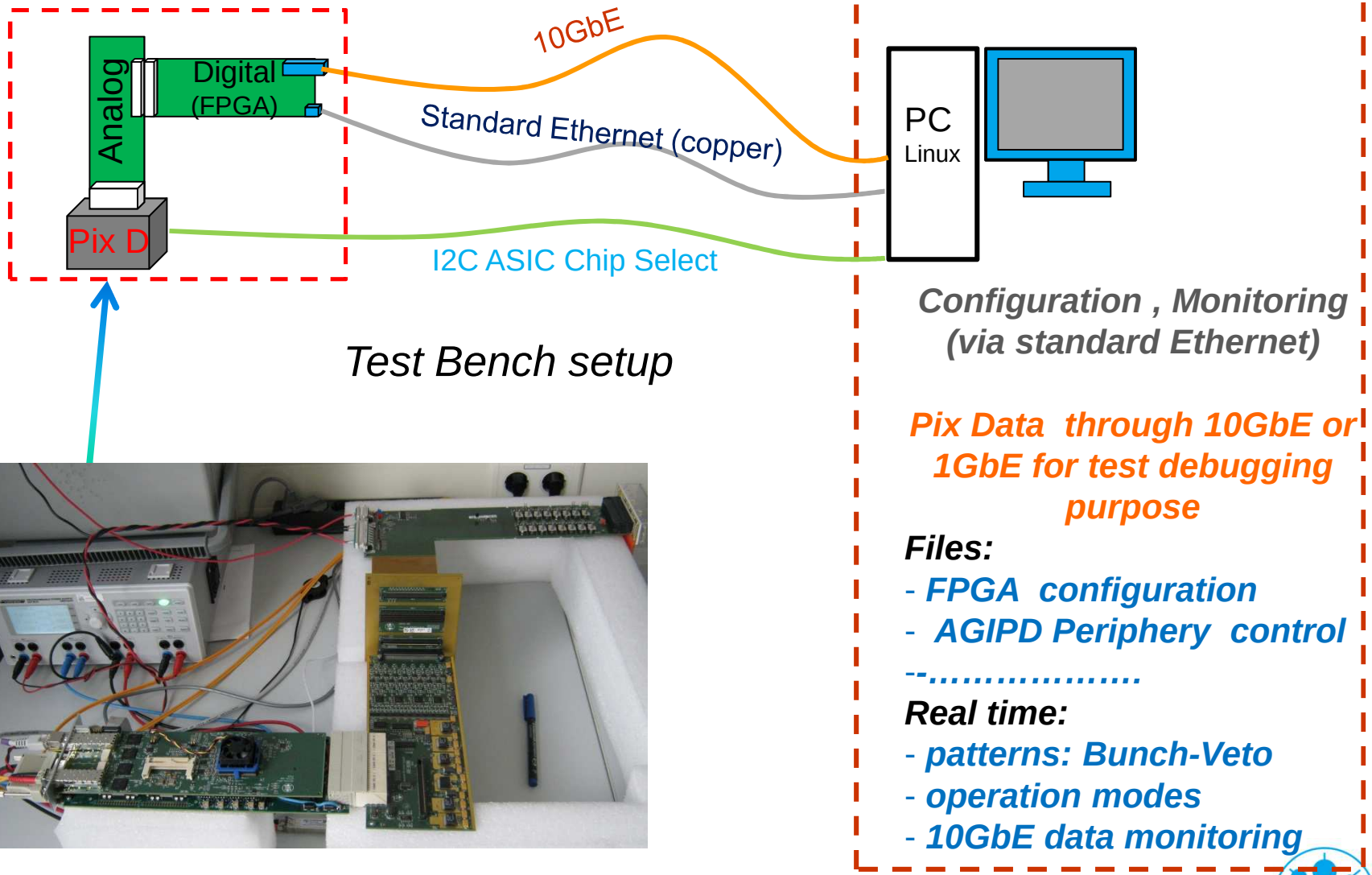
Digital read out

Backplane



Analogue boards

AGIPD Firmware/Software Development: Basic Concept

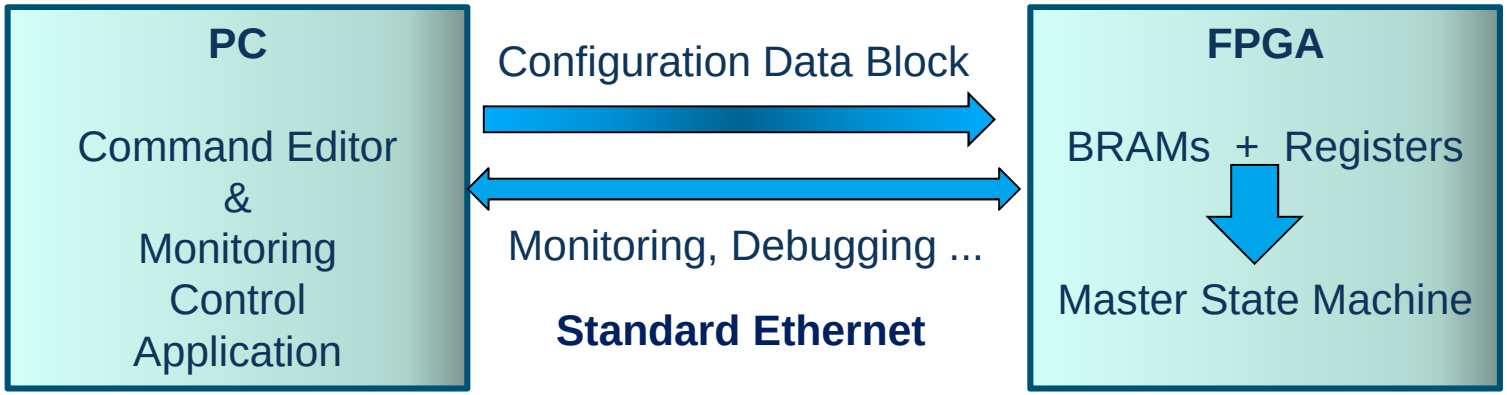


AGIPD Firmware/Software Development: Approach

- Parameterization of firmware operation
  - No need recompiling the VHDL code for every new mode of operation
  - No new VHDL compilation =>no need readjustment of timing, mapping,…..

AGIPD 1.0 Command Set

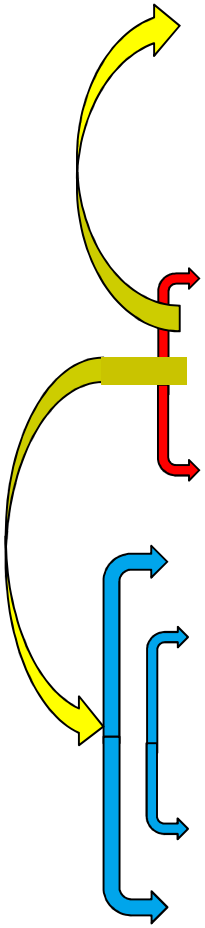
Memnonic	Bit pattern	Description	Arguments
SETMEM	1000000AAAAAAAAA	Set memory address	AAAAAAAAA = Memory address
ACQMEM	1000001AAAAAAAAA	Acquire image	AAAAAAAAA = Memory address
RPAMPN	1010PPPPPPMMMMMM	(Pre-)Read analogue pixel row, no multiplexing	PPPPPP = (Pre-)Read pixel row no multiplexing MMMMMM = Multiplexed pixel row
…….	……	…….	……..
SWCALV	01101111VVVVVVVV	Register 31 (calibration and LVDS bias switch)	VVVVVVVV = Register value



AGIPD Software Development: Concept

- Command Interpreter for test bench setup FE

~ 63 AGIPD Commands
+ several like:
Loop
Delay
Trigger (~if)
…….
and execution statement
exec x, y

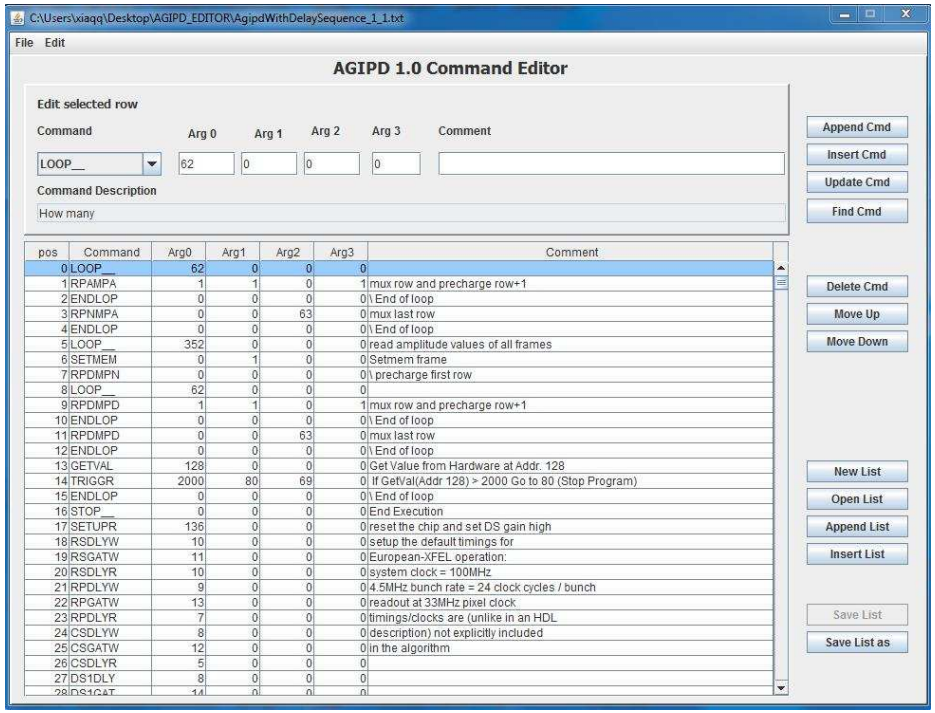


```
0
1
--
20  init_cmd_1  vvvvv, vvvvv      // initialization
21  --
22  init_cmd_N  vvvvv             // initialization
23  -----
24  register    vvvvv             // variable
25  register    vvvvv             // variable
26  -----
27  main
28  exec  20 22          // execute from 20 to 22
29  exec  33 43          // execute from 33 to 43
30  --
31  end
32  --
33  loop  43  vvvvv               // comments
34  trigger   vvvvv, reg 24       // comments
35  loop 41   vvvvv               // comments
36  cmd vvvvv, reg 25 , …..       // comments
37  delay vvvvv                   // comments
38  ----
41  Cmd  reg 25, +1, vvvvv        // comments
42  Out  file_name, vvvv,  ..     // send to write to file
43  ---
```

AGIPD Software Development: GUI Tool

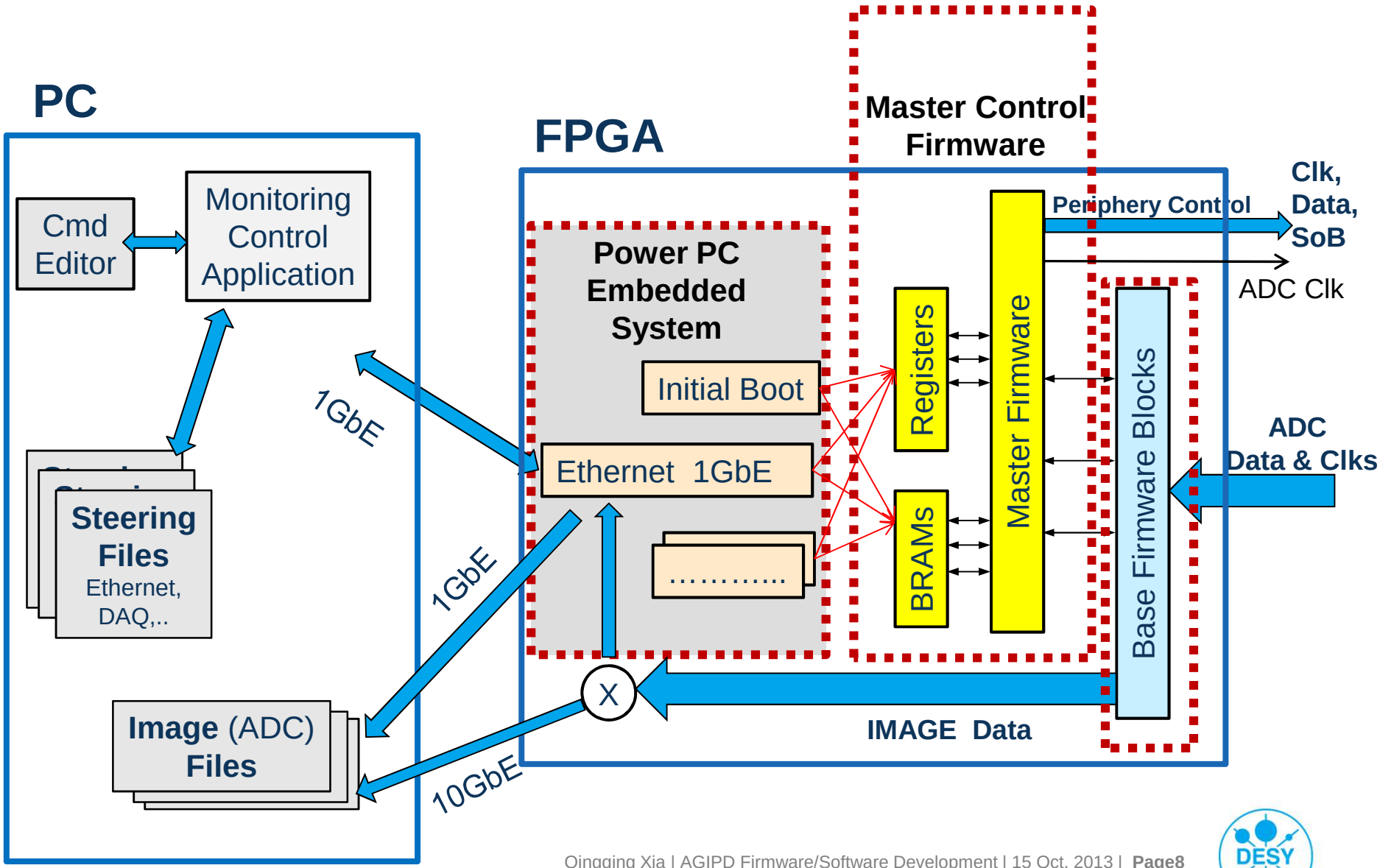
- Java Based Command Editor
  - Create validated commands
  - Create a command sequence
  - Operation System independent
  - Input and Output of Command Tables in FPGA Format stored as normal ASCII Files

For test bench purpose only!



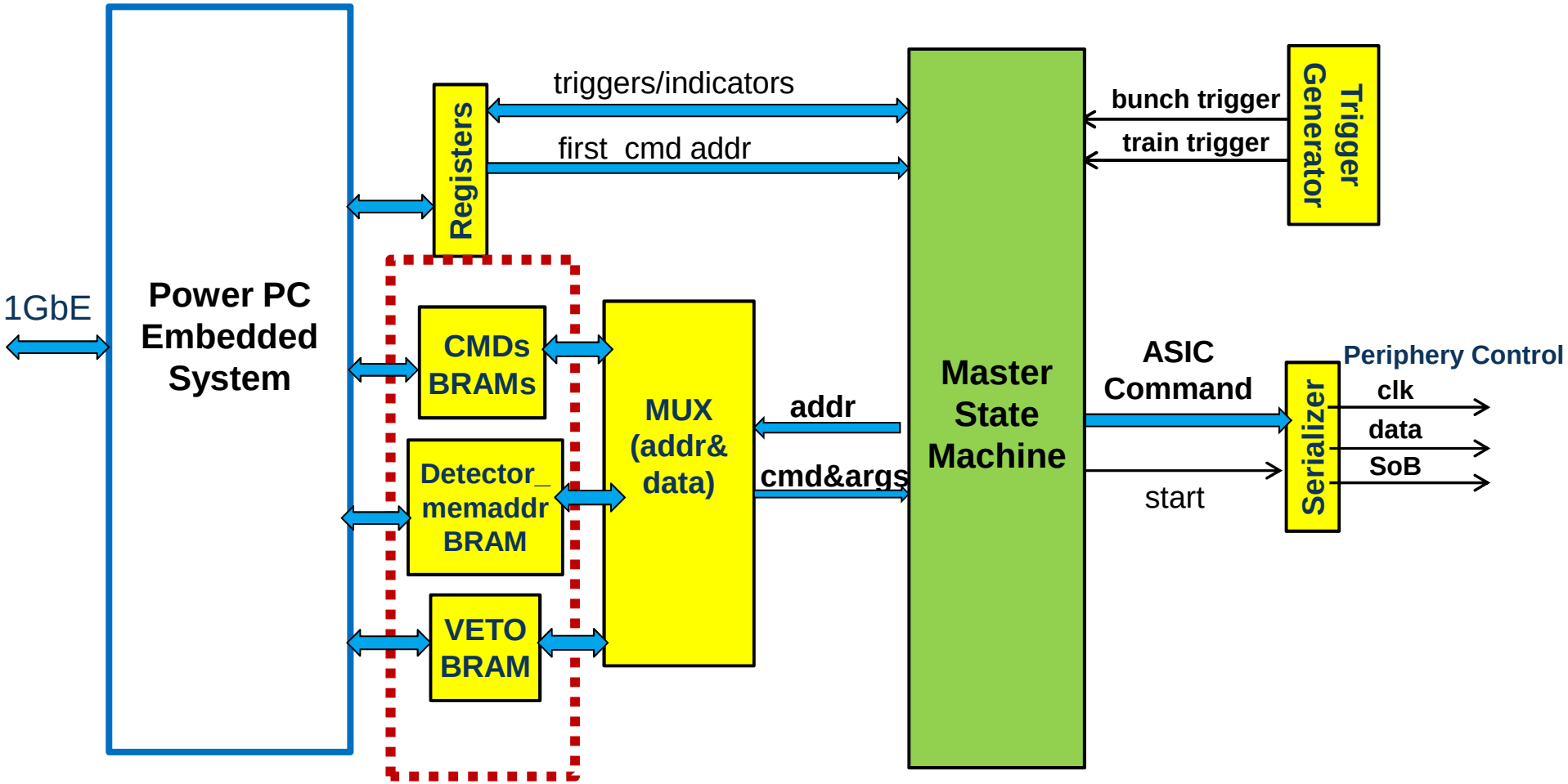

```
0,SETUPR,136,0,0,0,reset the chip and set DS gain high
1,RSDLYW,10,0,0,0,setup the default timings for
2,RSGATW,11,0,0,0,European-XFEL operation:
3,RSDLYR,10,0,0,0,system clock = 100MHz
4,RPDLYW,9,0,0,0,4.5MHz bunch rate = 24 clock cycles / bunch
5,RPGATW,13,0,0,0,readout at 33MHz pixel clock
6,RPDLYR,7,0,0,0,timings/clocks are (unlike in an HDL
7,CSDLYW,8,0,0,0,description) not explicitly included
8,CSGATW,12,0,0,0,in the algorithm
9,CSDLYR,5,0,0,0,
10,DS1DLY,8,0,0,0,
11,DS1GAT,14,0,0,0,
12,RSTDLY,8,0,0,0,
13,RSTGAT,14,0,0,0,
14,G1SDLY,5,0,0,0,
15,G1SGAT,17,0,0,0,
16,G2SDLY,6,0,0,0,
17,G2SGAT,16,0,0,0,
18,EGSDLY,7,0,0,0,
19,EGSGAT,15,0,0,0,
20,PXBDLY,8,0,0,0,
21,TSTDLY,12,0,0,0,for droop loop TSDLY must be bigger that RSTDLY(8)
22,TSTGAT,11,0,0,0,bigger than 10
23,MUXDIV,7,0,0,0,
24,TIROWM,255,0,0,0,
25,TICOLM,255,0,0,0,
26,VRFCDS,0,0,0,0,Biases and voltages are set to
27,IBNPXB,128,0,0,0,default values
28,VRFPXB,167,0,0,0,default values
29,VCAPXB,193,0,0,0,
30,IBPCOL,149,0,0,0,
31,IBNCOB,184,0,0,0,
32,IBPCOB,102,0,0,0,
33,IBNFDA,160,0,0,0,
34,IBNPRB,95,0,0,0,
35,IBPPRB,98,0,0,0,
36,VCMCHB,148,0,0,0,
37,VCACHB,93,0,0,0,
```

AGIPD FPGA Firmware Development: System Diagram



AGIPD FPGA Firmware Development: Master Control

- Master Control Firmware



AGIPD FPGA Firmware Development: Master Control

- Intermediate test results
  - Test bench sequence prepared

Sequence to initialize detector ✓

↓

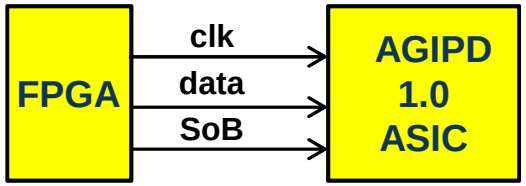
Record frames selectively (predefined VETO results) ✓

↓

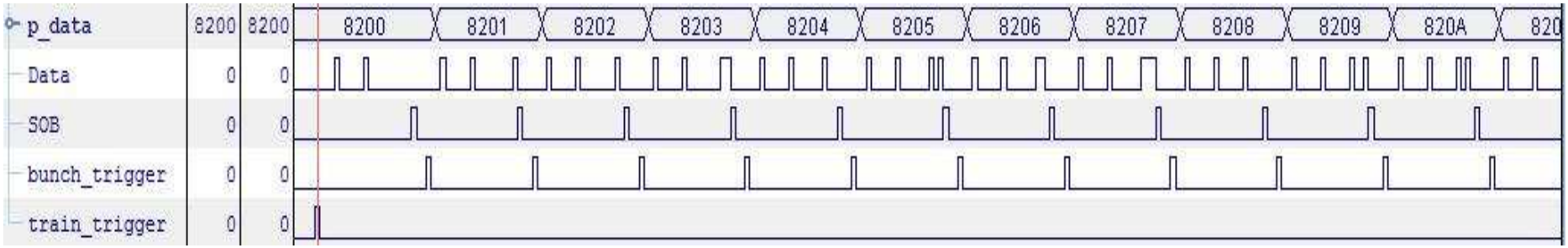
Readout amplitude values of all recorded frames ✓

  - Chipscope-based Hardware Test (without ASIC)
    - PC via Ethernet trigger PowerPC to start initializing Dual Port Block RAM
    - Power PC trigger the master control firmware to start read command sequence from BRAM
    - Master control firmware start sending the command sequence to periphery interface

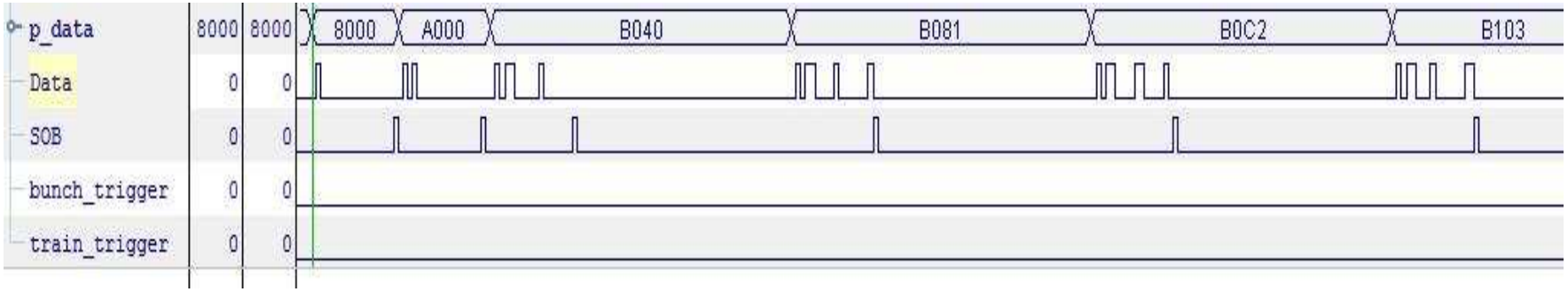
AGIPD FPGA Firmware Development: Master Control



- Examples from Chipscope
  - Record frame: *ACQ_MEM mem_addr =1000001AAAAAAAAA*

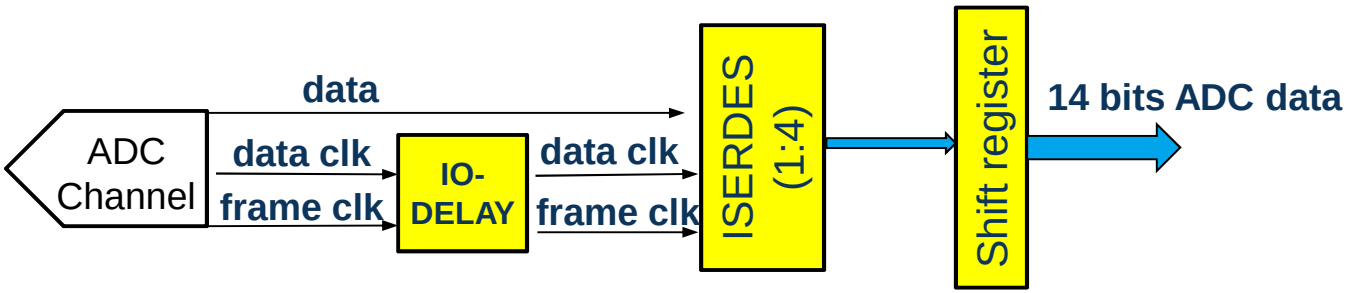


  - *Readout sequence: SETMEM mem_addr, RPAMPN 0 0 , RPAMPA (row+1) row,…*

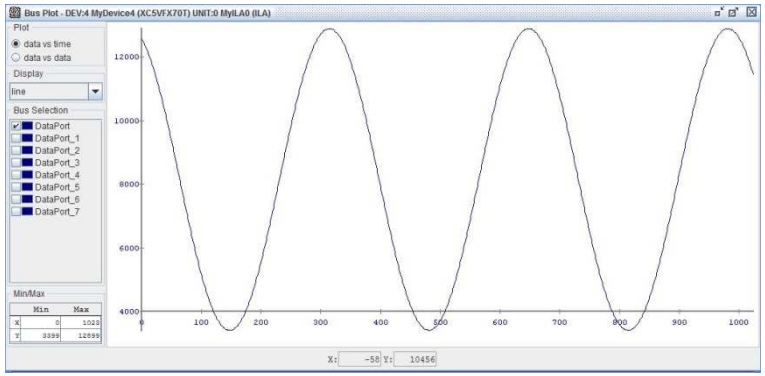


Firmware Development Status: ADC Fast Readout

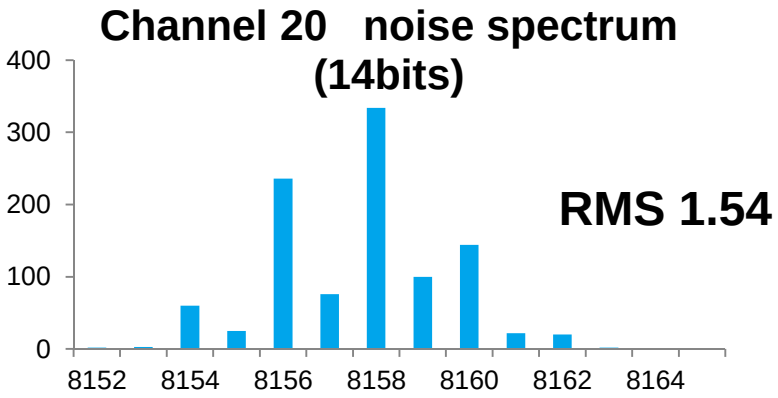
- ADC fast readout in standalone mode
  - Optimized clock delay region for IODELAY inside FPGA for this Test bench Set-Up founded
  - Two different mother ADC boards (32 Channels) work without individual delay adjustment for each board
  - 64 channels parallel ADC readout (mother + daughter boards) succeeded

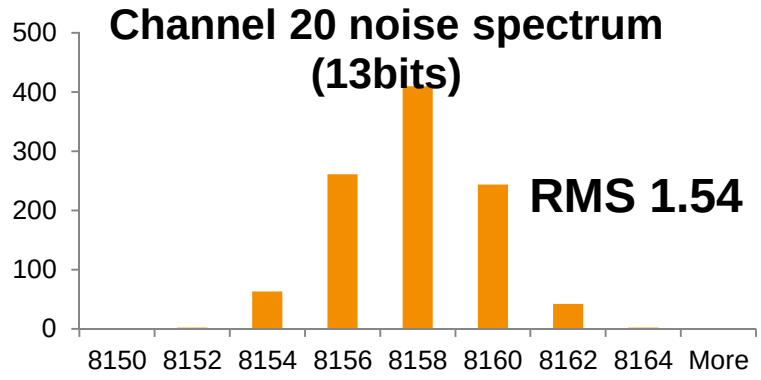


Firmware Development Status: ADC Fast Readout



Digital output of one ADC Channel 0 (analogue sine wave input)





Summary &

Outlook

Summary & Outlook

- PC Software
  - Command Editor: first version is tested by user
  - Further development of application protocol (TCP based) and Interfaces for Monitoring and Control
- FPGA Firmware
  - Parameterization of firmware operation → Dynamic update and execute user algorithm
  - Master control firmware: Simulation and Chipscope-based hardware tested
  - Reliable Power PC Ethernet communication with PC
  - ADC 64 channels read out implemented
  - Further development of ADC readout chain(sync, write to DDR2, Power PC DMA engine, 1GbE/10GbE back to PC)
  - Further development of Power PC System for dynamic configuration and readout control to simplify the transition to micro controller later

Thank you!

AGIPD Software Development: Java Based Command Editor

- Command List

```
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```
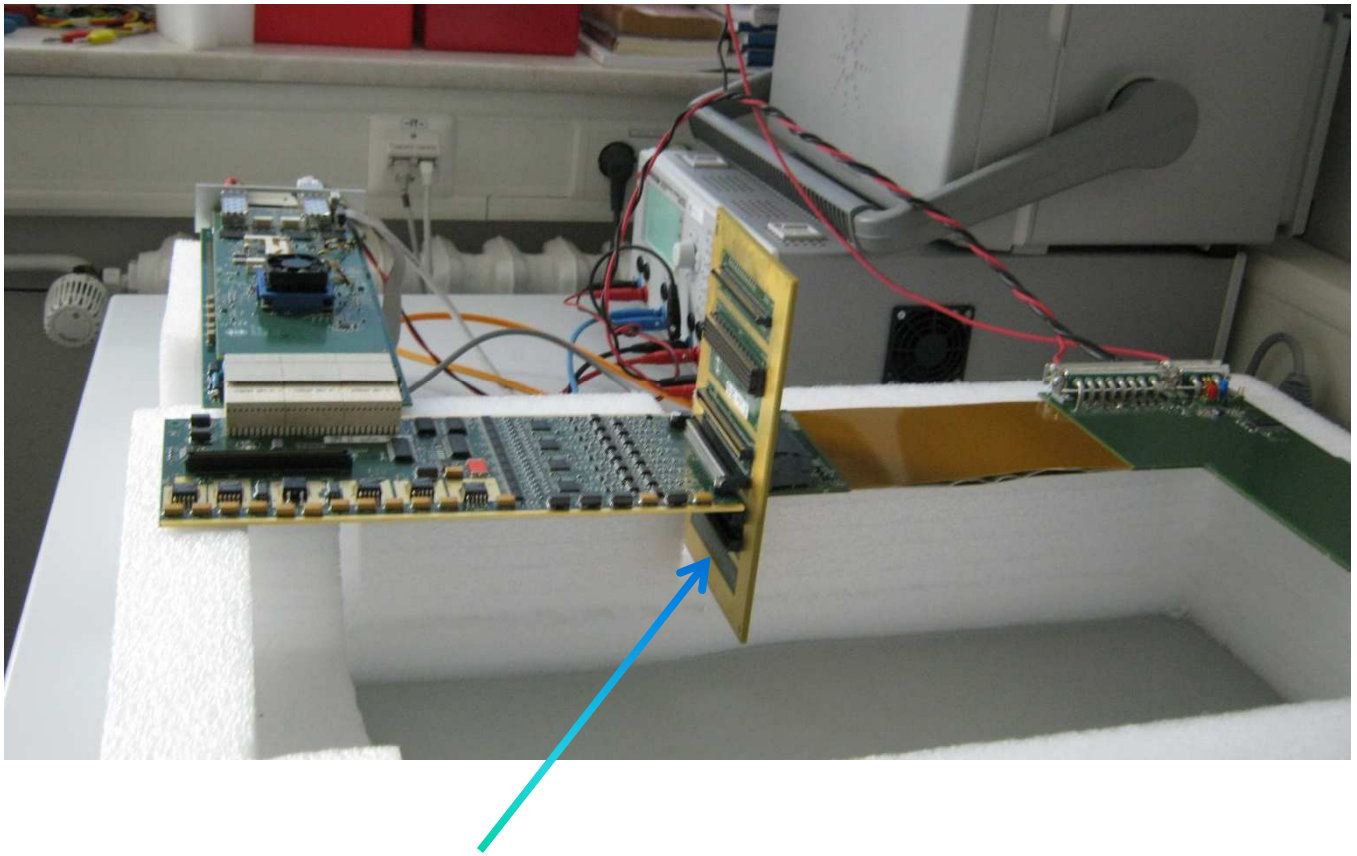

Test Bench Hardware Set Up

- Challenge



Test Bench Hardware Debugging

- Vacuum board
  - Shots found on the power supply connector