Update on the calibration activities and future plan discussion

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15 October, 2013
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Calibration procedure:

- Gain:

Slopes and offset for the 3 gain stages in each pixel.
In pixel pulsed capacitor: High-Med gain
In pixel current source: Med-Low gain

- Convert gain in number of photons on each pixel using lab radiation sources

Routinely X-ray sources
Ion sources

- Measure the pedestal for all 352 cells for the first gain

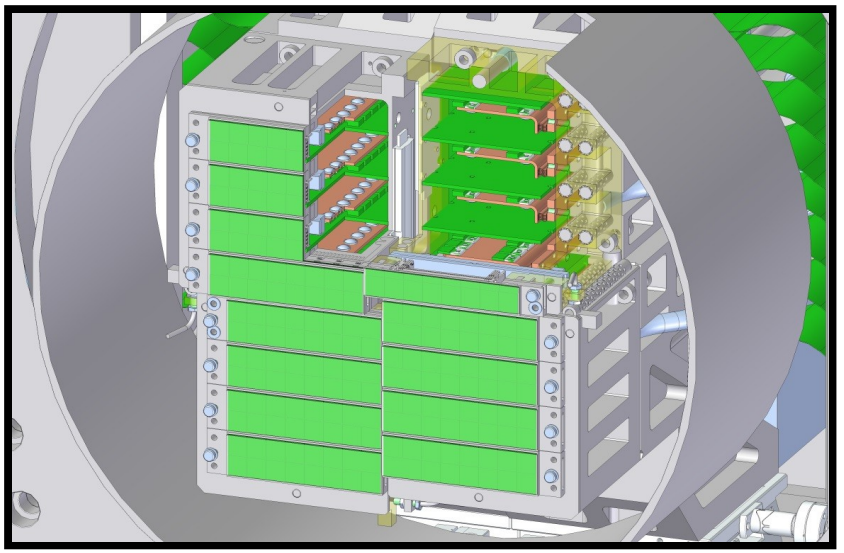
- Noise level+ bad/noisy pixels (from dark image)

- Measure droop for the 352 cells and store values at the appropriate time for the correction.

Calibration with X-Ray sources, some issues:

How to handle the calibration procedure of the 4 quadrants?
What is the more practical and reliable way of handling, per quadrant, per module?

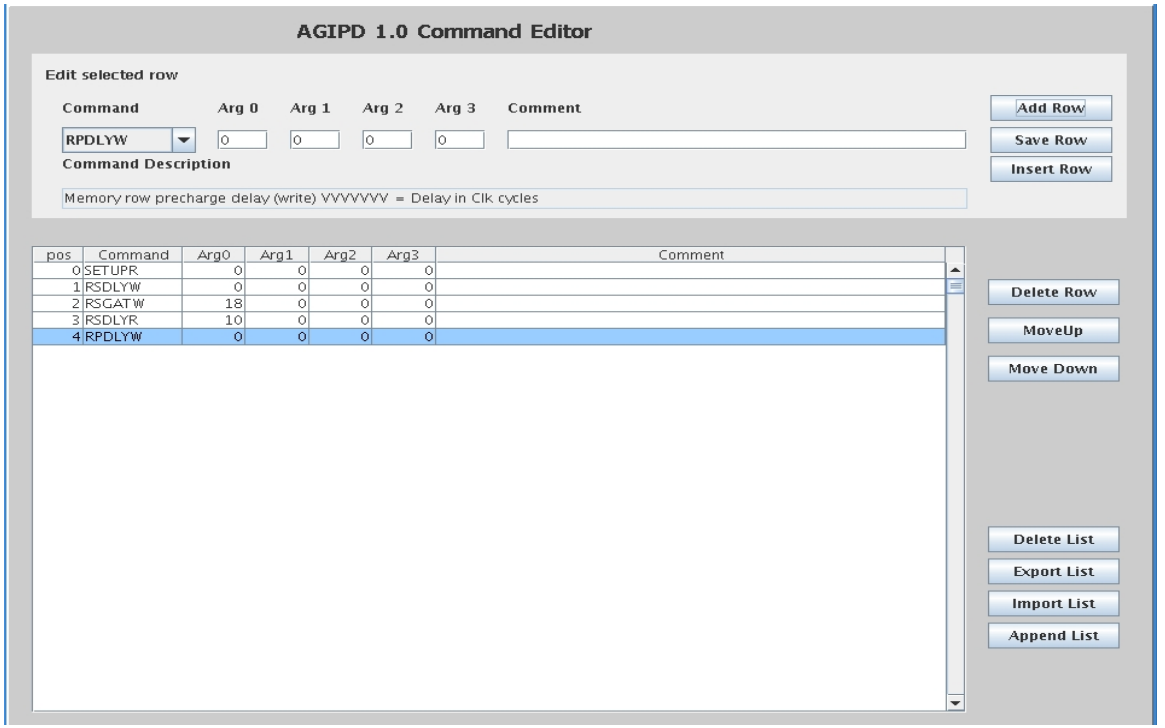
Can we take out 1 module at the time and place it in front of a X-ray lab source without compromising stability and reproducibility of the detector condition?



FPGA and Command Editor

FPGA and interface electronics work is ongoing (board being tested)

Command editor interface



We will have few fixed routine to be used for calibration that will be loaded with the command editor in the FPGA

Example of algorithm for droop check conversion

```
while(Run) \ Run control signals data taking

ACQMEM 0; \ record the frame from the reference cell (empty cell)

SETUPR 8'b10011000;    /enable test pulsed capacitor
for(frame=1;frame < 352, frame++)        \ record the first 352 frames in order
begin
ACQMEM frame; \ record the frame
end


for(frame < 352, frame = 0, frame++) \ read amplitude values of all frames
begin
SETMEM frame;
RPAMPN 0 0; \ precharge first row
for(row < 62, row = 0, row ++)
RPAMPA (row+1) row; \ mux row and precharge row+1
RPNMPA 0 63; \ mux last row
end
for(frame < 352, frame = 0, frame++) \ read gain values of all frames
begin
SETMEM frame;
RPDMPN 0 0; \ precharge first row
for(row < 62, row = 0, row ++)
RPDMPD (row+1) row; \ mux row and precharge row+1
RPNMPD 0 63; \ mux last row
end
frame = 0; \ reset variables
row = 0;
vetoed = 0;
vetoptr = 0;
end

SETUPR 8'b10001000; \  reset the chip and set DS gain high

/ second loop with waiting time:

while(Run) \ Run control signals data taking

ACQMEM 0; \ record the frame from the reference cell (empty cell)

SETUPR 8'b10011000;    /enable test pulsed capacitor
for(frame=1,frame < 352, frame++)        \ record the first 352 frames in order
begin
ACQMEM frame; \ record the frame
end

/loop to wait for some time for the droop:
for(frame=0,frame < 5000, frame++)
begin
SETMEM frame;   /execute the SETMEM as No OPeration command just to wait some clock cycles (5000 loops ~ 1.2 ms)
end

for(frame < 352, frame = 0, frame++) \ read amplitude values of all frames
begin
SETMEM frame;
RPAMPN 0 0; \ precharge first row
for(row < 62, row = 0, row ++)
RPAMPA (row+1) row; \ mux row and precharge row+1
RPNMPA 0 63; \ mux last row
end
for(frame < 352, frame = 0, frame++) \ read gain values of all frames
begin
SETMEM frame;
RPDMPN 0 0; \ precharge first row
for(row < 62, row = 0, row ++)
RPDMPD (row+1) row; \ mux row and precharge row+1
RPNMPD 0 63; \ mux last row
end
frame = 0; \ reset variables
row = 0;
vetoed = 0;
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end

SETUPR 8'b10001000; \  reset the chip and set DS gain high
```

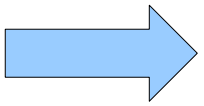

pos	Command	Arg0	Arg1	Arg2	Arg3	Comment
0	SETUPR	152	0	0	0	
1	LOOP__	351	0	0	0	
2	ACQMEM	351	0	0	0	
3	LOOP__	352	0	0	0	
4	SETMEM	0	0	0	0	
5	RPAMPN	0	0	0	0	
6	LOOP__	62	0	0	0	
7	RPAMPA	1	0	0	0	
8	RPAMPA	0	0	0	0	
9	TSTDLY	153	0	0	0	
10	SETMEM	351	0	0	0	

Command editor for FPGA

Assembly language style algorithm

Some time estimate:

Ongoing calibration using PSI chiptest box (focus on the calibration circuit test)

By end of 2013 AGIPD1.0 calibrated

As soon as FPGA is available start testing calibration routine

From January 2014 production of 1M system, test calibrate 1 module and estimate time for 16 modules