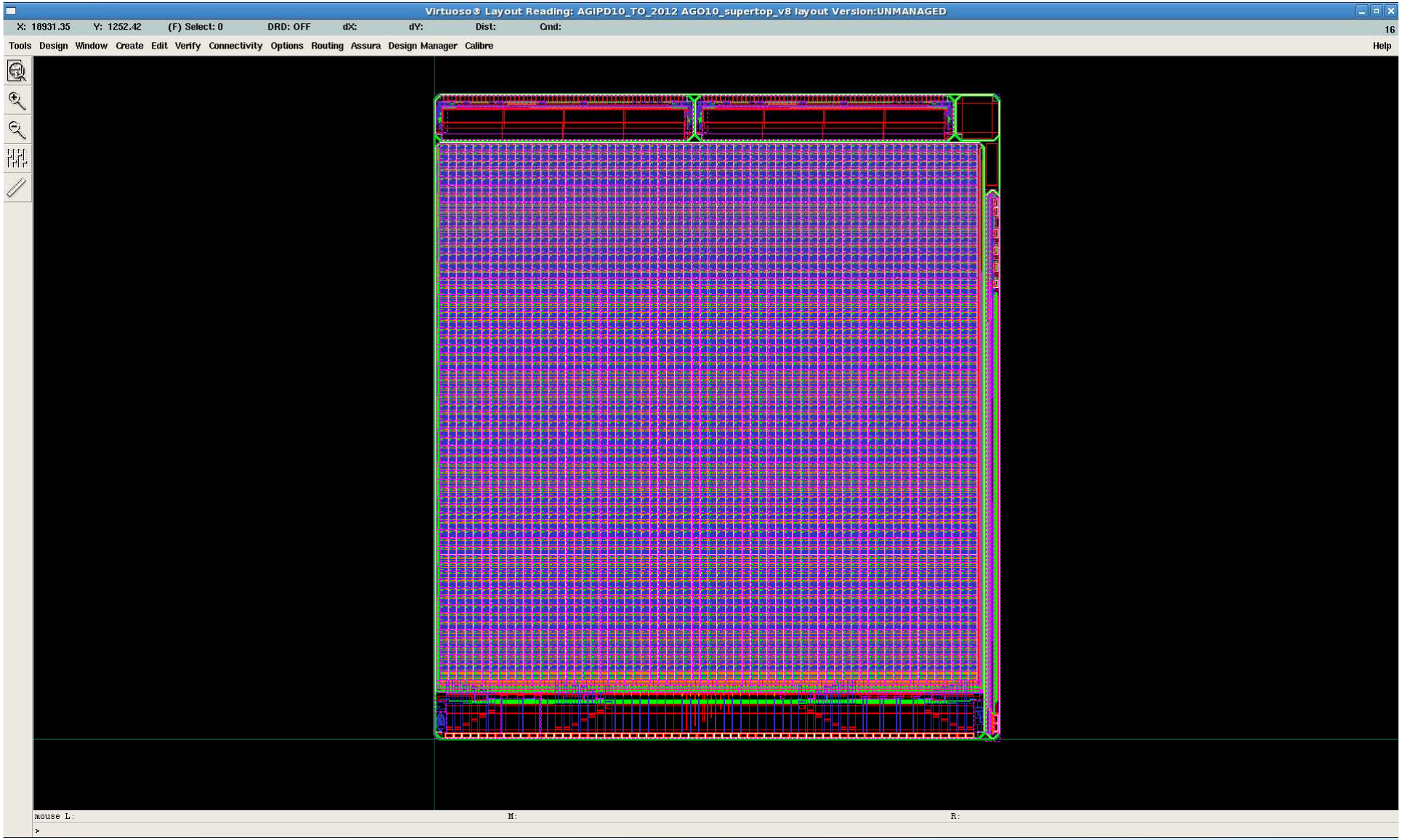
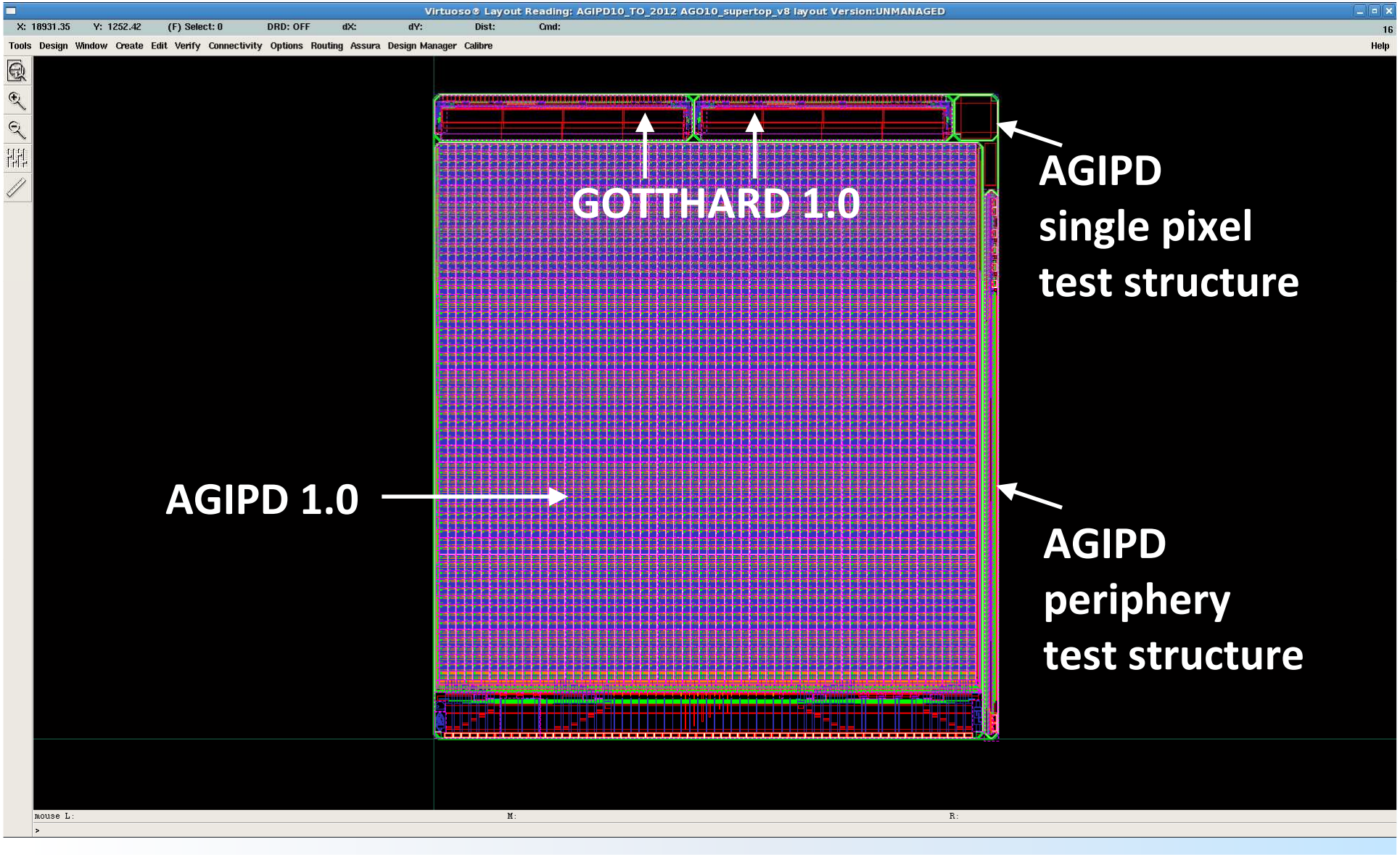
# Assembly status

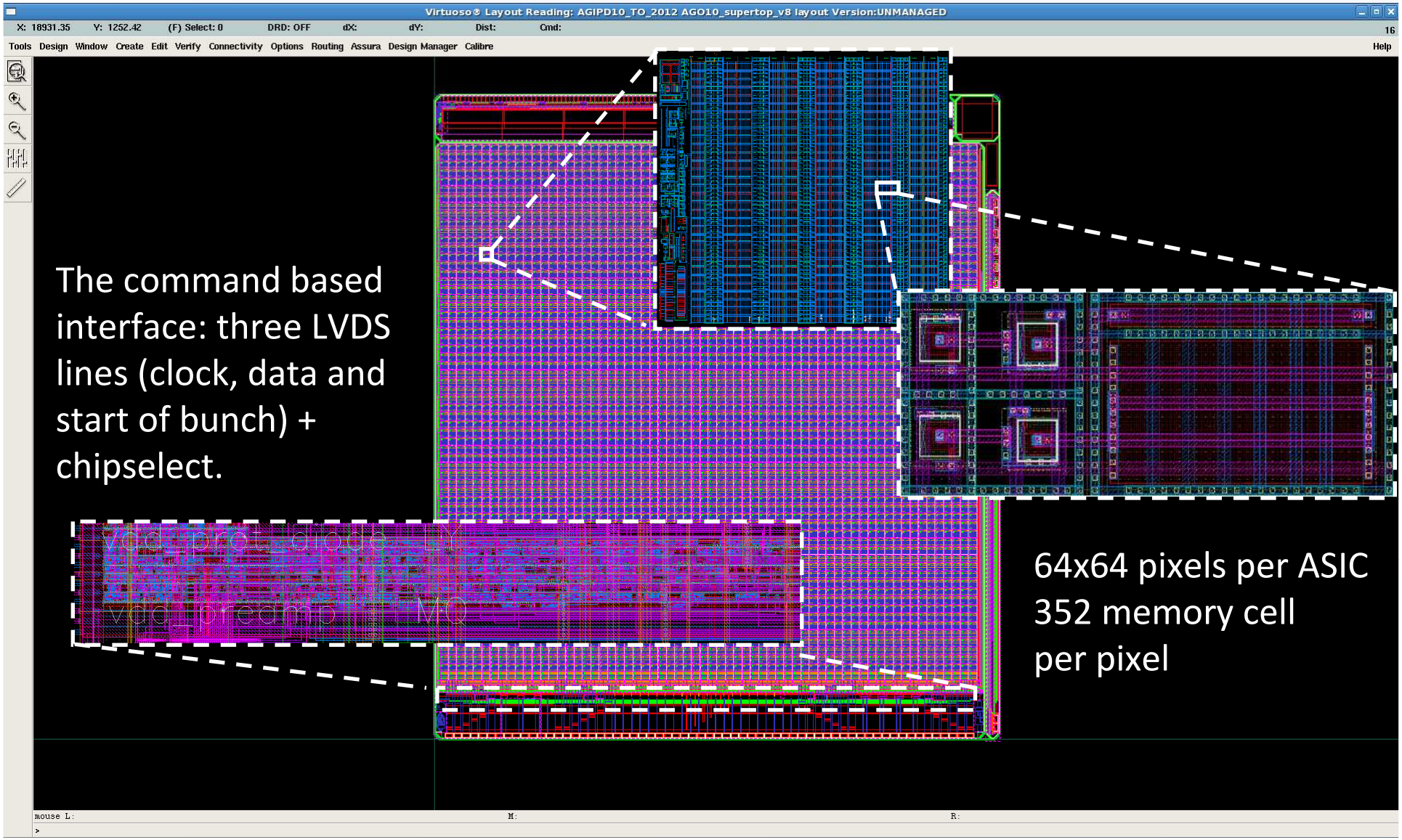
# assembly


Virtuoso® Layout Reading: AGIPD10_TO_2012 AGO10_supertop_v8 layout Version:UNMANAGED
X: 18931.35 Y: 1252.42 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd:
Tools Design Window Create Edit Verify Connectivity Options Routing Assura Design Manager Calibre Help
mouse L: M: R:

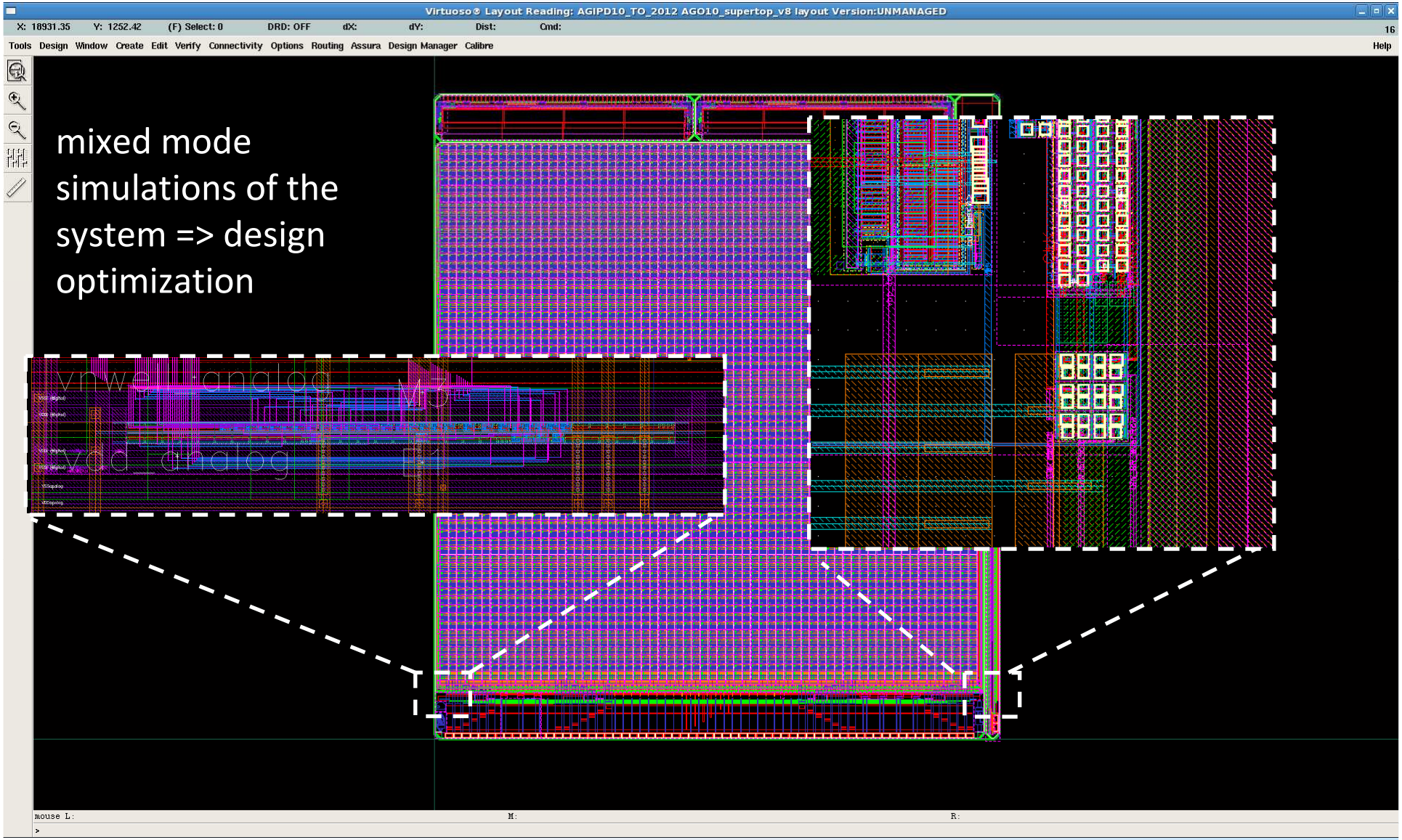
# assembly


Virtuoso® Layout Reading: AGIPD10_TO_2012 AGO10_supertop_v8 layout Version:UNMANAGED
X: 18931.35 Y: 1252.42 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd:
Tools Design Window Create Edit Verify Connectivity Options Routing Assura Design Manager Calibre Help
GOTTHARD 1.0
AGIPD
single pixel
test structure
AGIPD 1.0
AGIPD
periphery
test structure
mouse L: M: R:

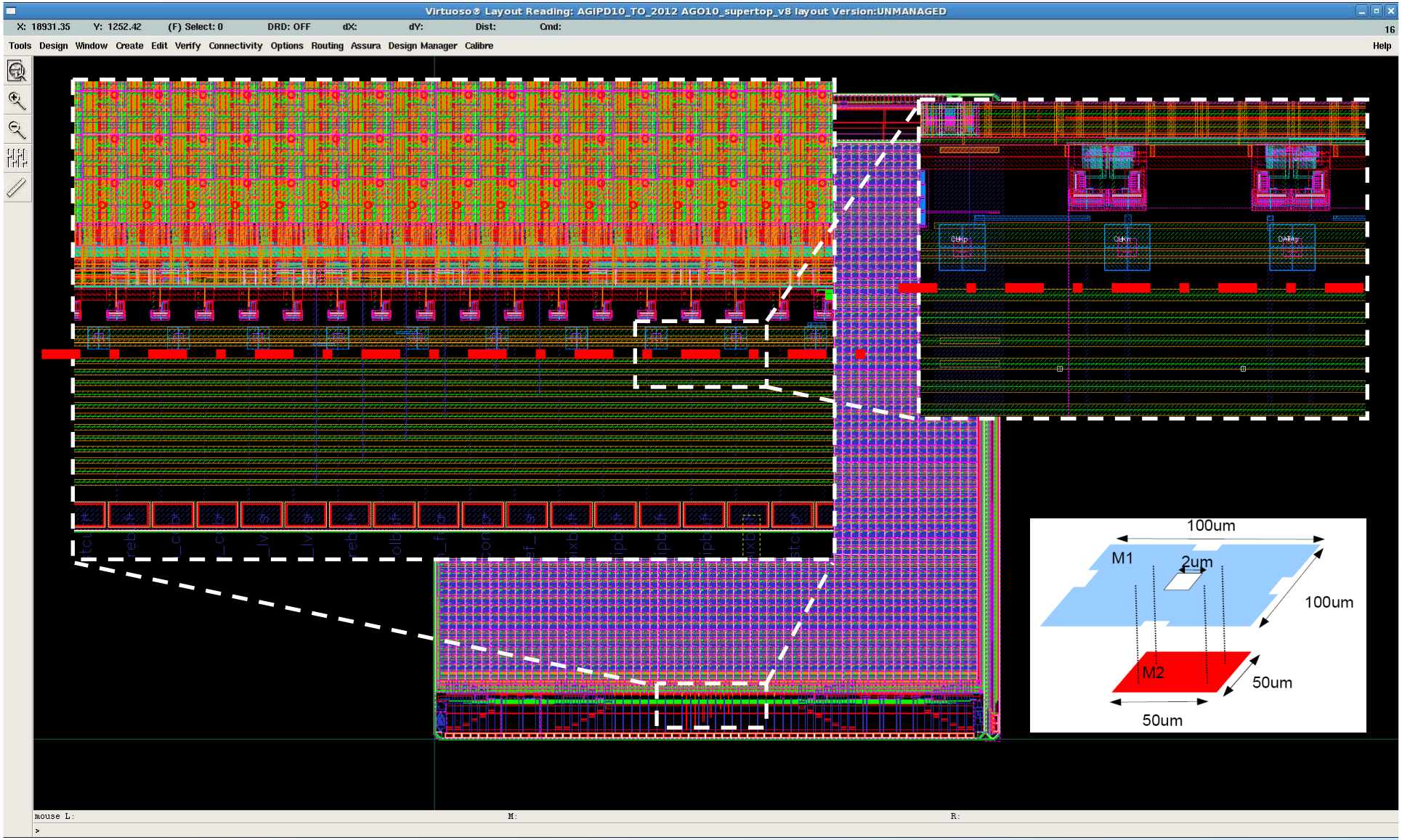
# AGIPD 1.0 general overview



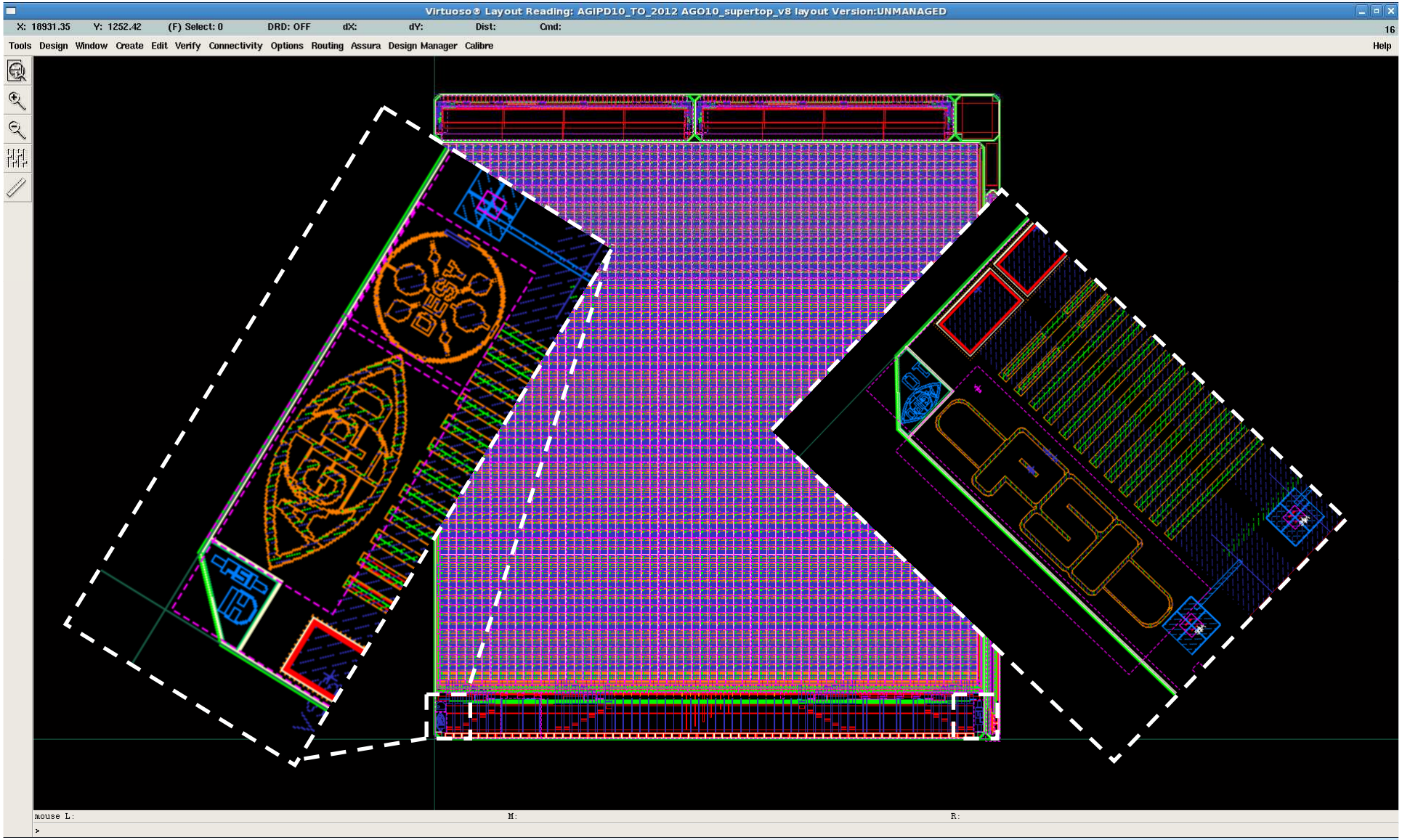
# buffers added to critical paths



# compatible with IZM TSV (edgless sensor possibility)



# logos


Virtuoso® Layout Reading: AGIPD10_TO_2012 AGO10_supertop_v8 layout Version:UNMANAGED
X: 18931.35 Y: 1252.42 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd:
Tools Design Window Create Edit Verify Connectivity Options Routing Assura Design Manager Calibre Help
mouse L: M: R:

# documentation effort


The AGIPD 1.0 ASIC Manual

Julian Becker[1], Roberto Dinapoli[2], Heinz Graafsma[1*], Dominic Greiffenberg[2], Alexander Klyuev[1], Alessandro Marras[1], Aldo Mozzanica[2], Bernd Schmitt[2], Xintian Shi[2], Ulrich Trunk[1]

[1]DESY Deutsches Elektronen-Synchrotron, Hamburg, Germany

[2]PSI Paul Scherrer Institut, Villingen, Switzerland

* also Mittuniversitet, Sundsvall, Sweden

Version 0.1α, April 8, 2013

Abstract

This document describes the AGIPD 1.0[1] ASIC[2] in terms of geometry, port definitions, electrical specifications, and of the implemented communications protocol. It furthermore provides brief descriptions of circuits implemented and sample command sequences for the operation on the ASIC.

AGIPD 1.0 ist the circuit to read out the AGIPD detector for the European XFEL. The detector features 1M ($1024 \times 1024$) pixels of 200µm pitch and is constructed from sensors of $128 \times 512$ pixels, bump-bonded to $2 \times 8$ ASICs. Each ASIC consists of the readout electronics for $64 \times 64$ pixels:

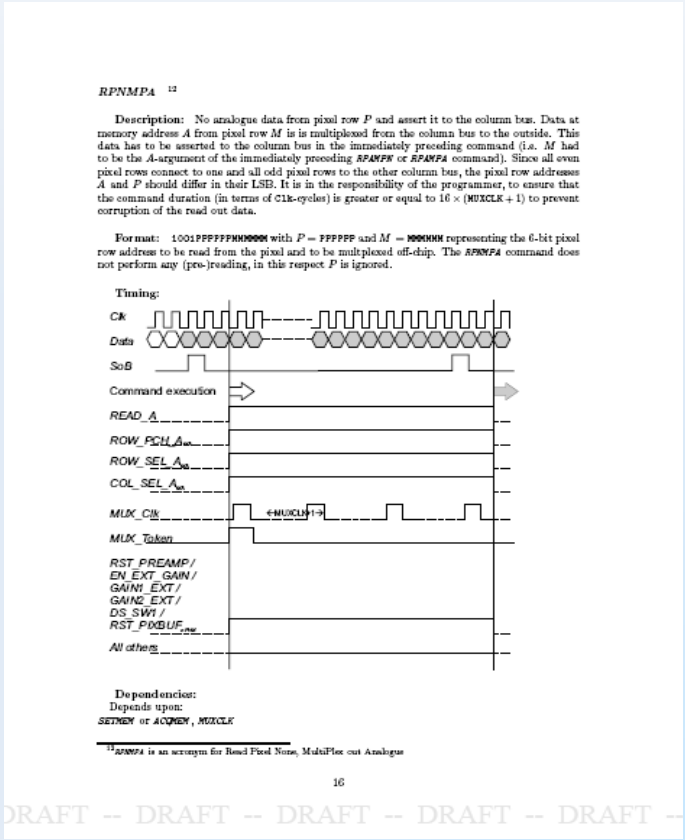
- A charge sensitive preamplifier with 3-fold self-adapting gain in each pixel
- A correlated double-sampling stage in each pixel
- Analogue storage for 352 samples (images) in each pixel
- Amplifiers and multiplexers to readout these signals via 4 differential analogue outputs
- Circuits for biasing and test signal injection
- A two-line serial interface to receive commands and digital circuitry to decode these and to steer and control the circuits mentioned above.

[1]Adaptive Gain Integrating Pixel Detector
[2]Application Specific Integrated Circuit

1



documentation (command description, “user manual”) being compiled



*RPNMPA* [12]

**Description:** No analogue data from pixel row $P$ and assert it to the column bus. Data at memory address $A$ from pixel row $M$ is is multiplexed from the column bus to the outside. This data has to be asserted to the column bus in the immediately preceding command (i.e. $M$ had to be the $A$-argument of the immediately preceding *RPAMPN* or *RPAMPA* command). Since all even pixel rows connect to one and all odd pixel rows to the other column bus, the pixel row addresses $A$ and $P$ should differ in their LSB. It is in the responsibility of the programmer, to ensure that the command duration (in terms of Clk-cycles) is greater or equal to $16 \times (\texttt{MUXCLK} + 1)$ to prevent corruption of the read out data.

**Format:** `1001PPPPPPMMMMMM` with $P =$ `PPPPPP` and $M =$ `MMMMMM` representing the 6-bit pixel row address to be read from the pixel and to be multiplexed off-chip. The *RPNMPA* command does not perform any (pre-)reading, in this respect $P$ is ignored.

**Timing:**

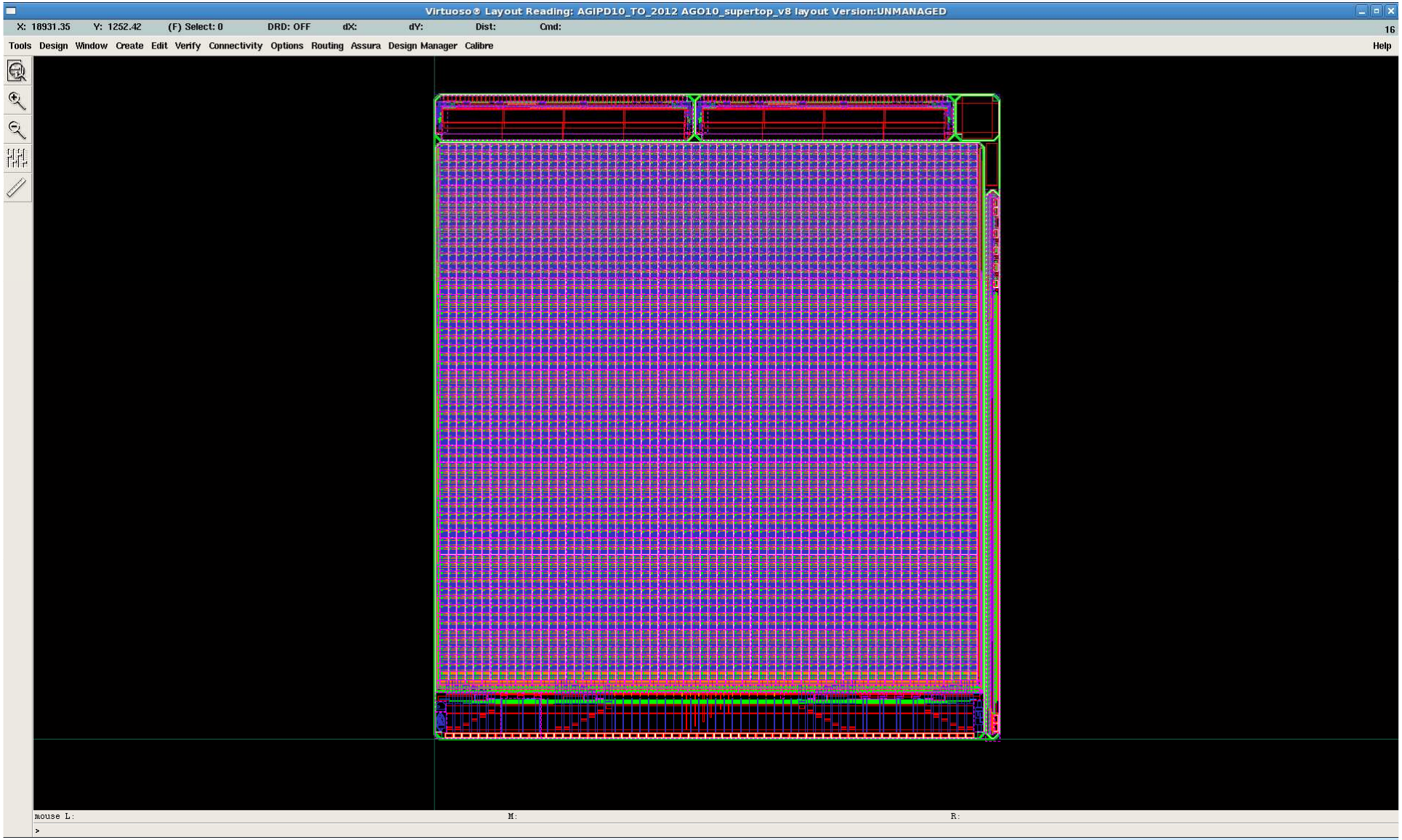


**Dependencies:**
Depends upon:
*SETMEN* or *ACQMEN*, *MUXCLK*

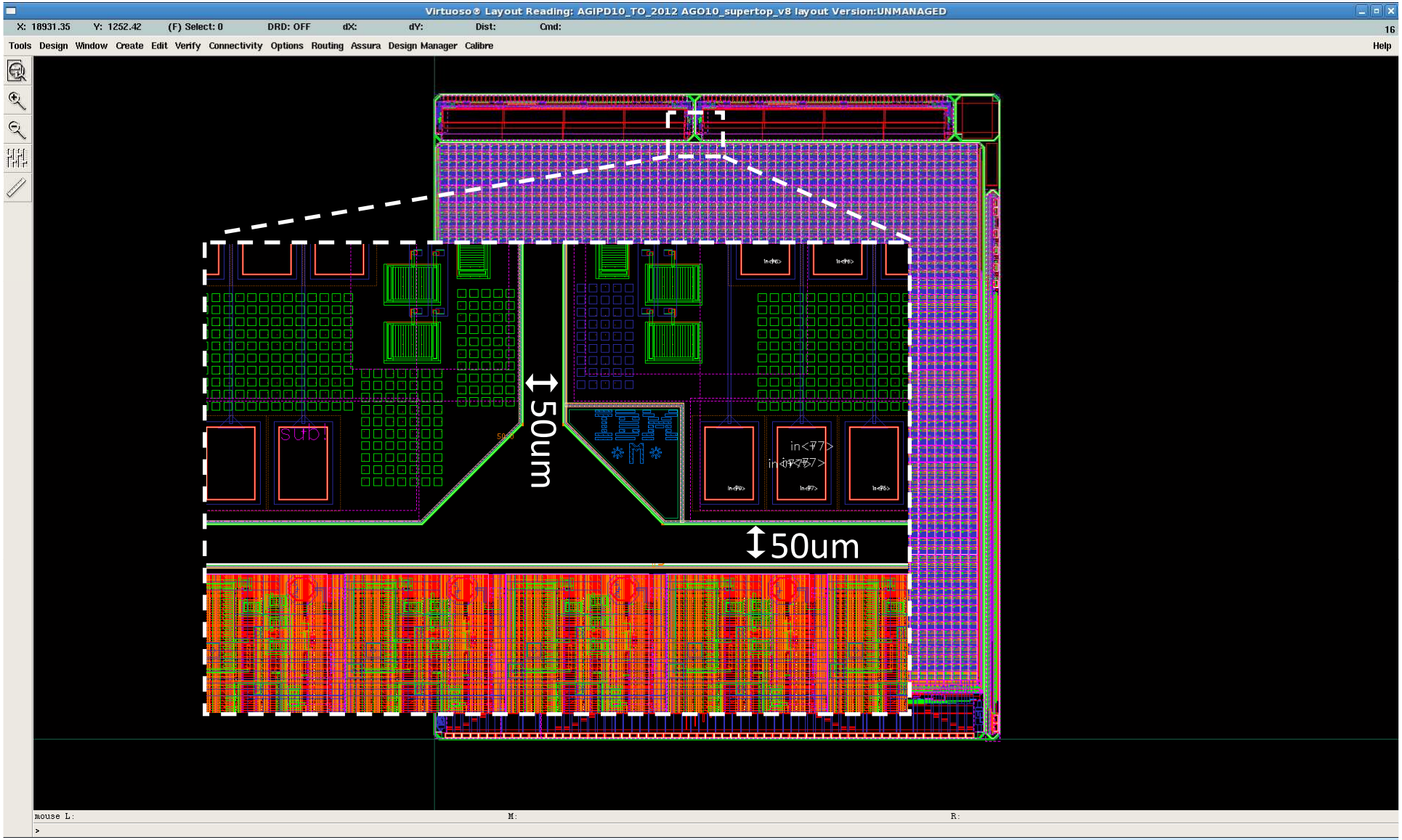
[12] *RPNMPA* is an acronym for Read Pixel None, MultiPlex out Analogue

16

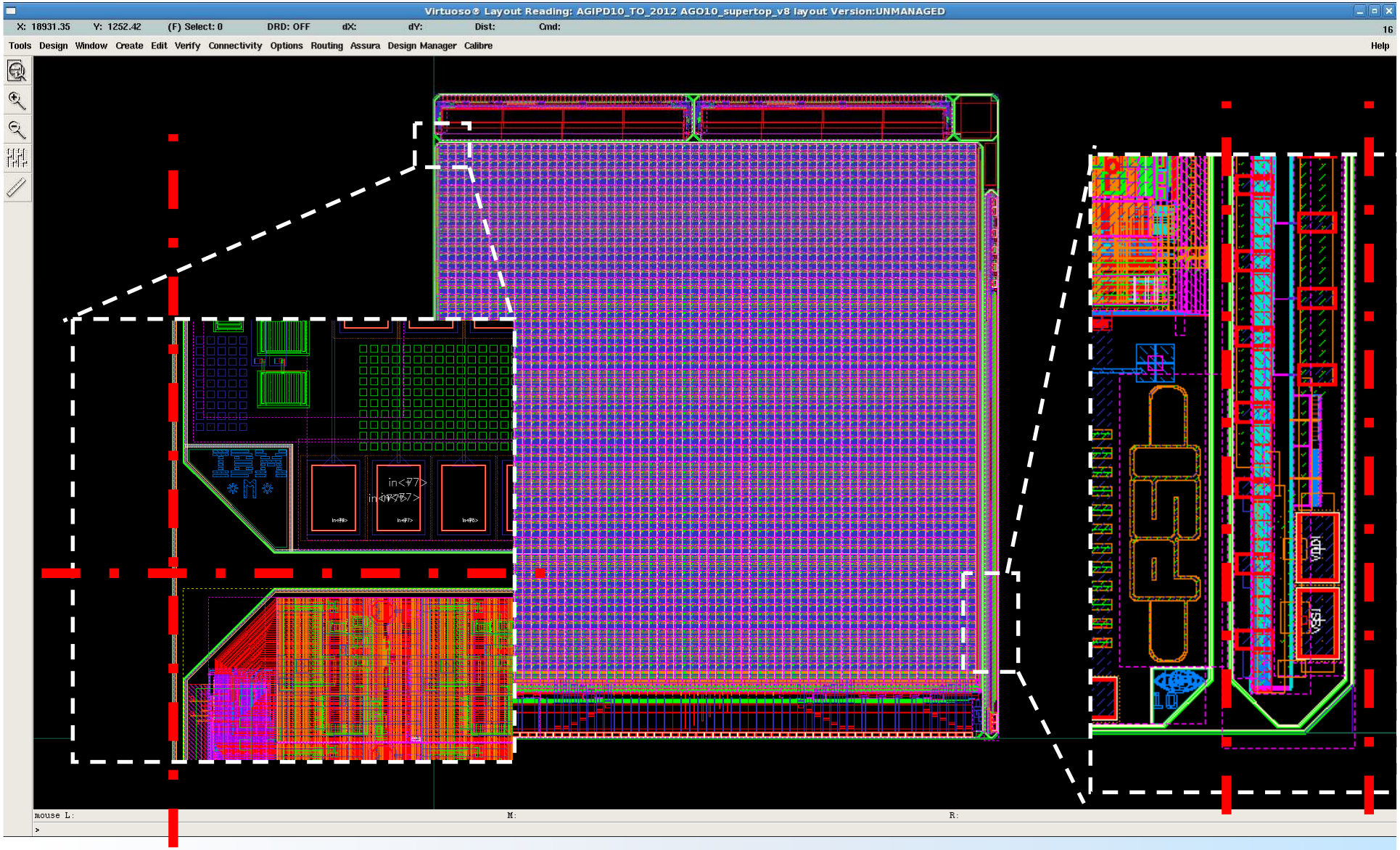
# assembly


Virtuoso® Layout Reading: AGIPD10_TO_2012 AGO10_supertop_v8 layout Version:UNMANAGED
X: 18931.35 Y: 1252.42 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd:
Tools Design Window Create Edit Verify Connectivity Options Routing Assura Design Manager Calibre Help
mouse L: M: R:

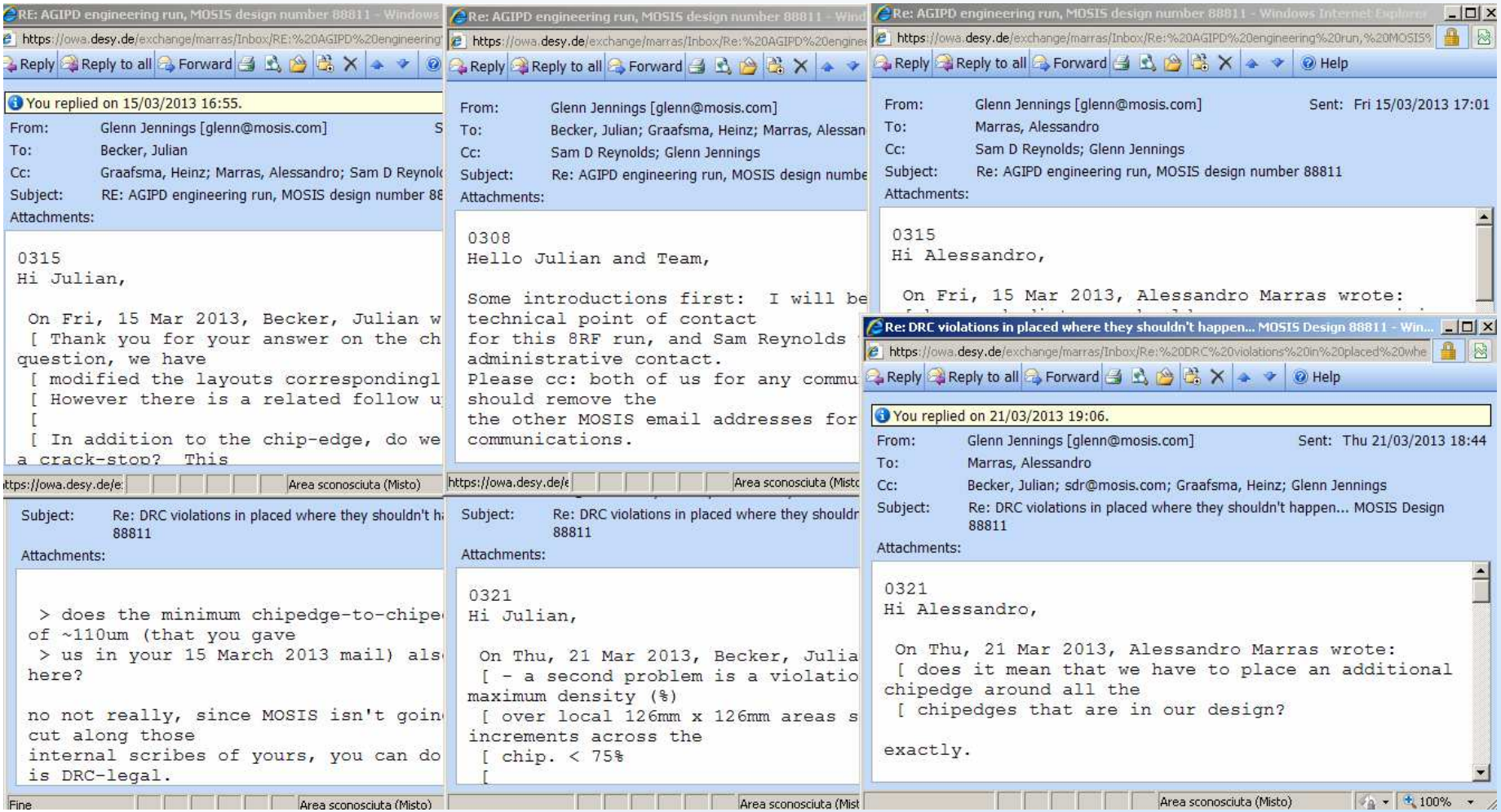
# assembly inner cutlines



# assembly outer cutlines



# interactions with Mosis already under way



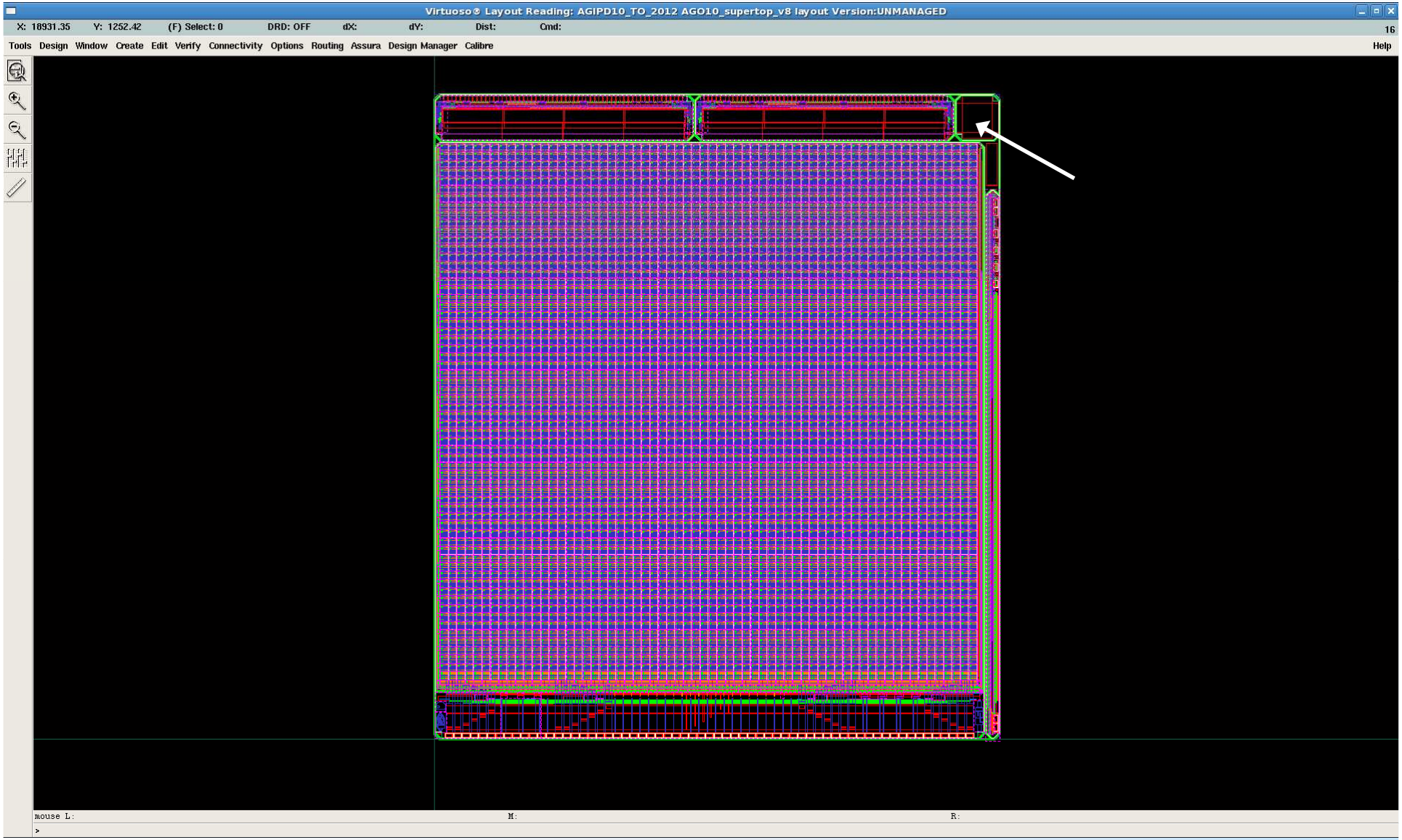

```
---------------------------------------------------------------------------------------------
 - Calibre - version: v2011.4_14.13 - report.drc.summary - Parser execution date: 4/[illegible]
---------------------------------------------------------------------------------------------
    Rule       | Cat |            Description                          | Error count
---------------------------------------------------------------------------------------------

GR655b     |  b  |DV width. | 28                                        | 8256
GRMA954    |  c  |Mx enclosed areas under (DV(touching MA) expanded by Rule MA| 640768
GRMA951    |  c  |(DV(touching MA) expanded by Rule MA948b1) terminal pad over| 19638
GRMA942b|  c  |DV(touching MA) terminal pad to {EFUSE, L1, QY, HY, F1, F1BA| 18560
GRMA946b|  c  |DV(touching MA) terminal pad width (parallel to the closest | 8803
GRMA945b|  c  |DV(touching MA) must be within CHIPEDGE (maximum) (entire DV| 4480
GRMA957    |  c  |(Mx over (DV(touching MA) expanded by Rule MA948b1 per edge)| 708
GRMA946g|  c  |DV(touching MA) terminal pad length (perpendicular to the cl| 115
GRMA956    |  c  |Mx (x=1,2,3,4,Q,G) over (DV(touching MA) expanded by Rule MA| 64

GRESD01    |  c  |All I/O (not including power supply pads) pads must be conne| 4469
GRESD01b|  c  |If none of the diffusion shapes within ESDUMMY identified in| 4469
GRESD01a|  c  |If none of the diffusion shapes within ESDUMMY identified in| 1087
GRESD10    |  c  |{[RX n+ diffusions connected to I/O signal pads], [(RX n+ di| 2463
GRESD08    |  c  |{[NW connected to I/O signal pads], [(NW within ESDUMMY) con| 4
GRESD09    |  c  |{[RX n+ diffusions connected to I/O signal pads], [(RX n+ di| 699
GRESD30    |  c  |All gates (not covered by DG) connected through metal or re| 534
```

major DRC issues already settled with Mosis


```
---------------------------------------------------------------------------------------------
 - Calibre - version: v2011.4_14.13 - report.drc.summary - Parser execution date: 4/6/2013
---------------------------------------------------------------------------------------------
    Rule       | Cat |            Description                          | Error count
---------------------------------------------------------------------------------------------

GRLUP13  |  b  |RX N+ (RX not over BP) shapes connected to an IO pad must be| 7514

GRZT1       |  b  |ZEROVT must overlap past gate on two opposite sides. | 0.66 | 1394
GR122a      |  c  |No bent gates (PC over RX) allowed over ZEROVT. | -        | 1394

GRPN101a |  b  |LOGOBND must not touch (CHIPEDGE sized by -150|m)(LOGOBND st| 6
GRPN101  |  b  |The leading edge of LOGOBND must be within CHIPEDGE (maximum| 2

GRPDPC     |  b  |(Summed PC area across full chip) / (CHIPEDGE area) | 15% | | 1
GRQCAP1c|  c  |(QY+HY) area (maximum per chip) (um2). | 2,000,000         | 1

GR1000MA|  c  |For designs that include MA, the guard ring must be connecte| 1
```

major DRC issues already settled with Mosis

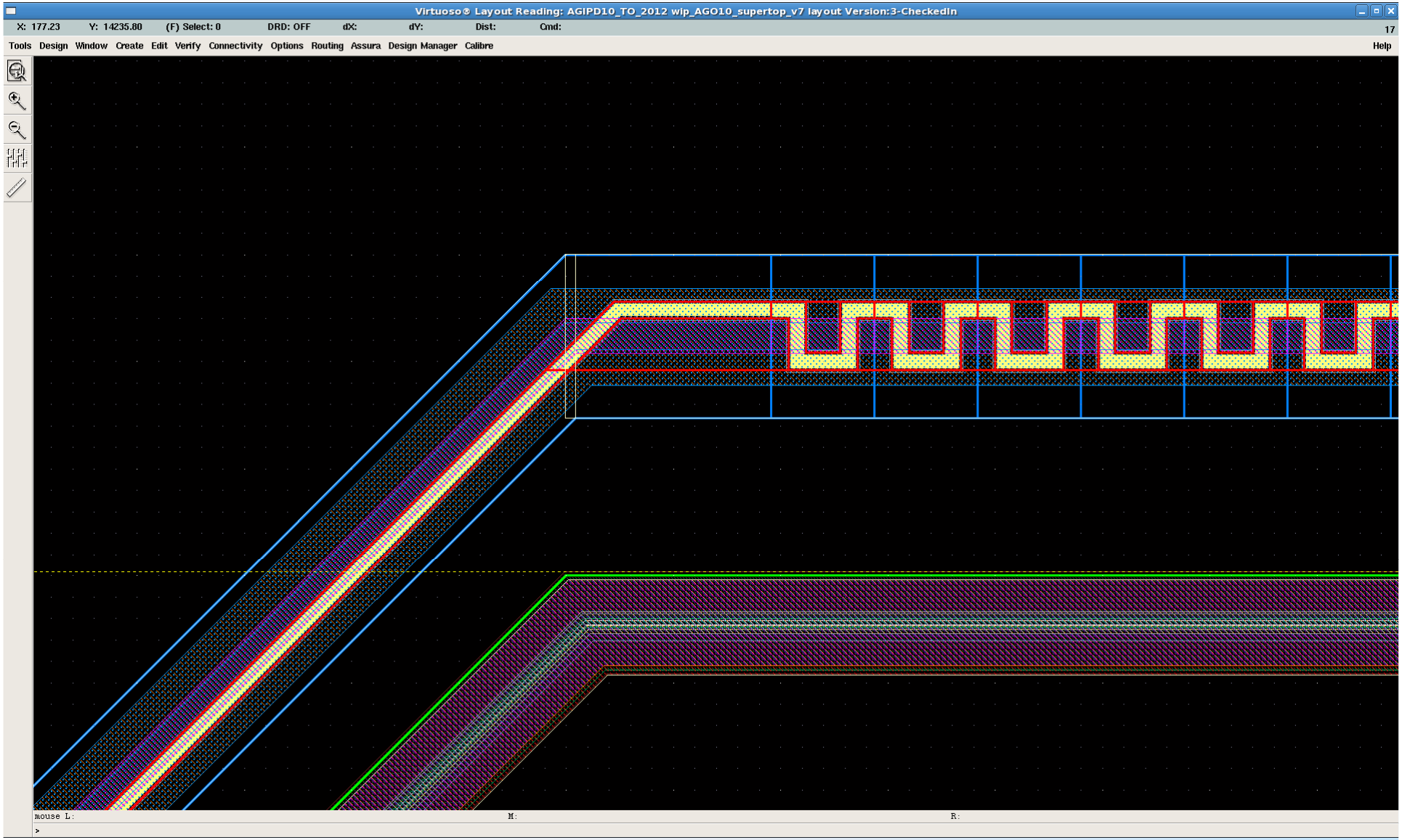
# assembly


Virtuoso® Layout Reading: AGIPD10_TO_2012 AGO10_supertop_v8 layout Version:UNMANAGED
X: 18931.35 Y: 1252.42 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd:
16
Tools Design Window Create Edit Verify Connectivity Options Routing Assura Design Manager Calibre
Help
mouse L:
M:
R:

# to do before submission

- single pixel test structure LVS (done this morning)
  - done
- mixed mode simulation with analog output (started lunchime)
  - result tomorrow afternoon
    - to be satisfied of them
- DRC of the assembly including single pixel structure (~ this evening/tomorrow)
  - ~half a day contingency to fix eventual issues


backup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Y: 14235.80
(F) Select: 0
DRD: OFF
dX:
dY:
Dist:
Cmd:
Tools Design Window Create Edit Verify Connectivity Options Routing Assura Design Manager Calibre
Help
mouse L:
M:
R:

Hi Alessandro,

On Mon, 25 Mar 2013, Alessandro Marras wrote:
[ Dear Dr Jennings,
[ as you have been told, we are to submit an aggregate: I am at the present
[ defining the dicing channel inside the aggregate.
[ I am worried that saw-induced vibration could cause cracks extending to our
[ circuits.
[ I reckon that enclosing each structure in a guardring (cell Image_bevel;
[ basically an octagon of all metals and all vias surrounding the structure)
[ should mitigate the risk.

Correct. IBM used to define two rings, one being the guardring which you know how to draw, and then a second ring out in the dicing channel called a "sealring" (sometimes called "crackstop"). This second ring has been found by IBM to serve very little value, so they are moving toward eliminating it. But the guardring remains as a safety margin.

Hi Alessandro,


I'm not the expert on this, Sam Reynolds will give you a more clear answer. But let me at least give an introduction:

On Mon, 8 Apr 2013, Marras, Alessandro wrote:
[ 1) how much silicon space should we expect to find between two
[ aggregates? (please remember we ask Mosis for uncut wafer)?
[ 2) I expect that in the space betweeen aggregates (i.e. along the
[ cutlines we will later cut along), IBM will put structures to monitor
[ the process parameters.
[ Is it possible to have such structures put only some cutlines
[ (e.g. only along vertical cutlines but not along horiziontal ones?)

Inside the CHIPEDGE which defines the aggregation's bouncing box:
IBM will place nothing; and it appears that you have understood this.

...


...
IBM has two kinds of structures, one of which are placed in one dimension (let's say, along the top/bottom of your aggregation), and the others placed along the other dimension (along the left/right of your aggregation). How much space depends on which structures occupies which dimension. In one dimension IBM places "optical structures" and these do not require much width. In the other they place "electical kerf stuctures", devices which are measured as fabrication proceeds, and these take much more width. The number of electrical devices which need to be placed are fixed: so if you request these electrical structures to go along your aggregation's narrow dimension, the width between aggregregations must become wider than if you give the "long side" to the electrial kerf.

IBM always uses these two opposing dimensions: optical along one axis, electrical along the other. They cannot both be combined into the same dimension.

With that introduction, I must pass your question to Sam.

Regards,
Glenn Jennings
MOSIS