



Assembly status



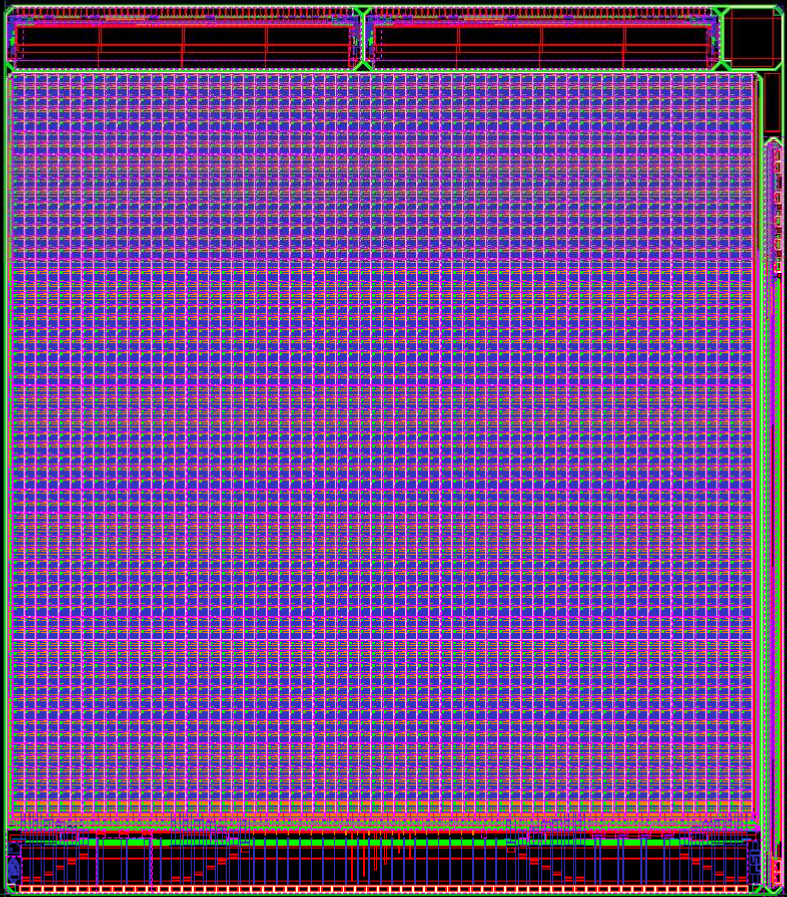
assembly



Virtuoso & Layout Reading: AGIPD10_TO_2012 AGO10_supertop_v8 layout Version:UNMANAGED

X: 18931.35 Y: 1252.42 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd: 16

Tools Design Window Create Edit Verify Connectivity Options Routing Assura Design Manager Calibre Help



mouse L: M: R:

>

The image shows a screenshot of a PCB layout software interface. The main window displays a large, dense grid of blue and purple lines, representing a fine grid or a complex routing pattern. The grid is bounded by a thick, multi-colored border (red, green, blue, yellow). The interface includes a top status bar with coordinates and tool settings, a menu bar with various options, and a left sidebar with icons for zooming and other functions. The bottom status bar shows mouse button indicators.

assembly



Virtuoso® Layout Reading: AGIPD10_TO_2012 AGO10_supertop_v8 layout Version:UNMANAGED

X: 18931.35 Y: 1252.42 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd: 16

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The diagram shows a detailed layout of a microchip. A large central area is filled with a dense grid of small, multi-colored squares (purple, blue, green, red). This area is labeled 'AGIPD 1.0' with a white arrow pointing to it from the left. Above this central area, there are two distinct rectangular regions with a different grid pattern, labeled 'GOTTHARD 1.0' with two white arrows pointing to them. To the right of the main grid, there is a narrow vertical strip of circuitry, labeled 'AGIPD periphery test structure' with a white arrow pointing to it. At the top right corner, there is a small, square-shaped structure labeled 'AGIPD single pixel test structure' with a white arrow pointing to it. The entire layout is displayed within a software window with a blue title bar and a menu bar.

AGIPD 1.0

GOTTHARD 1.0

AGIPD single pixel test structure

AGIPD periphery test structure

mouse L: M: R:

AGIPD 1.0 general overview



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16 Help

The command based interface: three LVDS lines (clock, data and start of bunch) + chipselect.

64x64 pixels per ASIC
352 memory cell
per pixel

buffers added to critical paths



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Tools Design Window Create Edit Verify Connectivity Options Routing Assura Design Manager Calibre Help

mixed mode simulations of the system => design optimization

The screenshot shows a detailed PCB layout in a Virtuoso environment. The layout is composed of various colored regions representing different materials or components. A large, semi-transparent window is overlaid on the layout, displaying a mixed-mode simulation. The simulation window shows two waveforms: 'vr_w_analog' and 'vcd_analog'. The 'vr_w_analog' waveform shows a complex, multi-colored signal, while the 'vcd_analog' waveform shows a more regular, periodic signal. The simulation window is titled 'mixed mode simulations of the system => design optimization'. The Virtuoso interface includes a toolbar on the left with icons for zooming and editing, and a status bar at the bottom with mouse and keyboard controls.

vr_w_analog
vcd_analog

mouse L:
>

M: R:

compatible with IZM TSV (edgless sensor possibility)



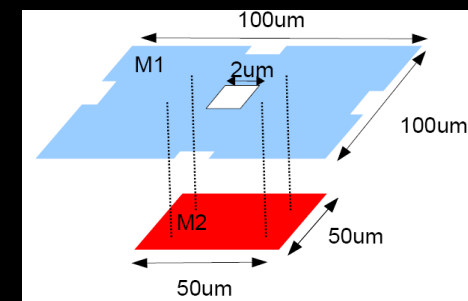
Virtuoso® Layout Reading: AGIPD10_TO_2012 AGO10_supertop_v8 layout Version:UNMANAGED

X: 18931.35 Y: 1252.42 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd: 16

Tools Design Window Create Edit Verify Connectivity Options Routing Assura Design Manager Calibre Help

The screenshot shows a complex layout design in a grid-based format. The design is composed of numerous small, repeating units, likely sensors or circuit elements, arranged in a regular pattern. The layout is color-coded, with different colors representing different layers or materials. A large, dense grid of red and green lines is visible, representing the main layout area. A smaller, more detailed view of a single unit is shown in the bottom right corner, illustrating the dimensions and structure of the individual components.

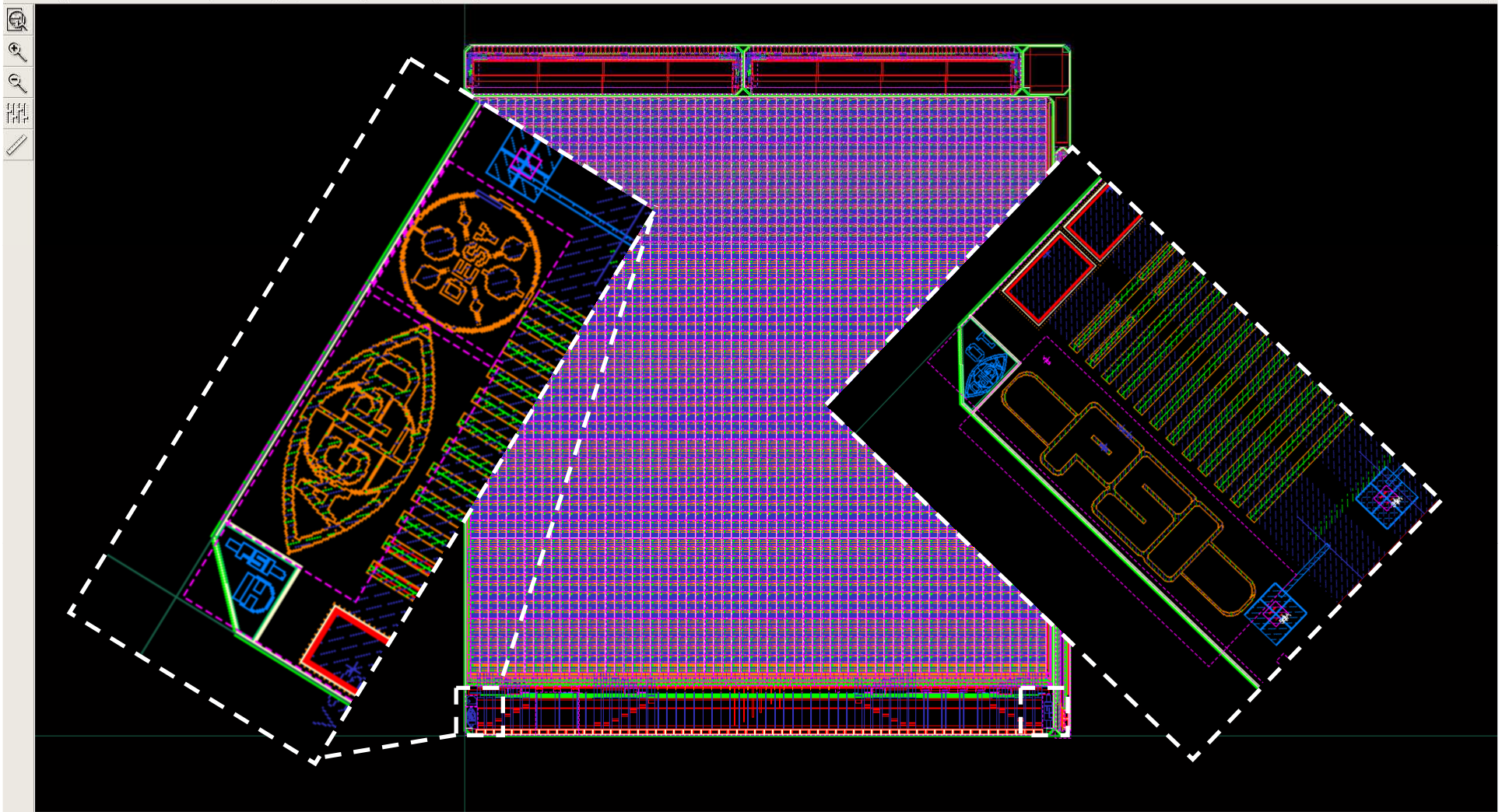
mouse L: M: R:



logos



Virtuoso® Layout Reading: AGIPD10_TO_2012 AGO10_supertop_v8 layout Version:UNMANAGED
X: 18931.35 Y: 1252.42 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd: 16
Tools Design Window Create Edit Verify Connectivity Options Routing Assura Design Manager Calibre Help



mouse L:

M:

R:

>

documentation effort



The AGIPD 1.0 ASIC Manual

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²PSI Paul Scherrer Institut, Villigen, Switzerland

* also Midevaden University, Sundsvall, Sweden

Version 0.1.0, April 8, 2013

Abstract

This document describes the AGIPD 1.0¹ ASIC² in terms of geometry, port definitions, electrical specifications, and of the implemented communications protocol. It furthermore provides brief descriptions of circuits implemented and sample command sequences for the operation on the ASIC.

AGIPD 1.0 is the circuit to read out the AGIPD detector for the European XFEL. The detector features 1M (1024 × 1024) pixels of 200µm pitch and is constructed from sensors of 128 × 512 pixels, bump-bonded to 2 × 8 ASICs. Each ASIC consists of the readout electronics for 64 × 64 pixels:

- A charge sensitive preamplifier with 3-fold self-adapting gain in each pixel
- A correlated double-sampling stage in each pixel
- Analogous storage for 352 samples (images) in each pixel
- Amplifiers and multiplexers to readout these signals via 4 differential analogue outputs
- Circuits for biasing and test signal injection
- A tree-line serial interface to receive commands and digital circuitry to decode these and to steer and control the circuits mentioned above.

¹Adaptive Gain Integrating Pixel Detector

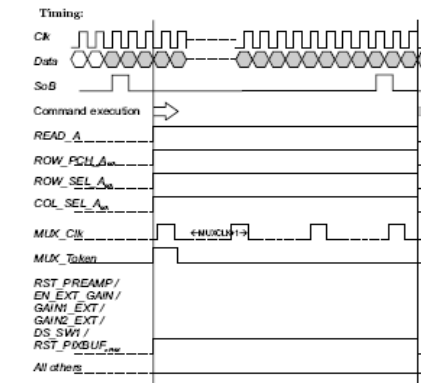
²Application Specific Integrated Circuit

documentation
(command description,
“user manual”)
being compiled

RPNMFA¹²

Description: No analogue data from pixel row P and assert it to the column bus. Data at memory address A from pixel row M is multiplexed from the column bus to the outside. This data has to be asserted to the column bus in the immediately preceding command (i.e. M had to be the A -argument of the immediately preceding *SPANEN* or *SPANFA* command). Since all even pixel rows connect to one and all odd pixel rows to the other column bus, the pixel row addresses A and P should differ in their LSB. It is in the responsibility of the programmer, to ensure that the command duration (in terms of CLK-cycles) is greater or equal to $16 \times (\text{MIXCLK} + 1)$ to prevent corruption of the read out data.

Format: 1001PPPPFFHHMMMM with $P = \text{FFFFFF}$ and $M = \text{MMMM}$ representing the 6-bit pixel row address to be read from the pixel and to be multiplexed off-chip. The *RPNMFA* command does not perform any (pre-)reading, in this respect P is ignored.



Dependencies:
DS_SW:
SETGEN or ACQGEN, MIXCLK

¹²RPNMFA is an acronym for Read Pixel Noise, MultiPixel Out Analogue

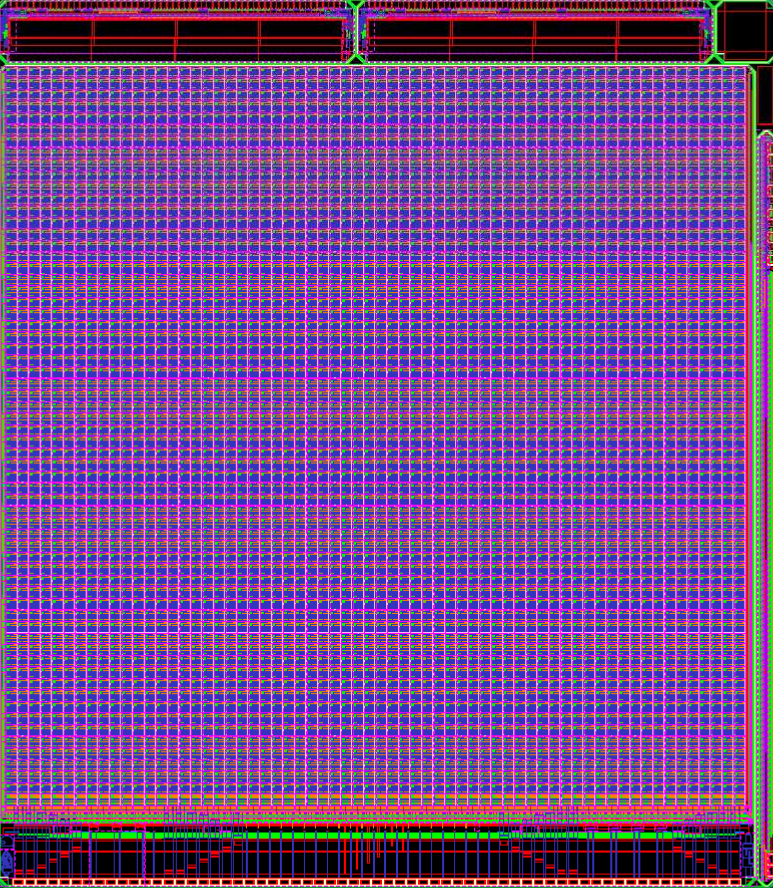
assembly



Virtuoso & Layout Reading: AGIPD10_TO_2012 AGO10_supertop_v8 layout Version:UNMANAGED

X: 18931.35 Y: 1252.42 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd: 16

Tools Design Window Create Edit Verify Connectivity Options Routing Assura Design Manager Calibre Help



mouse L: M: R:

>

The image shows a screenshot of a PCB layout software interface. The main window displays a large, dense grid of blue and purple lines, representing a fine grid or a complex routing pattern. The grid is bounded by a thick, multi-colored border (red, green, blue, yellow). The interface includes a top status bar with coordinates and tool settings, a menu bar with various options like 'Tools', 'Design', and 'Verify', and a left sidebar with icons for zooming and other functions. The bottom status bar shows mouse button indicators.

assembly inner cutlines



Virtuoso® Layout Reading: AGIPD10_TO_2012 AGO10_supertop_v8 layout Version:UNMANAGED

X: 18931.35 Y: 1252.42 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd: 16

Tools Design Window Create Edit Verify Connectivity Options Routing Assura Design Manager Calibre Help

The image shows a detailed PCB layout in a software interface. The layout is primarily black with various colored patterns representing different layers or materials. A central area is highlighted with a dashed white line, and two white arrows with the text "50um" indicate the width of the inner cutlines. The layout includes several rectangular blocks, some labeled "sub:" and "in<77>". The interface includes a toolbar on the left with icons for zooming and editing, and a status bar at the bottom with mouse coordinates (L, M, R) and a cursor arrow.

assembly outer cutlines



Virtuoso® Layout Reading: AGIPD10_TO_2012 AGO10_supertop_v8 layout Version:UNMANAGED

X: 18931.35 Y: 1252.42 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd:

Tools Design Window Create Edit Verify Connectivity Options Routing Assura Design Manager Calibre

The image shows a detailed PCB layout in a software interface. The layout is primarily black with various colored traces and components. A large, dense grid of purple and blue lines is visible in the upper right quadrant. The layout is bounded by a thick red dashed line representing the assembly outer cutline. A white dashed line indicates a specific region or boundary. The interface includes a top menu bar, a toolbar on the left, and a status bar at the bottom with mouse coordinates (L, M, R) and a cursor arrow.

mouse L: M: R:

interactions with Mosis already under way



The screenshot shows three overlapping email windows from a client. The top row contains three windows, and the bottom row contains one larger window.

Top Left Window: "RE: AGIPD engineering run, MOSIS design number 88811 - Windows". Sent: 15/03/2013 16:55. From: Glenn Jennings [glenn@mosis.com]. To: Becker, Julian. Subject: RE: AGIPD engineering run, MOSIS design number 88811. Content: "0315 Hi Julian, On Fri, 15 Mar 2013, Becker, Julian w [Thank you for your answer on the ch question, we have [modified the layouts correspondingl [However there is a related follow u [[In addition to the chip-edge, do we a crack-stop? This

Top Middle Window: "RE: AGIPD engineering run, MOSIS design number 88811 - Windows". Sent: Fri 15/03/2013 17:01. From: Glenn Jennings [glenn@mosis.com]. To: Marras, Alessandro. Subject: Re: AGIPD engineering run, MOSIS design number 88811. Content: "0315 Hi Alessandro, On Fri, 15 Mar 2013, Alessandro Marras wrote: Some introductions first: I will be technical point of contact for this 8RF run, and Sam Reynolds administrative contact. Please cc: both of us for any commu should remove the the other MOSIS email addresses for communications."

Top Right Window: "Re: DRC violations in placed where they shouldn't happen... MOSIS Design 88811 - Win...". Sent: Thu 21/03/2013 18:44. From: Glenn Jennings [glenn@mosis.com]. To: Marras, Alessandro. Subject: Re: DRC violations in placed where they shouldn't happen... MOSIS Design 88811. Content: "0321 Hi Julian, On Thu, 21 Mar 2013, Becker, Julia [- a second problem is a violatio maximum density (%) [over local 126mm x 126mm areas s increments across the [chip. < 75% [

Bottom Window: "Re: DRC violations in placed where they shouldn't happen... MOSIS Design 88811". Sent: Thu 21/03/2013 19:06. From: Glenn Jennings [glenn@mosis.com]. To: Marras, Alessandro. Subject: Re: DRC violations in placed where they shouldn't happen... MOSIS Design 88811. Content: "0321 Hi Alessandro, On Thu, 21 Mar 2013, Alessandro Marras wrote: [does it mean that we have to place an additional chipedge around all the [chipedges that are in our design? exactly."



Rule	Cat	Description	Error count
GR655b	b	DV width.	28 8256
GRMA954	c	Mx enclosed areas under (DV(touching MA) expanded by Rule MA	640768
GRMA951	c	(DV(touching MA) expanded by Rule MA948b1) terminal pad over	19638
GRMA942b	c	DV(touching MA) terminal pad to {EFUSE, L1, QY, HY, F1, F1BA	18560
GRMA946b	c	DV(touching MA) terminal pad width (parallel to the closest	8803
GRMA945b	c	DV(touching MA) must be within CHIPEDGE (maximum) (entire DV	4480
GRMA957	c	(Mx over (DV(touching MA) expanded by Rule MA948b1 per edge)	708
GRMA946g	c	DV(touching MA) terminal pad length (perpendicular to the cl	115
GRMA956	c	Mx (x=1,2,3,4,Q,G) over (DV(touching MA) expanded by Rule MA	64
GRES01	c	All I/O (not including power supply pads) pads must be conne	4469
GRES01b	c	If none of the diffusion shapes within ESDUMMY identified in	4469
GRES01a	c	If none of the diffusion shapes within ESDUMMY identified in	4469
GRES10	c	{[RX n+ diffusions connected to I/O signal pads], [(RX n+ d	2463
GRES08	c	{[NW connected to I/O signal pads], [(NW within ESDUMMY) con	4
GRES09	c	{[RX n+ diffusions connected to I/O signal pads], [(RX n+ di	699
GRES30	c	All gates (not covered by DG) connected (through metal or re	534

major DRC issues already settled with Mosis



Rule	Cat	Description	Error count
GRLUP13	b	RX N+ (RX not over BP) shapes connected to an IO pad must be	7514
GRZT1	b	ZEROVT must overlap past gate on two opposite sides.	0.66 1394
GR122a	c	No bent gates (PC over RX) allowed over ZEROVT.	- 1394
GRPN101a	b	LOGOBND must not touch (CHIPEDGE sized by -150 m)(LOGOBND st	6
GRPN101	b	The leading edge of LOGOBND must be within CHIPEDGE (maximum	2
GRPDPC	b	(Summed PC area across full chip) / (CHIPEDGE area)	15% 1
GRQCAP1c	c	(QY+HY) area (maximum per chip) (um ²).	2,000,000 1
GR1000MA	c	For designs that include MA, the guard ring must be connecte	1

major DRC issues already settled with Mosis

assembly



Virtuoso & Layout Reading: AGIPD10_TO_2012 AGO10_supertop_v8 layout Version:UNMANAGED

X: 18931.35 Y: 1252.42 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd: 16

Tools Design Window Create Edit Verify Connectivity Options Routing Assura Design Manager Calibre Help

A screenshot of a PCB layout viewer. The main area shows a dense grid of components, likely a microcontroller or a similar integrated circuit, rendered in various colors (blue, purple, red, green). A white arrow points to a specific component in the top right corner of the grid. The interface includes a top status bar with coordinates and tool settings, a menu bar, and a toolbar on the left side with icons for zooming and other functions. At the bottom, there are labels for mouse and keyboard controls: 'mouse L:', 'M:', and 'R:'.

to do before submission



- single pixel test structure LVS (done this morning)
 - done
- mixed mode simulation with analog output (started lunchtime)
 - result tomorrow afternoon
 - to be satisfied of them
- DRC of the assembly including single pixel structure (~ this evening/tomorrow)
 - ~half a day contingency to fix eventual issues





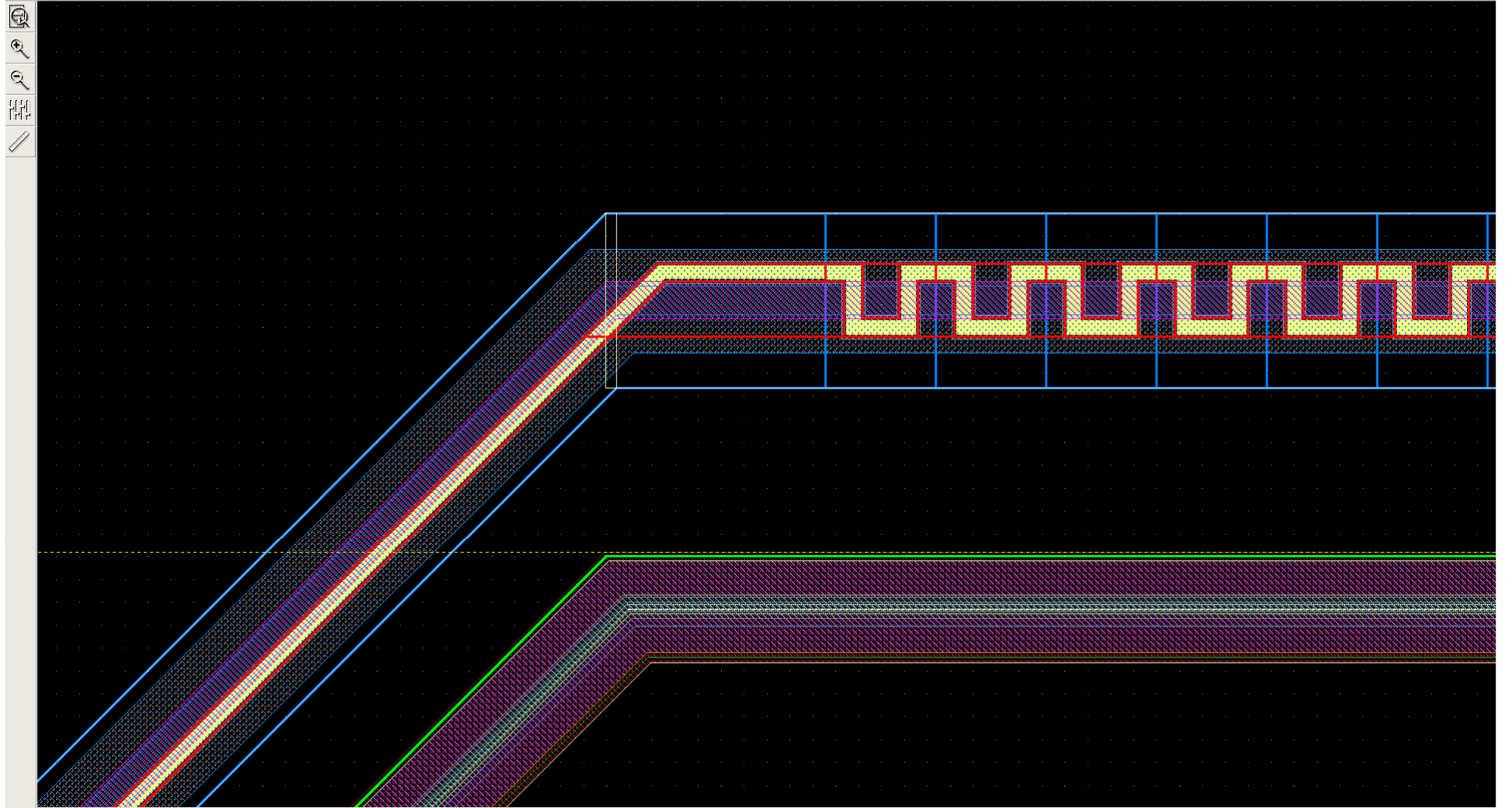
backup



Virtuoso® Layout Reading: AGIPD10_TO_2012_wip_AGO10_supertop_v7 layout Version:3-CheckedIn

X: 177.23 Y: 14235.80 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd: 17

Tools Design Window Create Edit Verify Connectivity Options Routing Assura Design Manager Calibre Help



mouse L:
>

M:

R:



Hi Alessandro,

On Mon, 25 Mar 2013, Alessandro Marras wrote:

[Dear Dr Jennings,

[as you have been told, we are to submit an aggregate: I am at the present

[defining the dicing channel inside the aggregate.

[I am worried that saw-induced vibration could cause cracks extending to our

[circuits.

[I reckon that enclosing each structure in a guardring (cell Image_bevel;

[basically an octagon of all metals and all vias surrounding the structure)

[should mitigate the risk.

Correct. IBM used to define two rings, one being the guardring which you know how to draw, and then a second ring out in the dicing channel called a "sealring" (sometimes called "crackstop"). This second ring has been found by IBM to serve very little value, so they are moving toward eliminating it. But the guardring remains as a safety margin.

Hi Alessandro,



I'm not the expert on this, Sam Reynolds will give you a more clear answer. But let me at least give an introduction:

On Mon, 8 Apr 2013, Marras, Alessandro wrote:

- [1) how much silicon space should we expect to find between two aggregates? (please remember we ask Mosis for uncut wafer)?
- [2) I expect that in the space between aggregates (i.e. along the cutlines we will later cut along), IBM will put structures to monitor the process parameters.
- [Is it possible to have such structures put only some cutlines (e.g. only along vertical cutlines but not along horizontal ones?)

Inside the CHIPEDGE which defines the aggregation's bouncing box: IBM will place nothing; and it appears that you have understood this.

...



...

IBM has two kinds of structures, one of which are placed in one dimension (let's say, along the top/bottom of your aggregation), and the others placed along the other dimension (along the left/right of your aggregation). How much space depends on which structures occupies which dimension. In one dimension IBM places "optical structures" and these do not require much width. In the other they place "electrical kerf structures", devices which are measured as fabrication proceeds, and these take much more width. The number of electrical devices which need to be placed are fixed: so if you request these electrical structures to go along your aggregation's narrow dimension, the width between aggregations must become wider than if you give the "long side" to the electrical kerf.

IBM always uses these two opposing dimensions: optical along one axis, electrical along the other. They cannot both be combined into the same dimension.

With that introduction, I must pass your question to Sam.

Regards,
Glenn Jennings
MOSIS