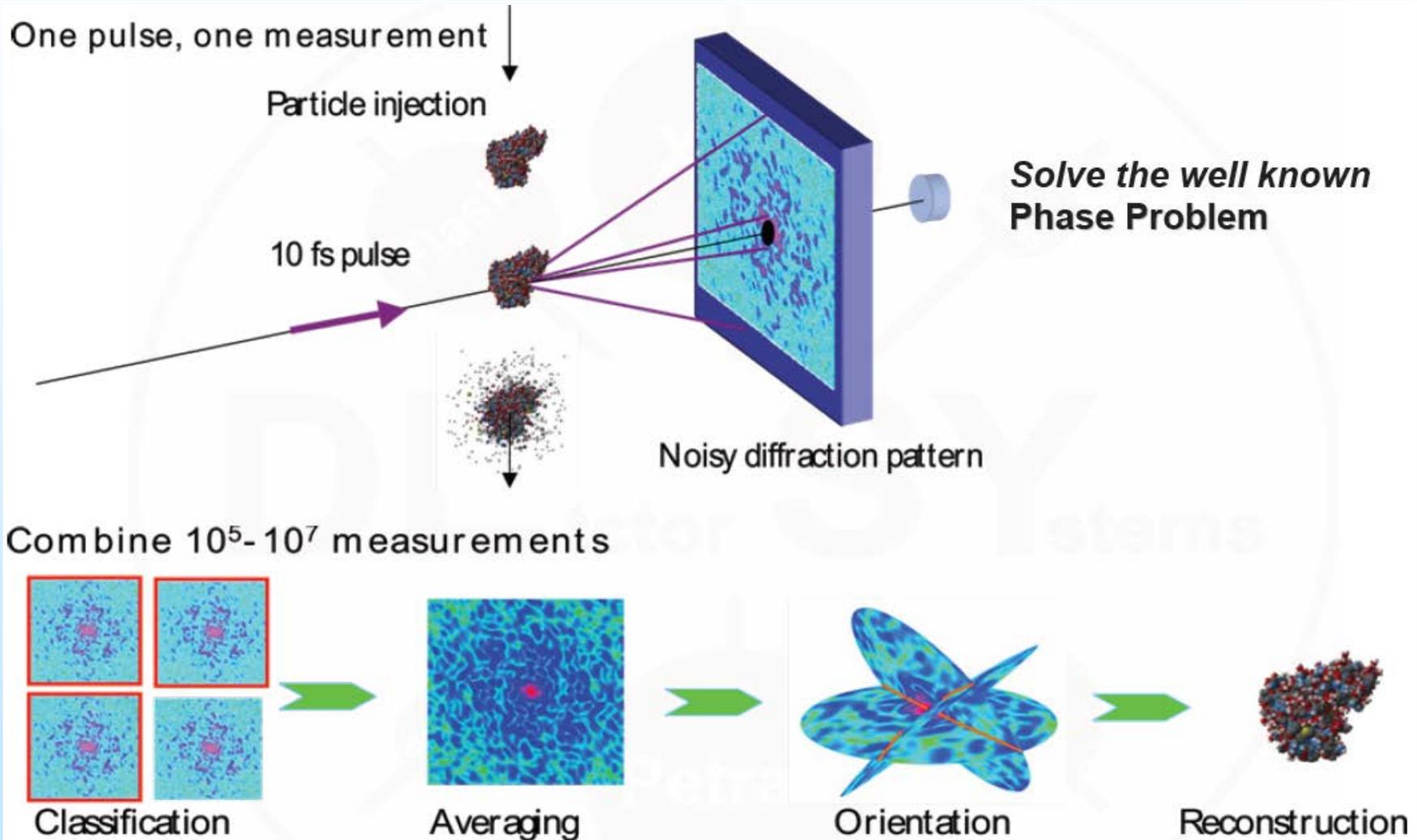


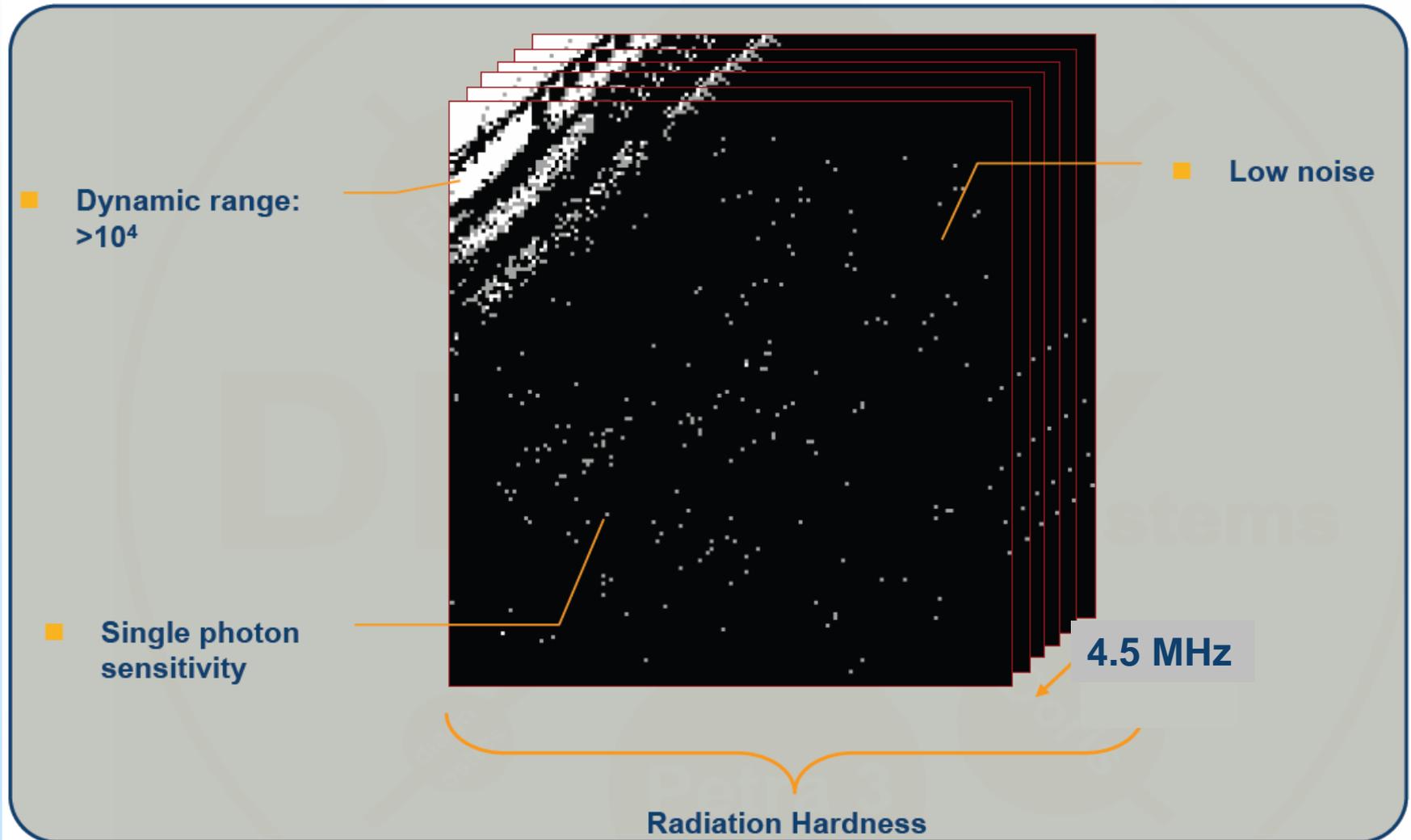
The Adaptive Gain Integrating Pixel Detector (AGIPD) Project

Heinz Graafsma, DESY
on behalf of the AGIPD-Consortium

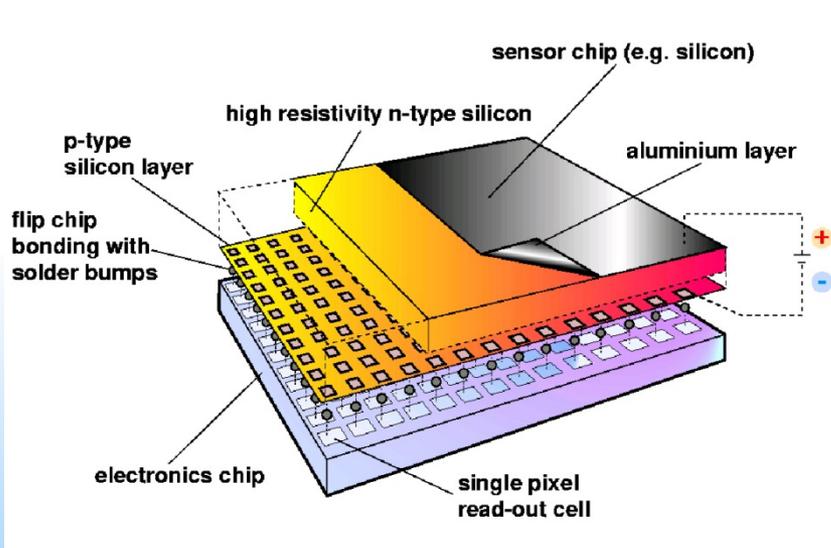
What is the Goal ?



What are the Challenges ?



Hybrid Pixel Array Detectors

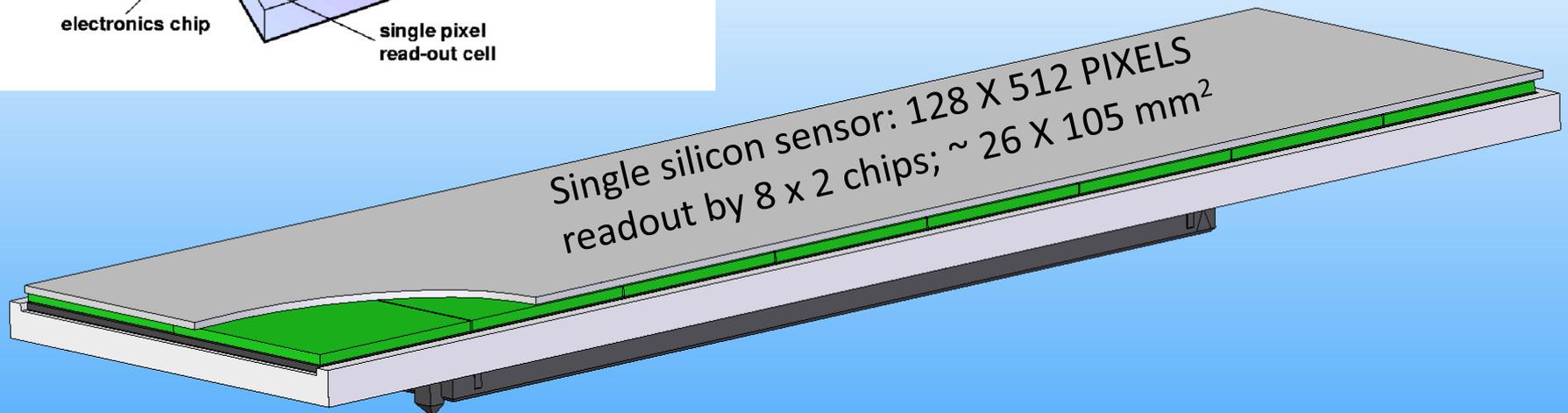


Pixellated Silicon Sensor:

absorbs photons and produces electrical signal

Pixellated readout chip (ASIC):

Processes signal produced in sensor and sends data out



Chip carrier board to talk to and readout chips

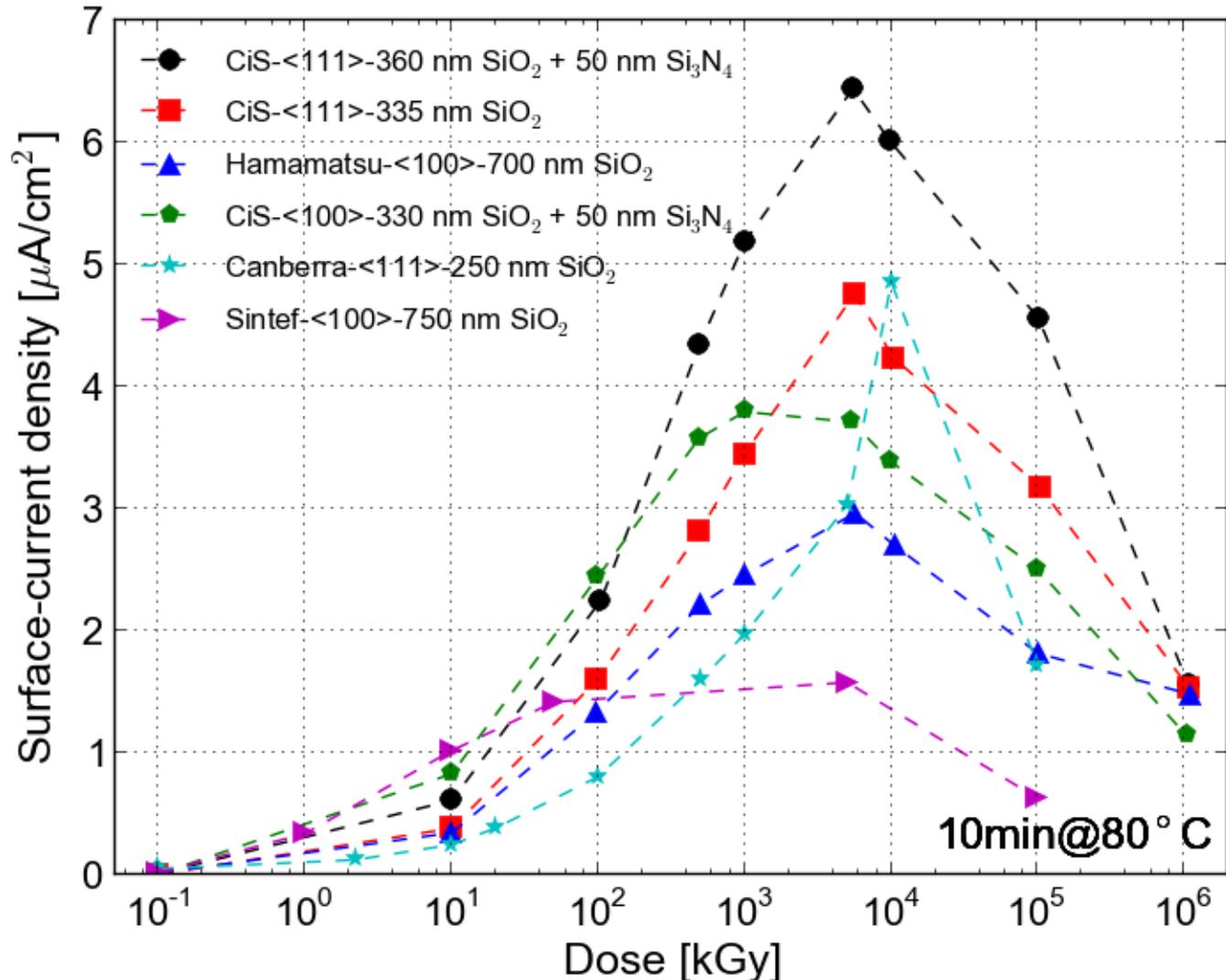


- No bulk damage expected for 12 keV (<300 keV)
- Surface and interface damage:



- Higher leakage current

Radiation hardness sensor





- No bulk damage expected for 12 keV (<300 keV)
- Surface and interface damage:



- Higher leakage current
- Higher depletion voltage
- Lower breakdown voltage
- Charge losses at interface
- Increased inter-pixel capacitance

Special high voltage design:
withstands 10^{16} photons
(= 1 GGy)

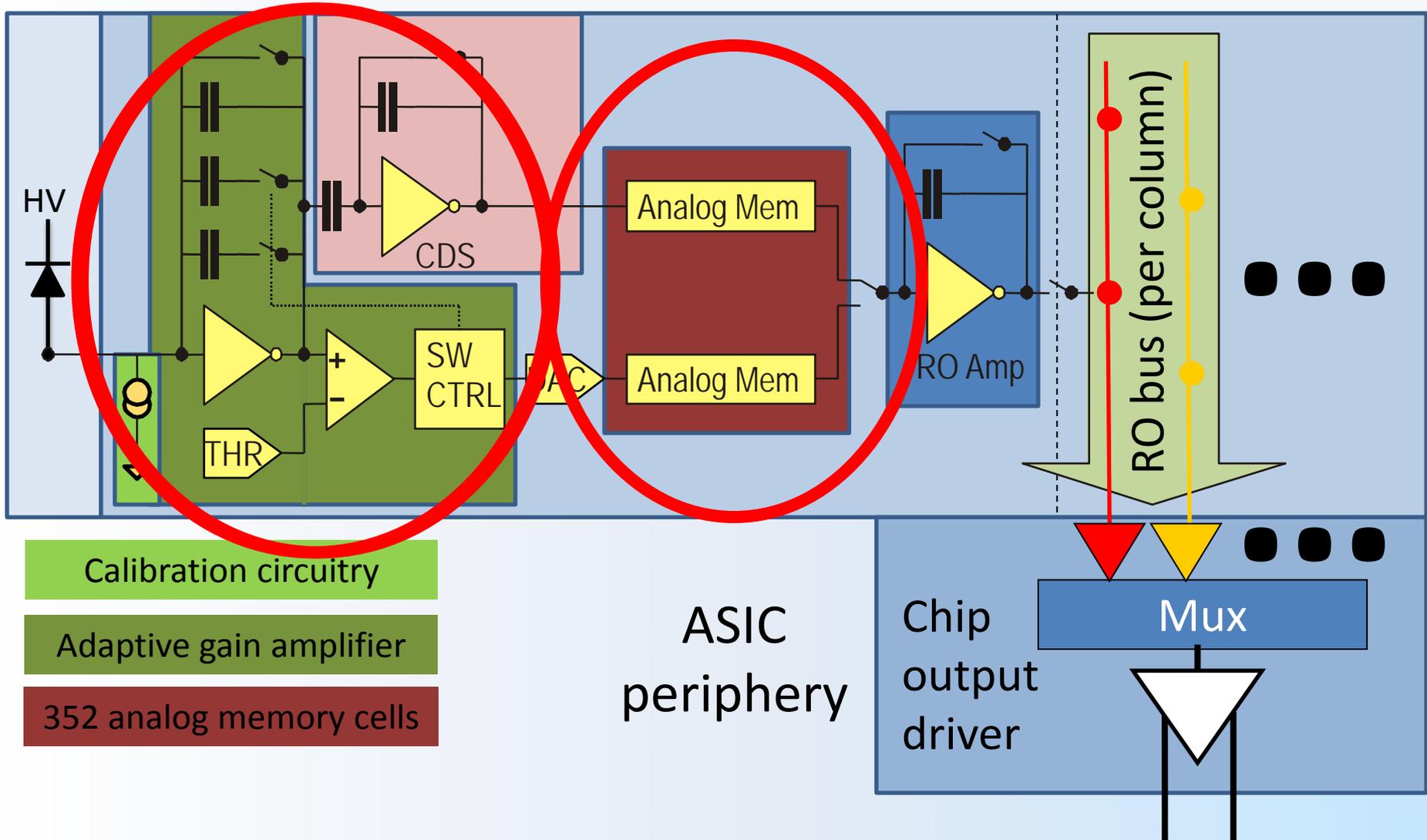
The AGIPD RO-Principle



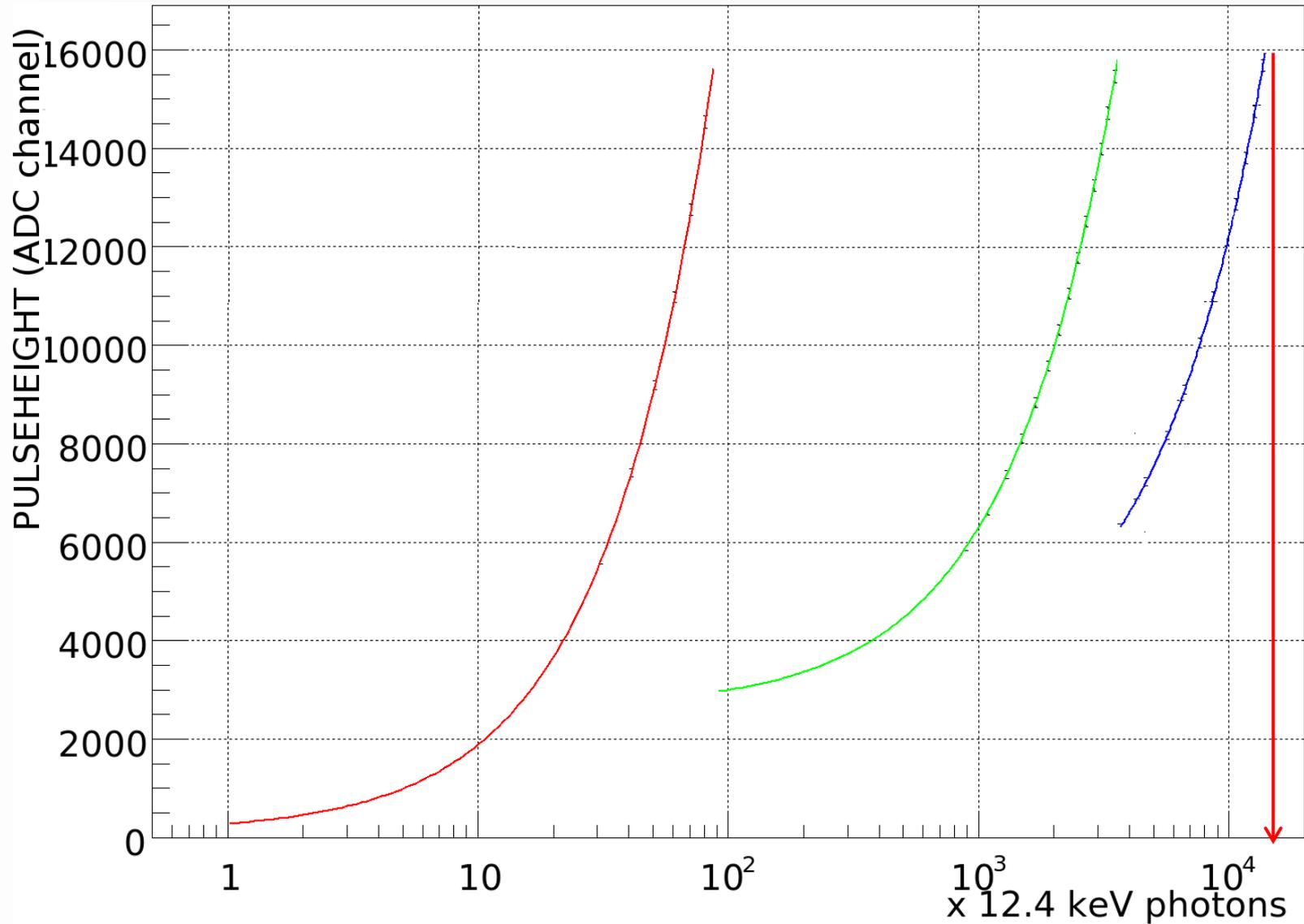
Sensor

Electronics per pixel

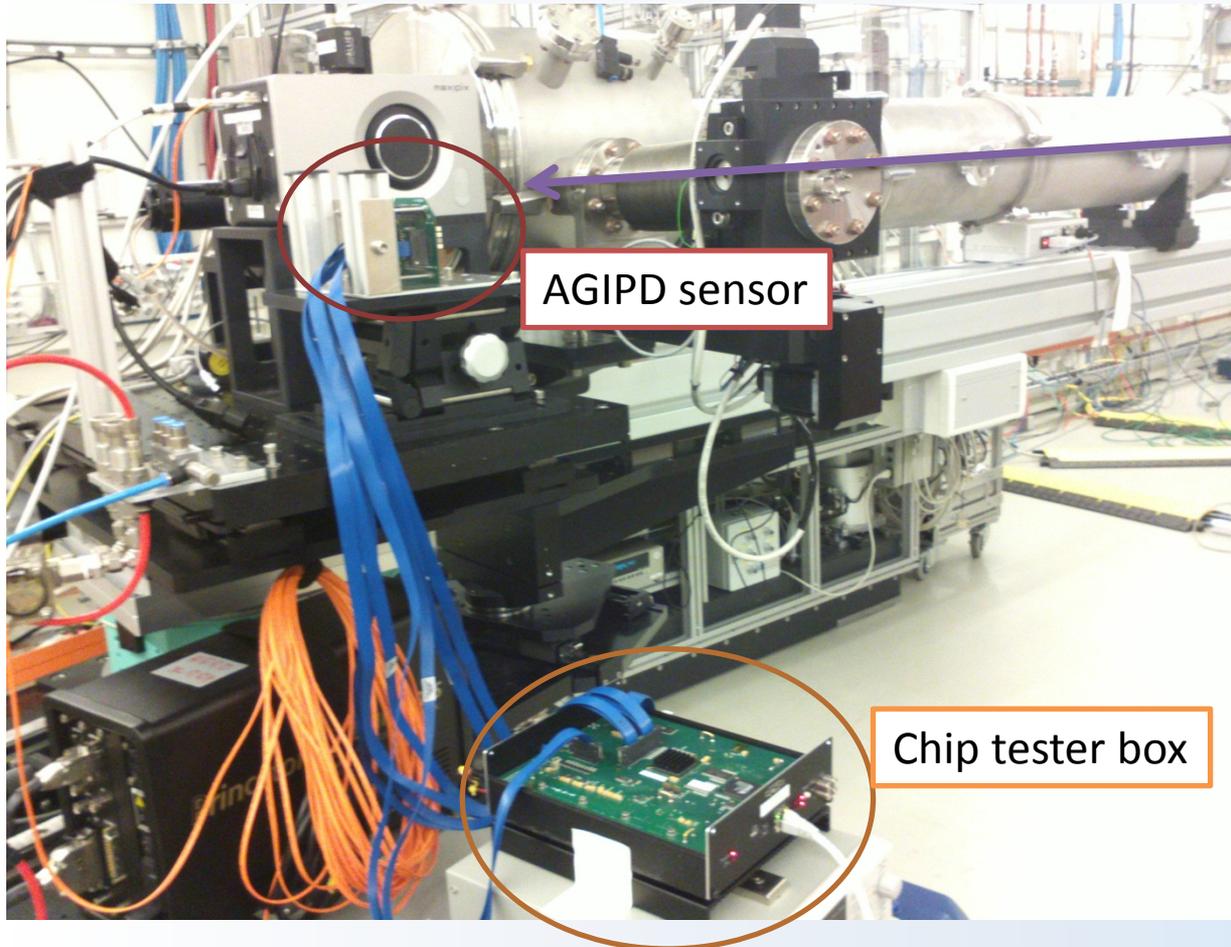
Pixel matrix



Dynamic Range



At the P10 beamline

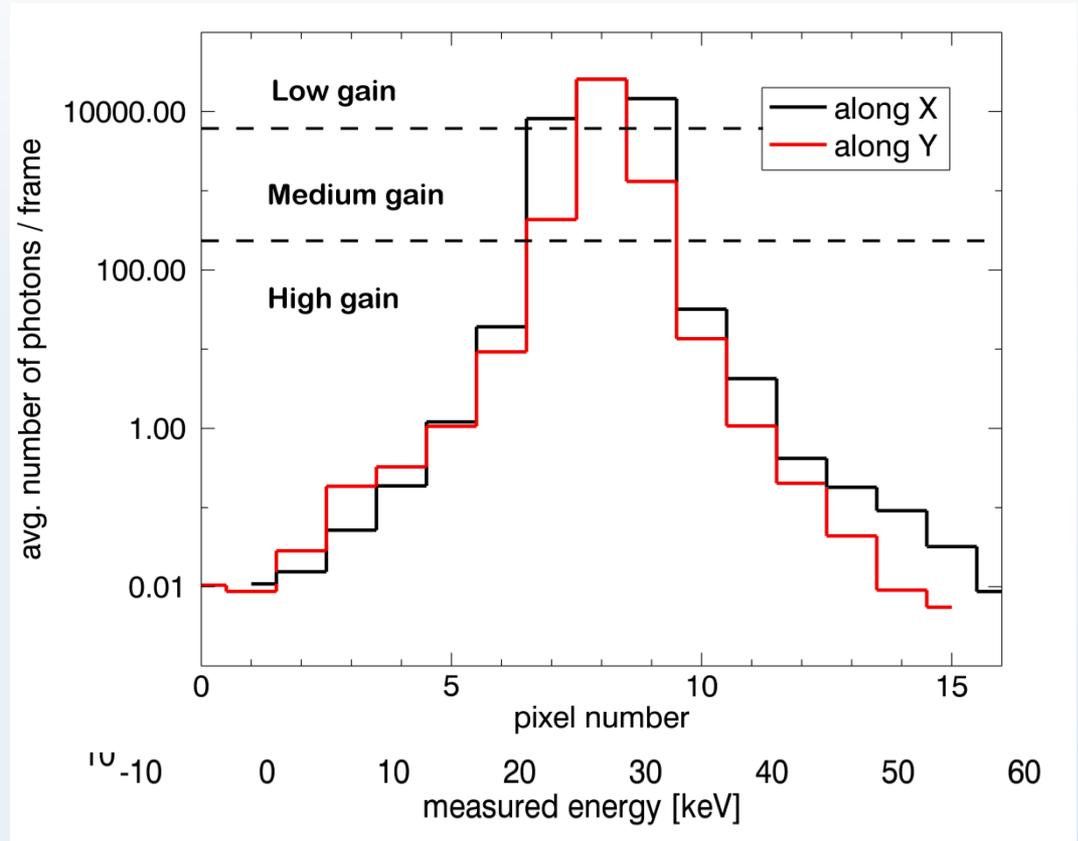
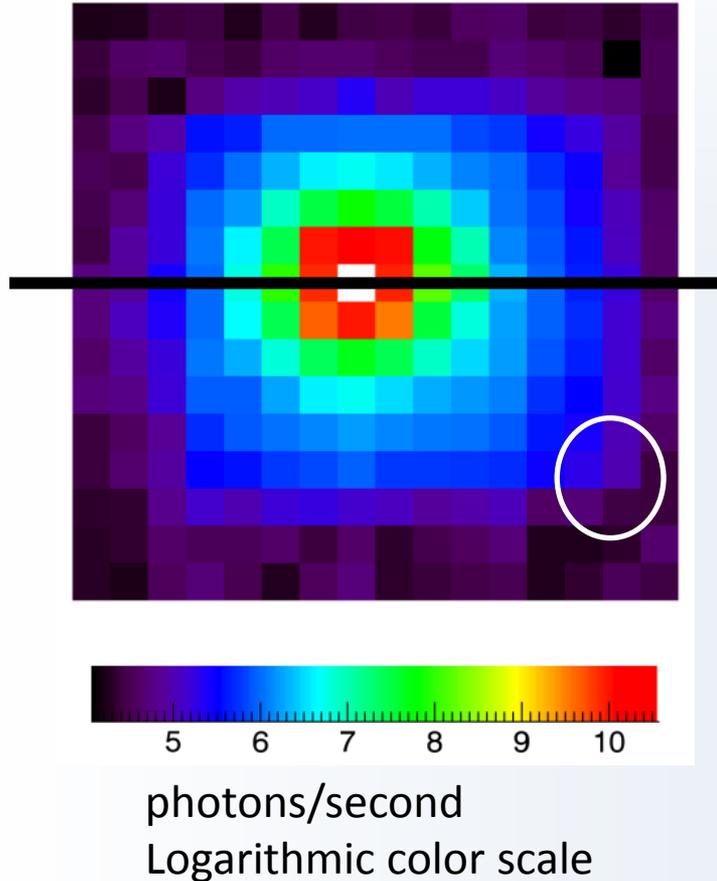


Beam direction
(coming from sample)

It took about 1 ½
hours to set up, after
about 2 hours we saw
the first image

Not in the picture: Sample,
Alexanders PC, people, ...

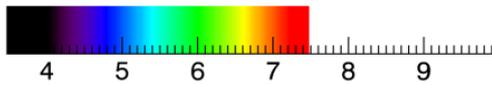
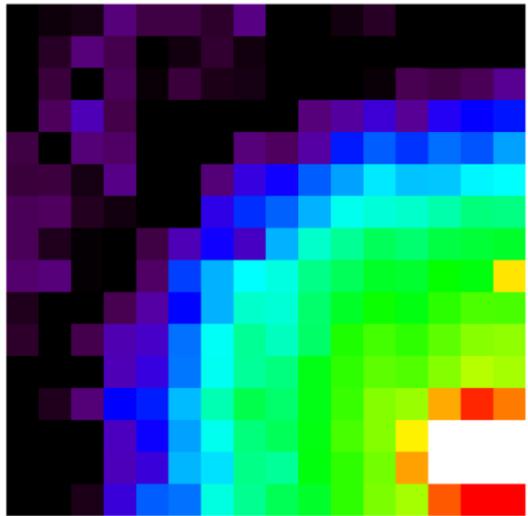
Looking at the direct beam



Gain switching experimentally proven

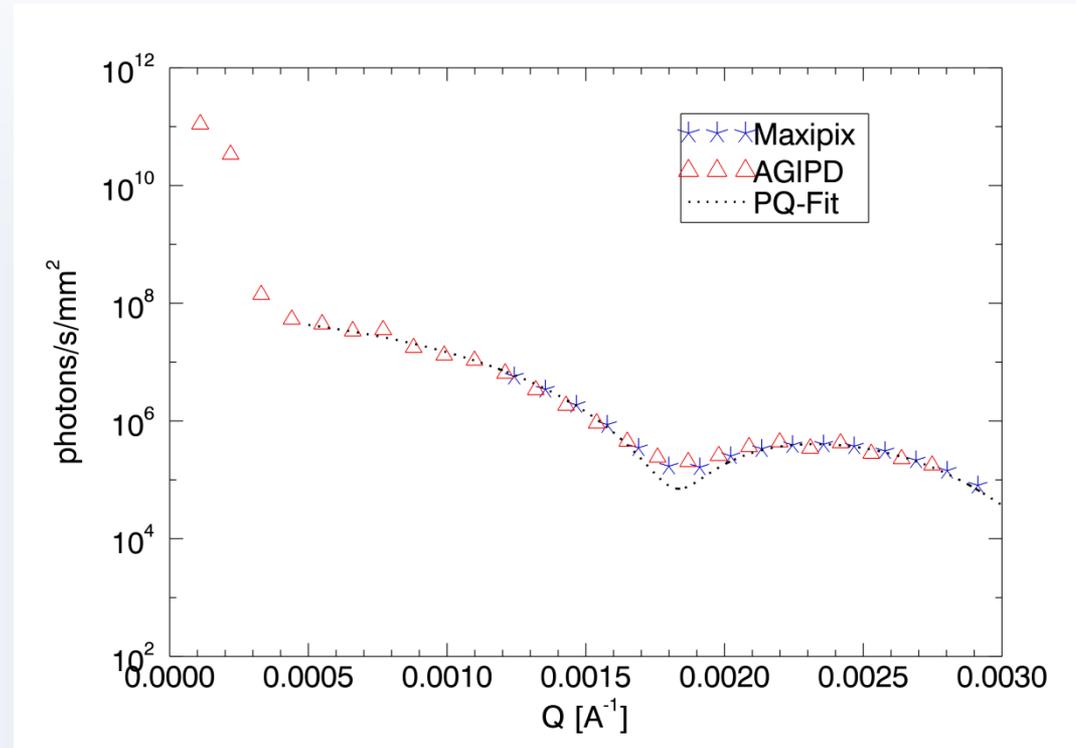
- 10^4 photons / pulse
- Single photon sensitivity
- 4.5 MHz frame rate

Some XPCS measurements



photons/second

Logarithmic color scale



Scientific quality data obtained

- Complete system proven to work
- Calibration proven to be adequate

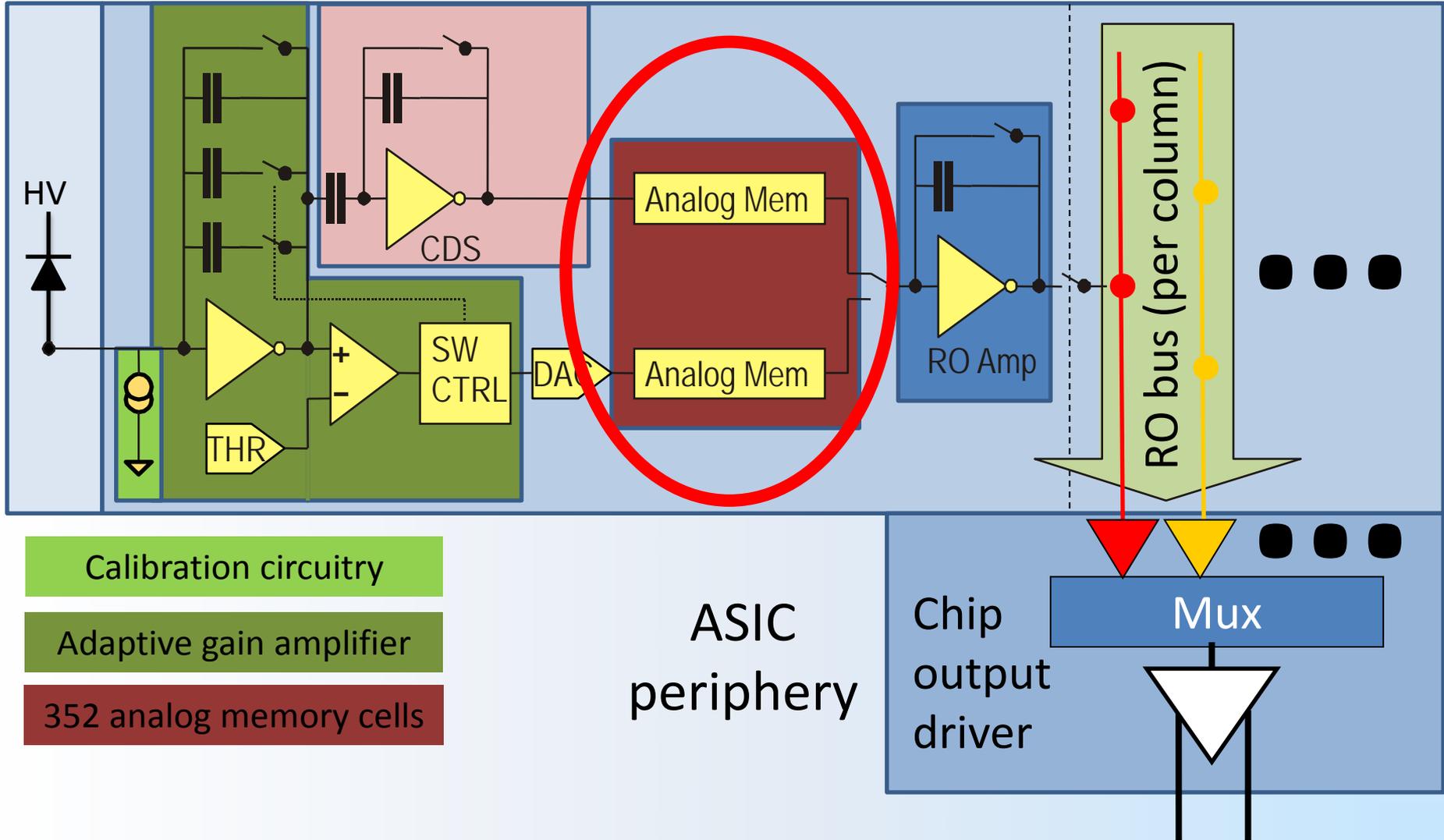
The Analogue Storage



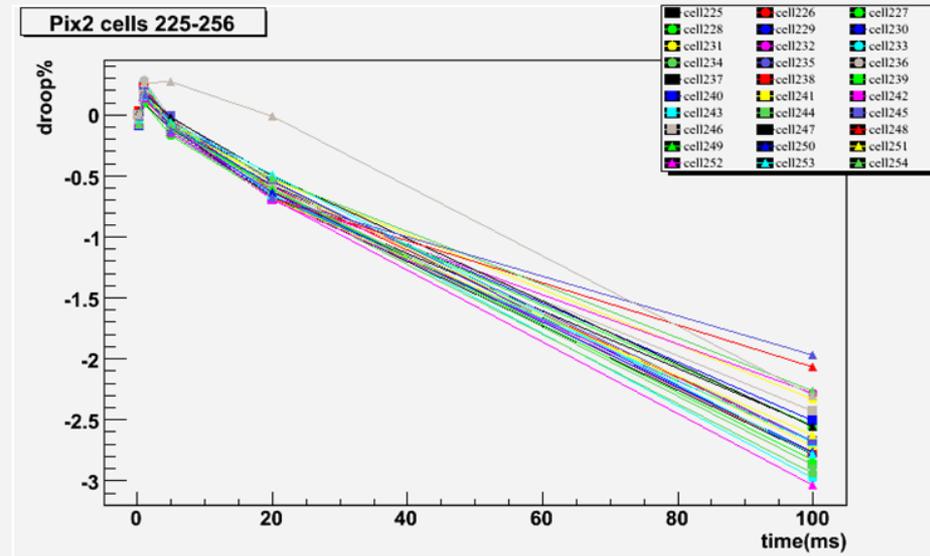
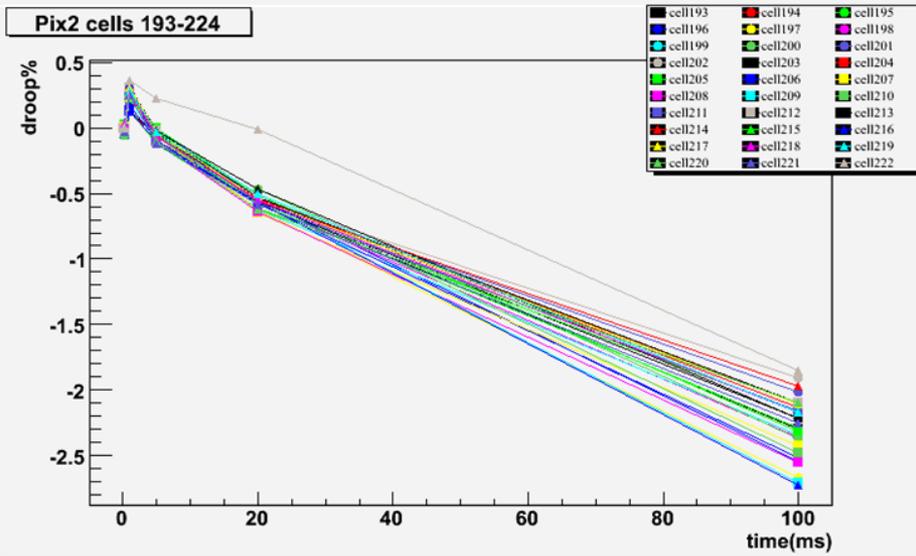
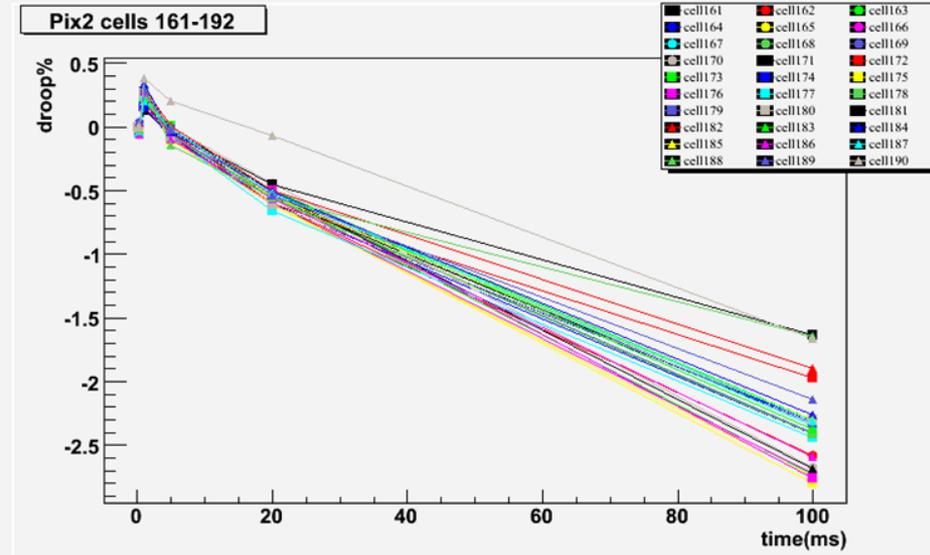
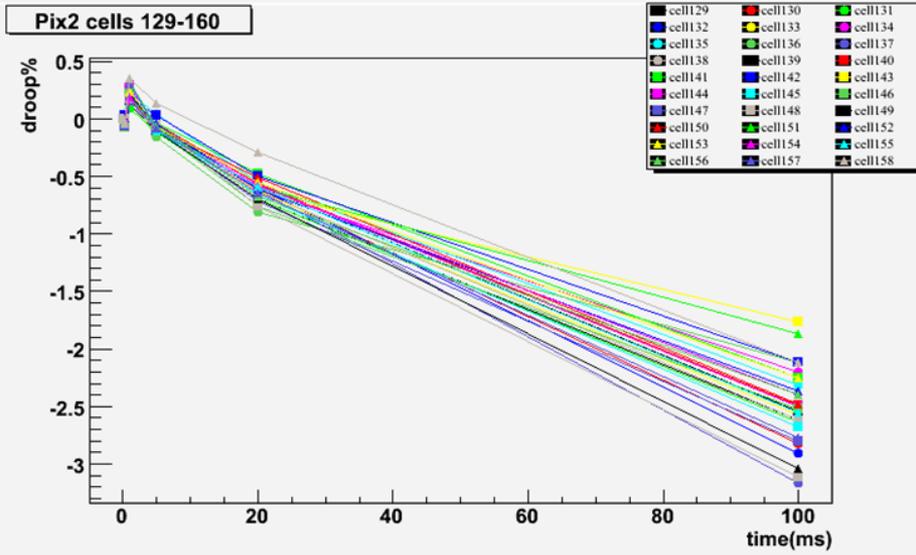
Sensor

ASIC per pixel

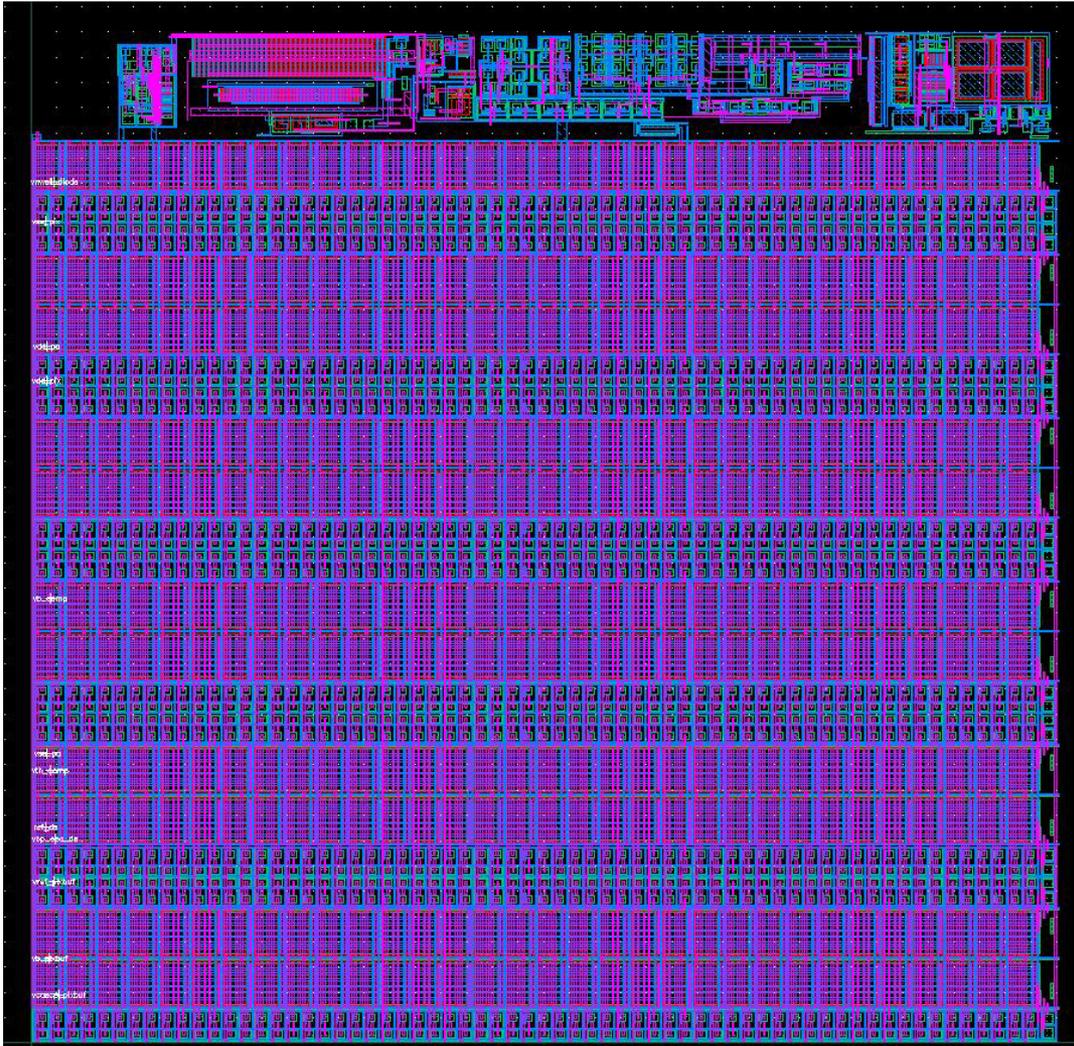
Pixel matrix



Drop curve: Pix 2 cell 128-256

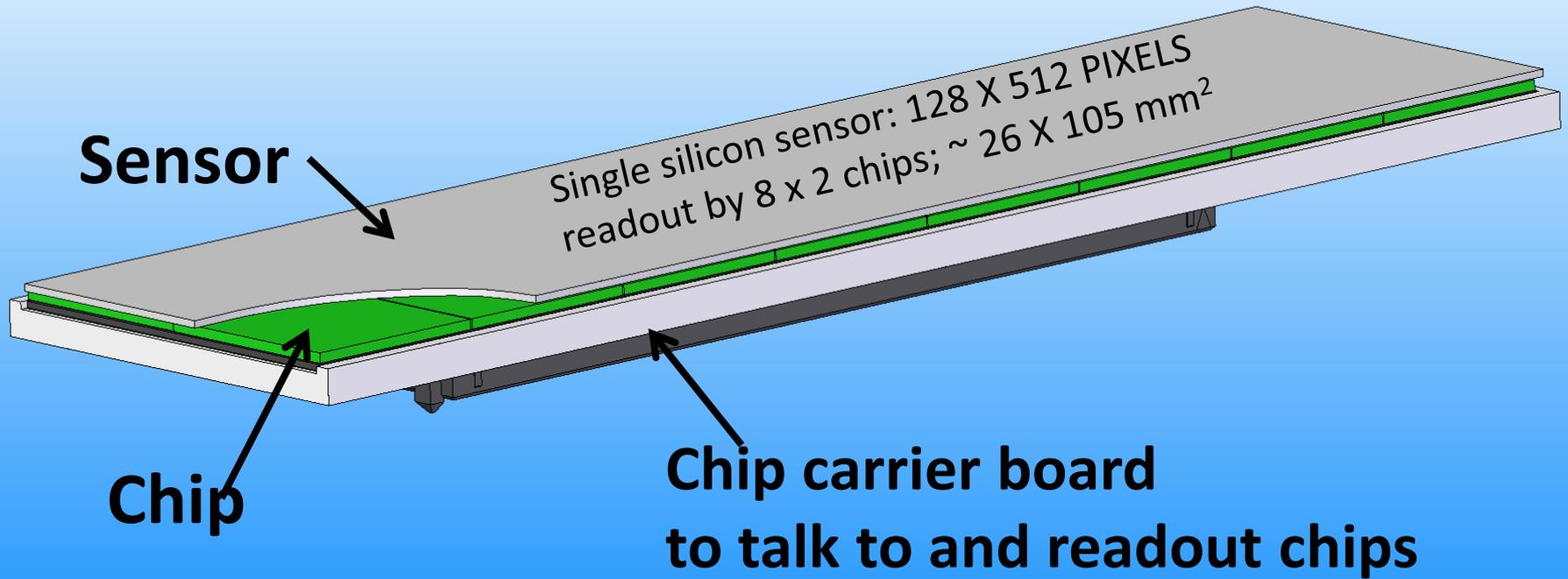


AGIPD 1.0 Pixel electronics

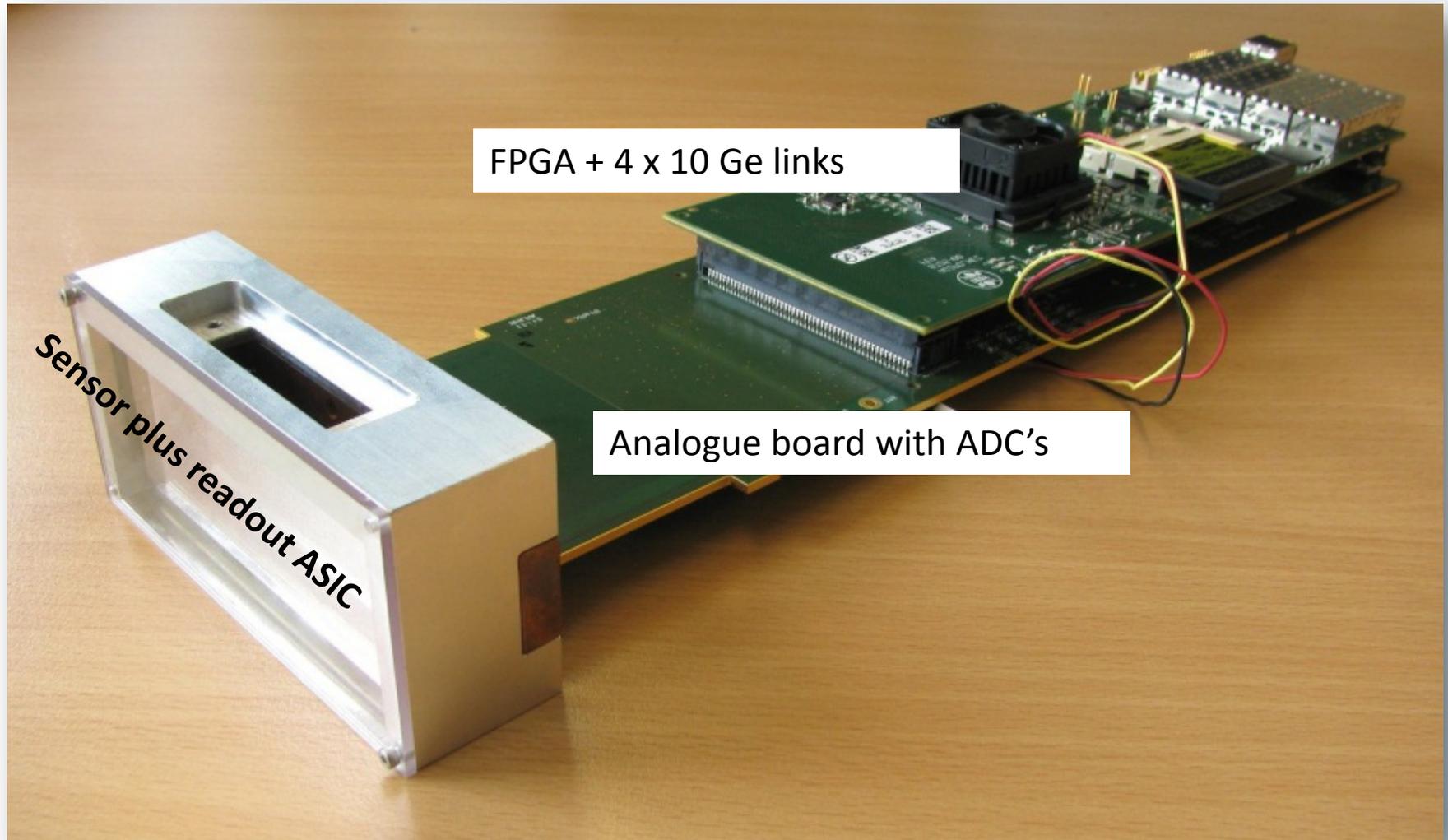


- 200 x 200 micron² pixels
- 352 storage cells + veto possibilities.
- Minimum signal (noise) = 330 electrons = 0.1 photon of 12 keV
- Maximum signal = 33 10⁶ electrons = 10⁴ photons of 12 keV
- 4.5 MHz frame rate
- 64 x 64 pixels per ASIC
- 2 x 8 ASICs per module (128x512 pixels, no dead area)
- 4 modules per quadrant

The front-end



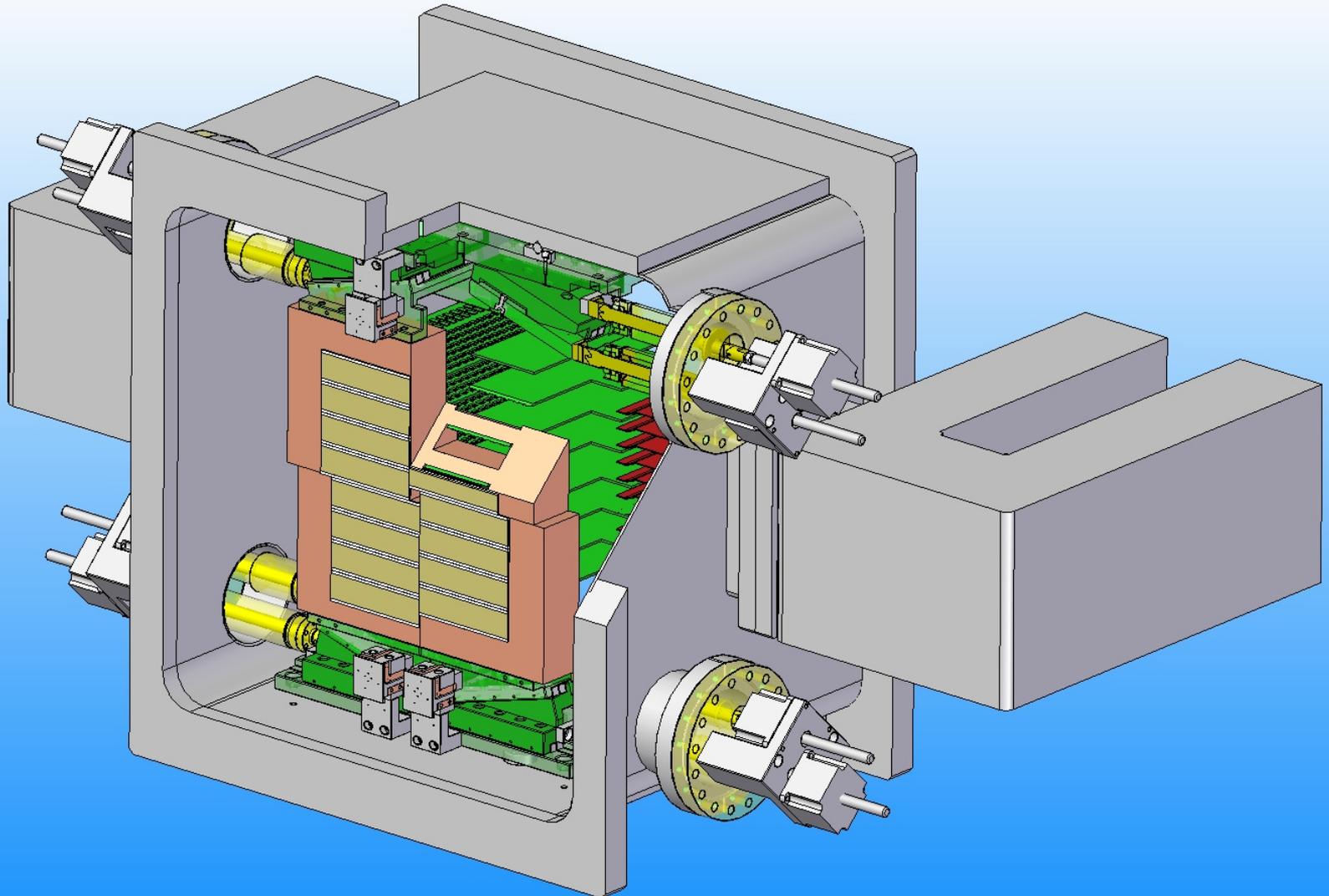
The module building block



FPGA + 4 x 10 Ge links

Analogue board with ADC's

Sensor plus readout ASIC





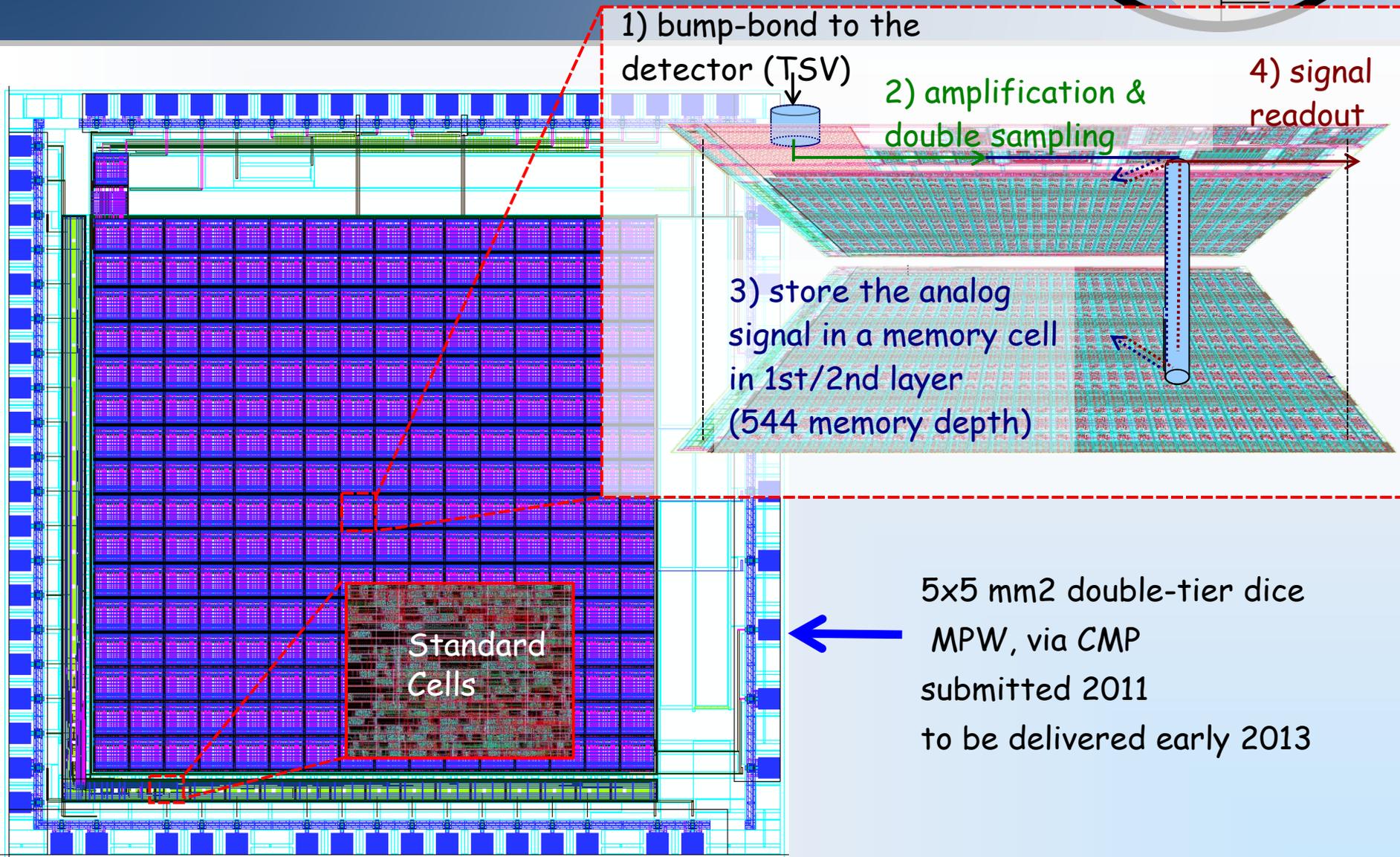
- Sensors are ordered: delivery Jan. 2013
- AGIPD 1.0 in final stage of design: submission coming weeks
- Interface boards designed and ordered
- Single chip assemblies: summer 2013
- First modules (8x2 chips): beginning 2014
- 1k x 1k system(s) beginning 2015

What could be next? AGIPD2?



- Smaller pixels with
 - Reduced dynamic range (no gain switching);
 - Reduced number of frames?
- New Technologies including:
 - 3D CMOS: second layer (more functionality)

3D-CMOS



What could be next? AGIPD2?



- Smaller pixels with
 - Reduced dynamic range (no gain switching);
 - Reduced number of frames?
- New Technologies including:
 - 3D CMOS: second layer (more functionality)
 - 65 nm CMOS technology (more functionality)
 - 3D CMOS + 65 nm CMOS

Who are the People ?



DESY

Julian Becker

Laura Bianco

Peter Goettlicher

Heinz Graafsma

Helmut Hirsemann

Stefanie Jack

Alexandre Klyuev

Sabine Lange

Alessandro Marras

Bjoern Nilsson

Seungyu Rah

Igor Shevyakov

Segrej Smoljanin

Ulrich Trunk

Manfred Zimmer

PSI

Roberto Dinapoli

Doninic Greiffenberg

Beat Henrich

Aldo Mozzanica

Xintian Shi

Bernd Schmitt

Uni-HH

Eckhard Fretwurst

Robert Klanner

Joern Schwandt

Jiaguo Zhang

Uni-Bonn

Markus Gronewald

Hans Krueger

E-XFEL

Jolanta Sztuk-Dambietz