Interface Electronics

Peter Göttlicher

DESY, September 27th, 2012

HELMHOLTZ ASSOCIATION

DESY

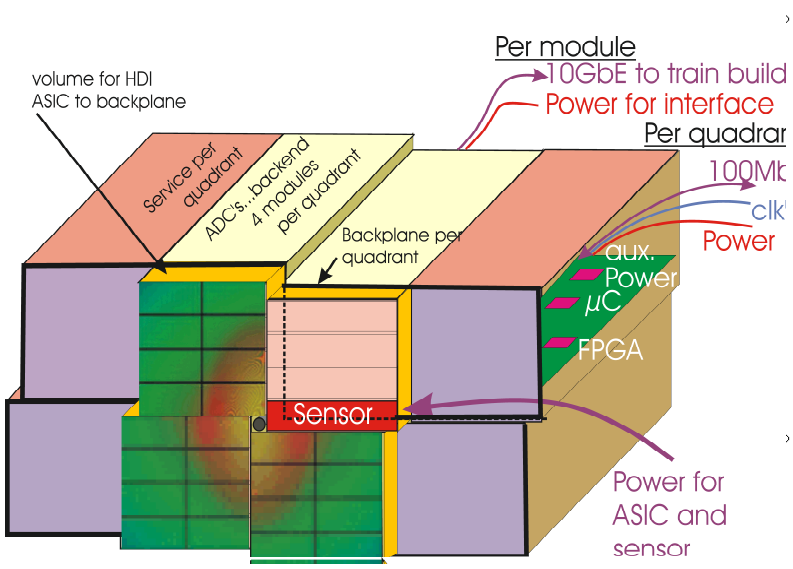
Outline

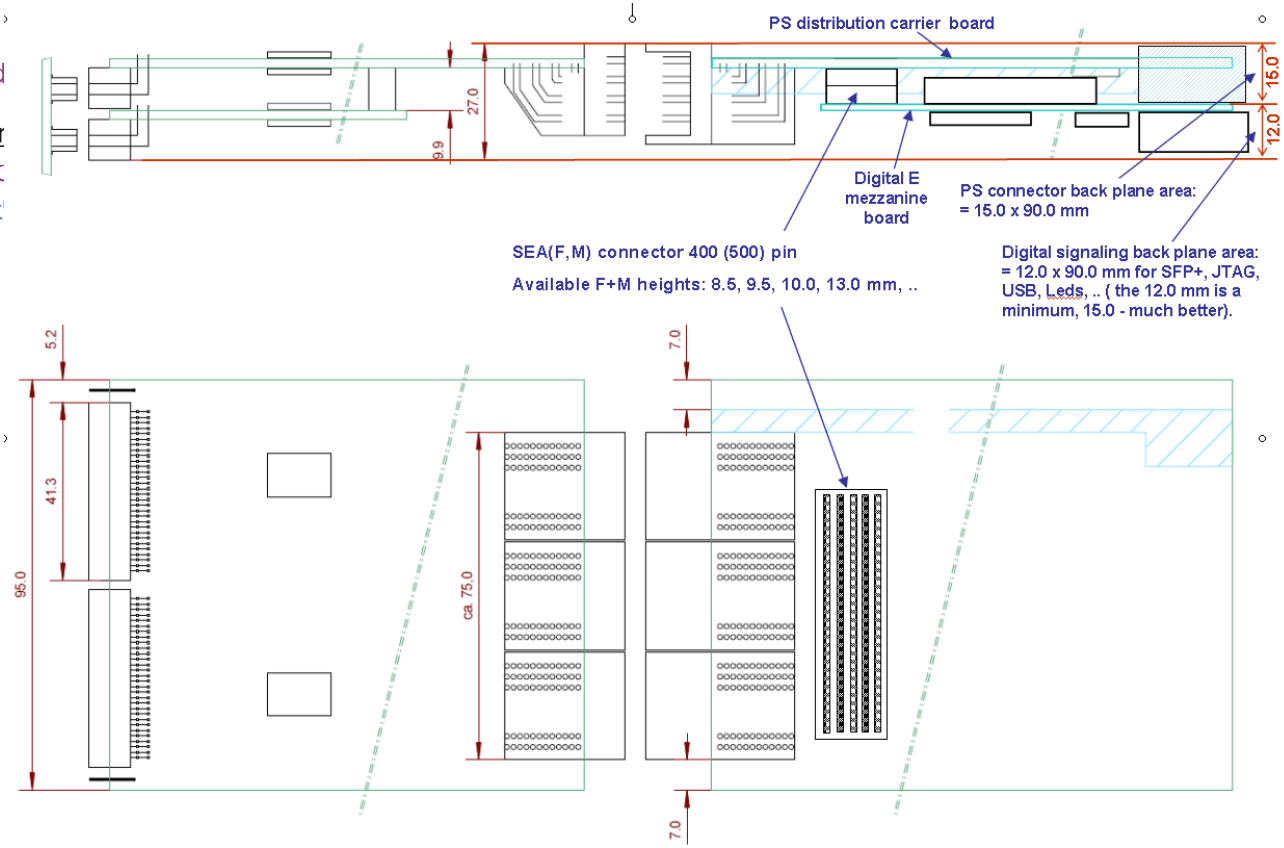
- Up to now constraints
- Digital part
- Analogue part
- Backplane
- Vacuum board
- Quadrants

DESY responsibilities

> Digital part	DESY: FEA-group, M.Zimmer et.al.
> Analogue part	DESY: FEB-group, P.Göttlicher et al.
> Backplane	DESY: FEB-Group P.Göttlicher et. al.
> Vacuum board	DESY: FSDT-Group H.Graafsma et. al.
> Quadrant	DESY: FEA/FEB-groups. …..

Mechanical baseline for the design





Baseline was:

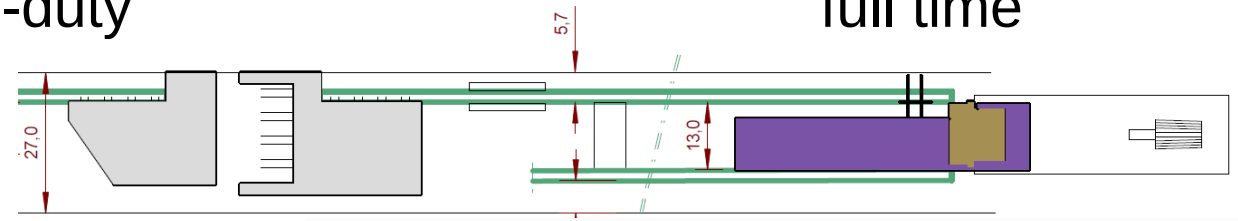
- Everything should fit behind the sensor
- Backplane as vacuum barrier
- Control and ASIC-power from the quadrant

- Two parallel analogue boards
- Rails for guiding the motherboards with a width of 95mm

Digital part

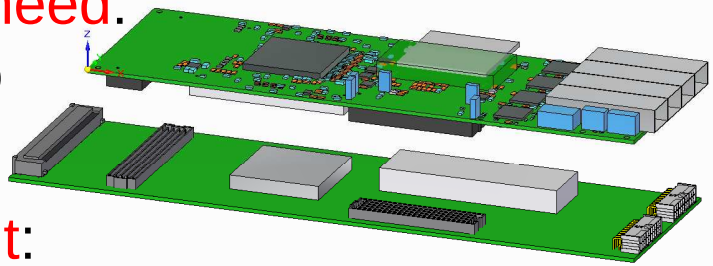
From analogue board:
64x <700Mbit/s = 45Gbit/s
20%-duty

To the DAQ: 10GbE
4Gbit/sec
full time



To fit behind sensor
- Small modification reducing from 4x10GbE to one link.

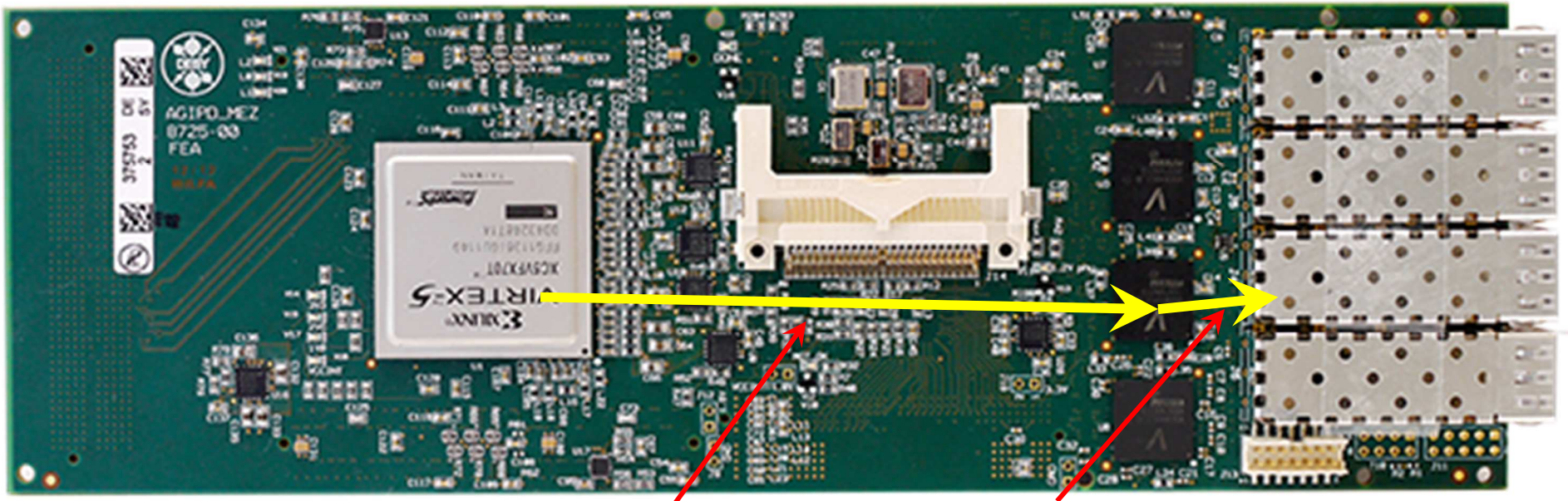
Multiple Pixel-projects need:
Many medium speed to few 10GbE is generic



Facing the development:
⇒ Generic complex functional mezzanine
⇒ Project specific mother-board for connectivity and infrastructure

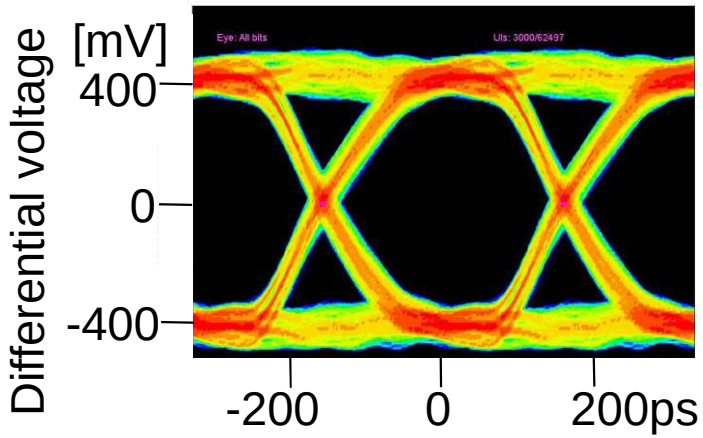
To be done
After vacation.
Is the 95mm width still fine?

Digital part: Performance



No bit errors within a day:
Bit error $<10^{-15}$

Fast Memory Access, OK.



Well open eyes

Coded:

- 10GbE/UDP
- DDR2-Memory Access
- ADC, except small modification for datasheet changes

Backend: Train builder

Developped:
- ATCA @ STFC
- FMC @ DESY-FEA

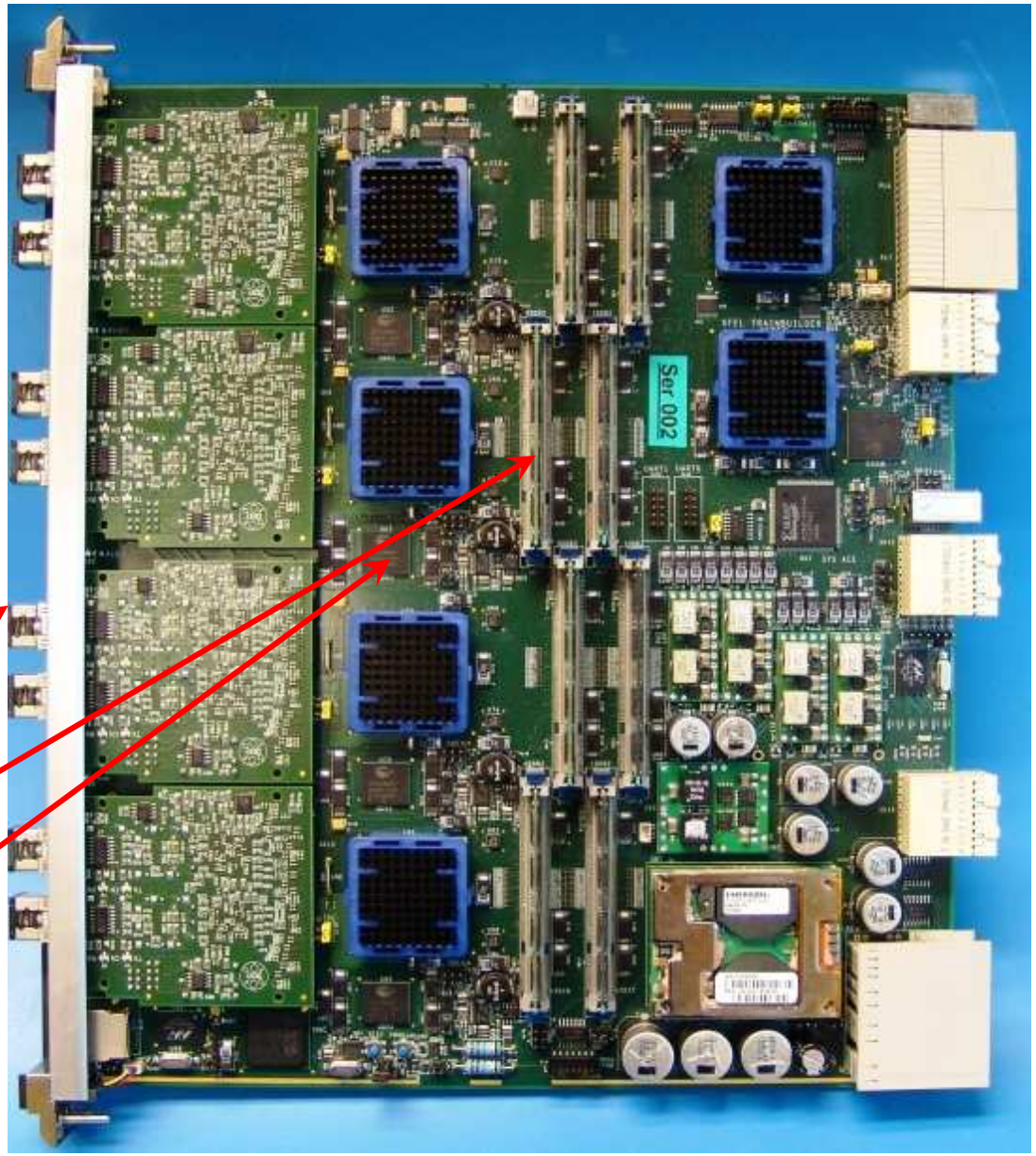
For all XFEL-detectors

First board for testing and
Work on PC connection
@ XFEL

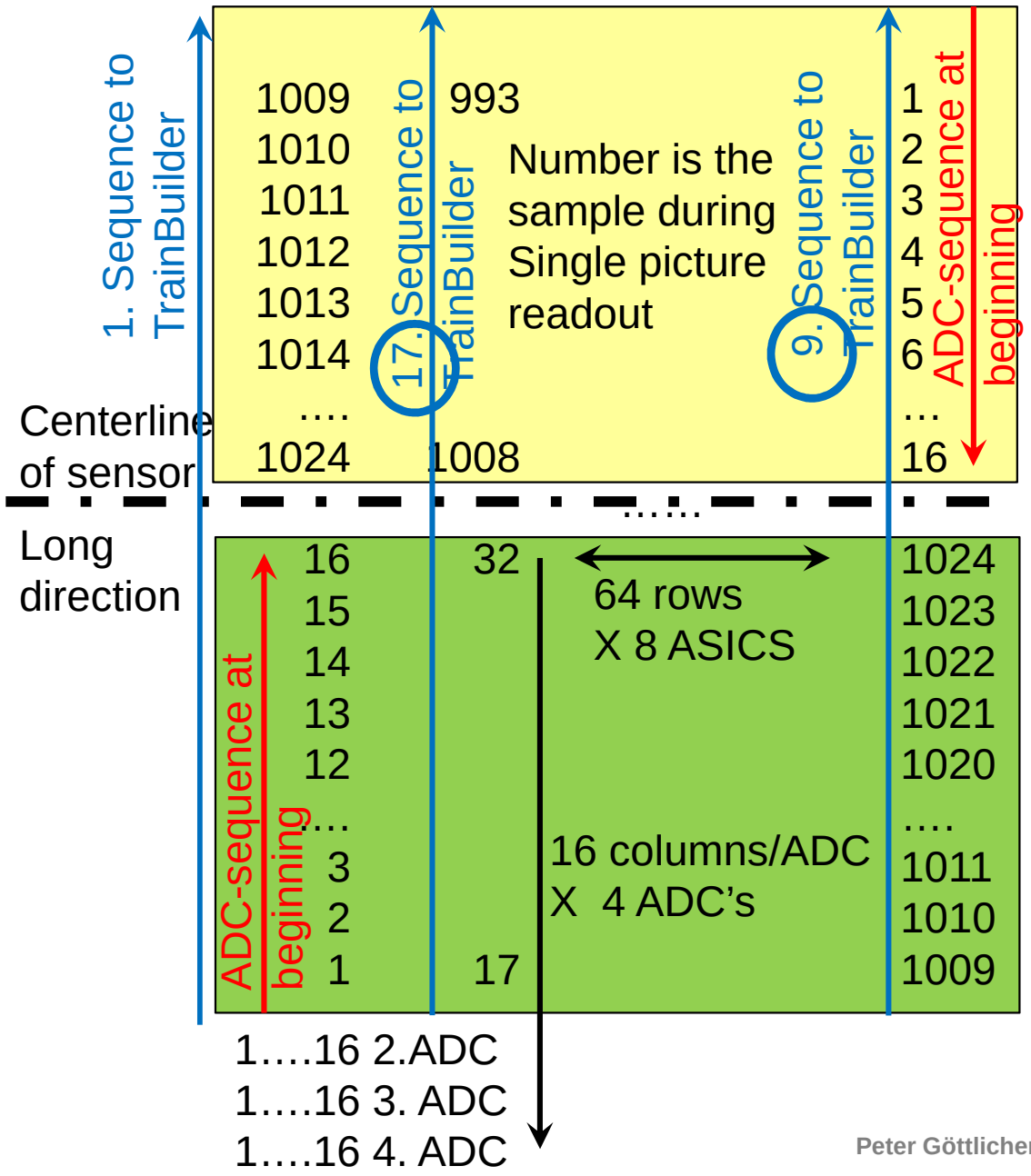
Links for 8 Frontends,
½ of 1-MegaPixel
or 8 outputs

DDR2- SODIMM
for trains

QDR-II SRAM
e.g. geometry sorting



Train builder: Requests presorted geometry



While digitizing

1. Writing a block of
   16 pixel x 64ADC's to DDR2
   (Remember: 128Data-bus,~40Gbit/s)
2. Gains reduce to 5..8 bits (debug!)

While reading: (10-Gb/s)

1. Read first 16 samples,128 accesses
2. Read first 16 gains 43 accesses
3. Read top last 16 samples
4. Read top last 16 gains

Intermittant reduces gains to 2 bit
(Radiation aging!?!, DDR2-access)

5. Send a strip of 128 Pixel

6. second/second-last, 3rd, 4th …..32nd

Column order: Very left of all ASIC's, very right, moving to center of ASIC

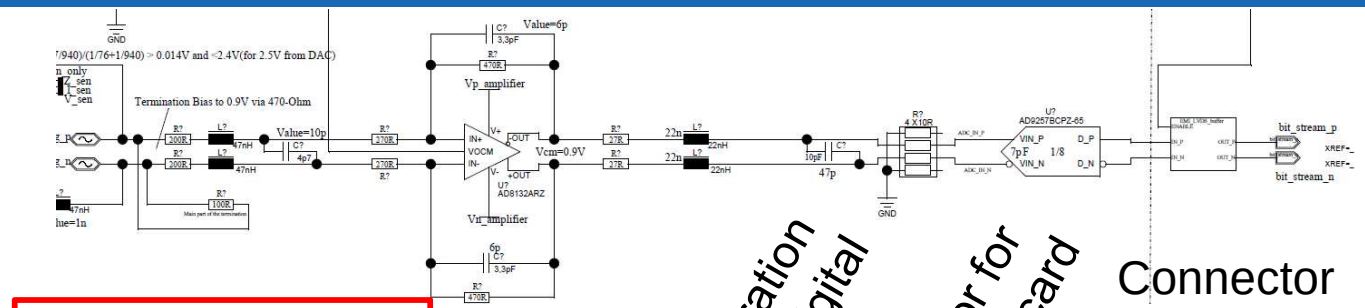
128 pixels in sequences look feasible
More I don't like to promise.
512 pixels look awful on BRAM
- Not final !

Analogue Part

Board width "NOW"
- Active within 80mm
- Graphic 85mm

Will increase to 95mm
- EMI strips to mechanical rails
- New mechanical constraints?

Board length:
- 30 cm allowed
- Likely to get shorter
- Power giving up to gain length? Would fit into 30cm



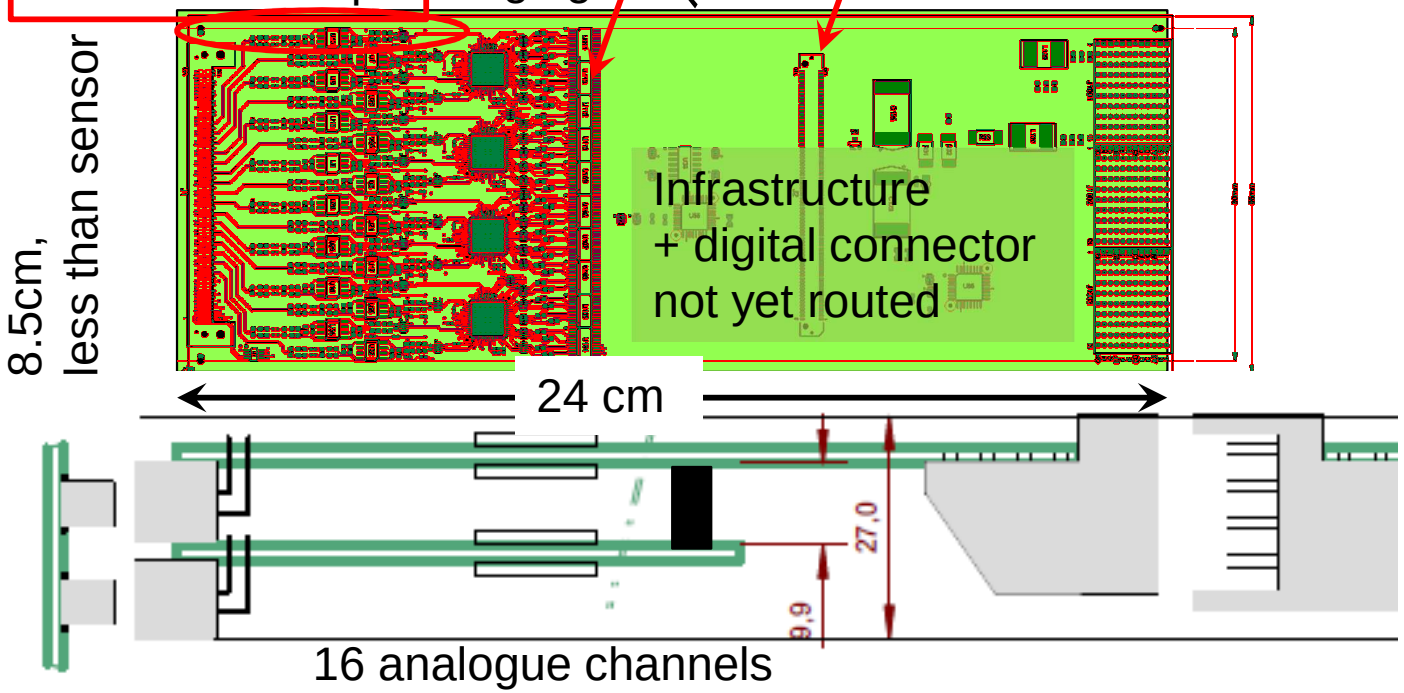
Single channel
- differential filter,
- ADC-adaptation
- 5mm wide strip

14 bit ADC
8-channel
Medical-imaging

EMI-Separation Analogue-digital

Connector for daughter card

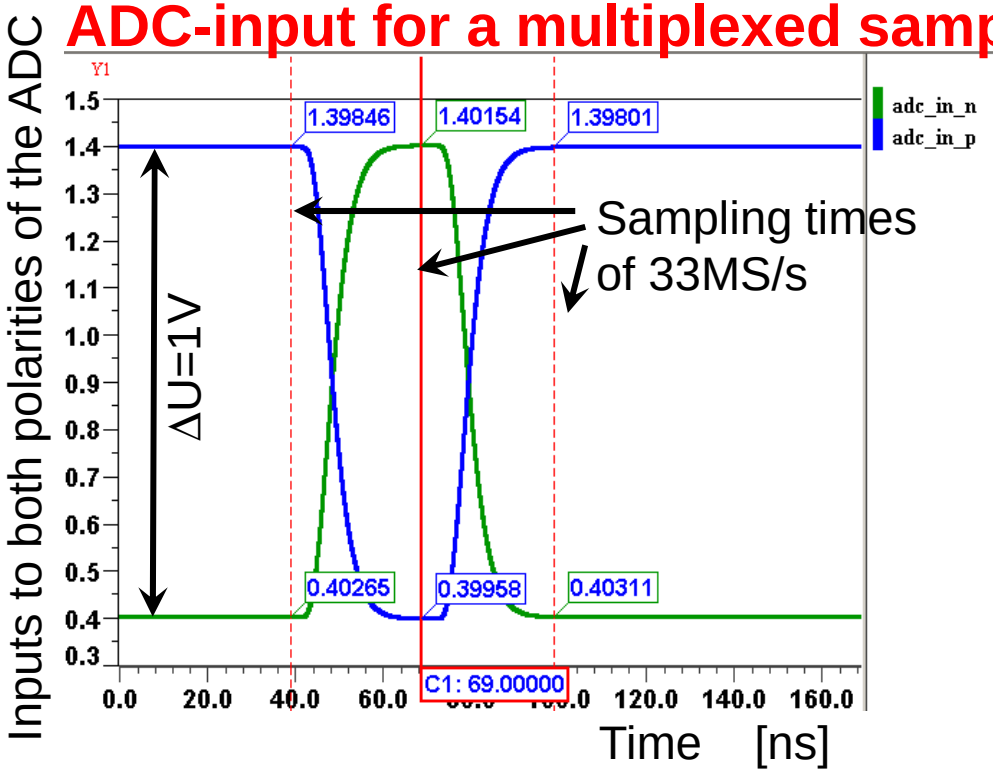
Connector to digital part
64x
<700Mbit/s



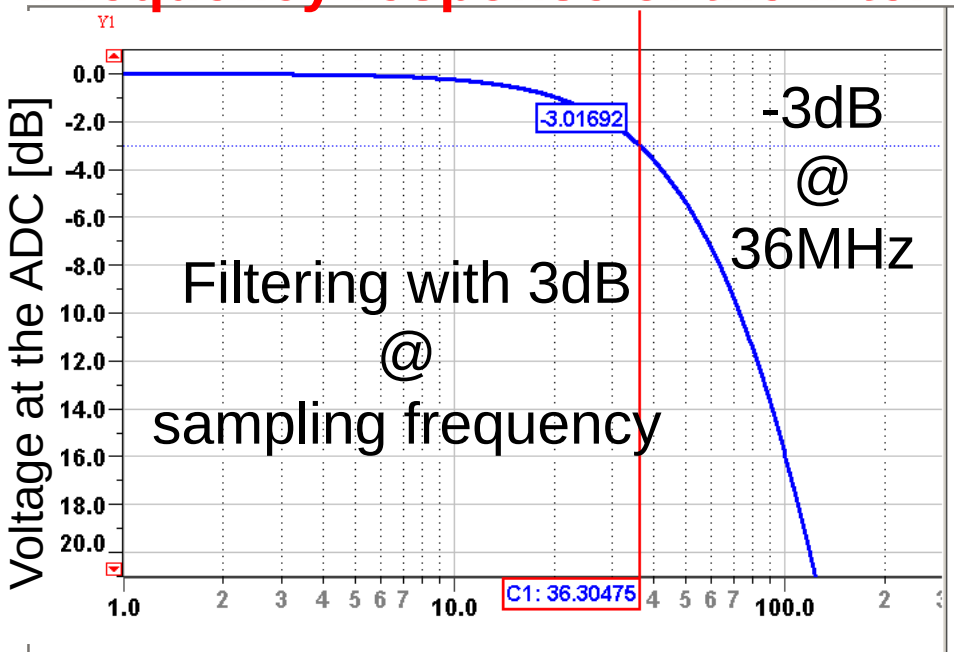
16 analogue channels
on each side of the PCB's
64 channels

Analogue part: Simulated performance

ADC-input for a multiplexed sample

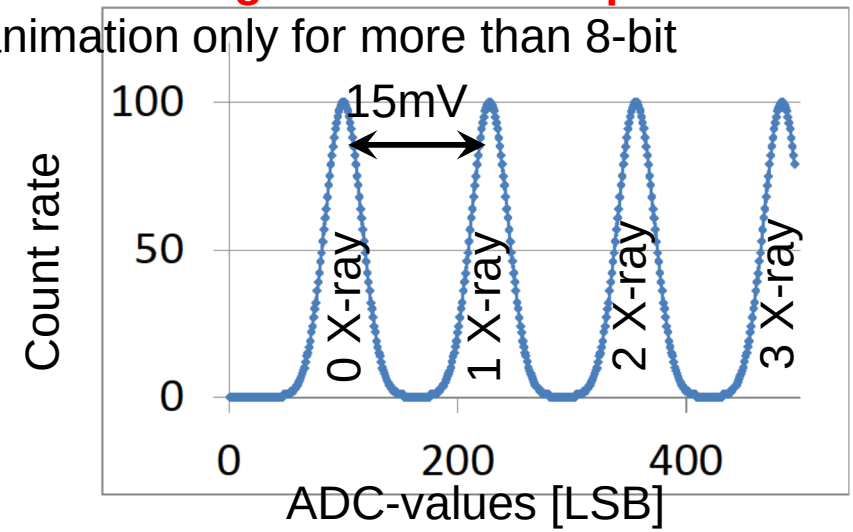


Frequency response of the filter



Aim is to distinguish individual photons

animation only for more than 8-bit



Now Sampling ASIC->ADC: 33MS/s

- Simple $Clk_{System}/3$
- Resynchronized before train
- Continues running train+digitizing
- No data-telegram/strobe for time of phase-Jump to ASIC and digital-part

Analogue part: Status

Mother Board

- Layout for the dense part done
- Infrastructual part will be optimized for space in the circuit diagram
- Layout until end October

That allows to operate ONE row of the 8 ASIC's

Daughter board

- Dense part is reused from mother
- So start than with the copy from Mother while mother is in production

Backplane

What constraints are up to date?

- Vacuum tide burried vias/micro via is not seen as a problem
- SAMTEC would have also a 400-pin or 500-pin SMD-connector right angle.

Need the input from the vacuum board design
Layouter is the same as the analogue boards!

Vacuum board

What are the tasks?

- ASIC-designer requests to have the voltage regulated close to the ASIC's: 16 voltage regulators up to 2A.
- A negative voltage for the ASIC: current, common ?
- A positive voltage for the pixel-input-protection
  Charge/train? Voltage? Current? Common?

- Own monitoring via I2C from quadrant

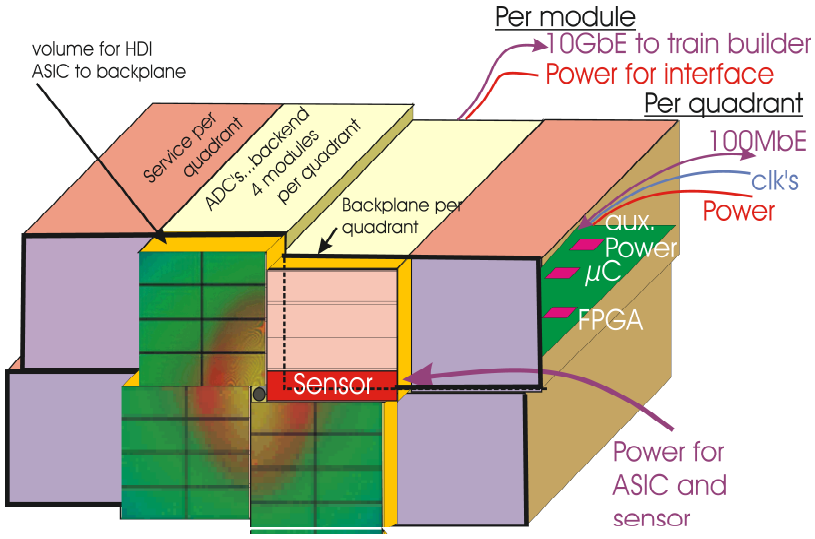
- Three LVDS-line buffering for the ASIC control

- Generating a ASIC-select from commands of I2C
  for booting. While running all in parallel

- Passing the ASIC analogue outs through all that digital/power

Mechanics?

Quadrant



Tasks:

- Power guidance for ASIC's
- Control signals receiver from C&C
- Slow Control receiving from PC

C&C has specified their protocol

- Including a bunch-reject with random time delay
- Based on 99MHz system clock synchronized to the bunches

Prototype will be based on ARM9 and XILINX Evaluation boars.
After settling experience + specifications Development for dedicated geometry.

Summary

- Digital Active board in hand
  Basing blocks for ADC and data link and
  Detector specific blocks getting first ideas, what needed, e.g. sorting
- Digital mother board will be started very soon:
  - Last chance for mechanics constraints changes
  - Baseline: Everything behind the sensor, when going to 1MegaPixel
    rail system with electrical conductive rails
  - Reuse of multi-project digital board only for single module and if more height.
- Analogue Mother board
  - major part is routed
  - Baseline: everything behind sensor with conductive rails
- Analogue daughter will follow
- Backplane needs more inputs and layouter the same as analogue
- Vacuum board, no explicite design started
- Quadrant start with evaluation boards