Towards AGIPD1.0

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Changes arising from the characterization of AGIPD prototype chips

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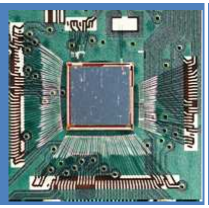
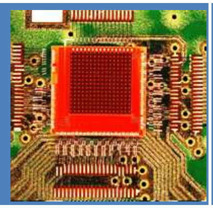
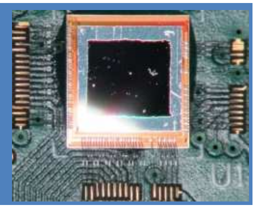
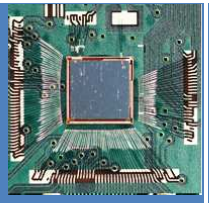
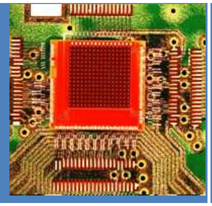
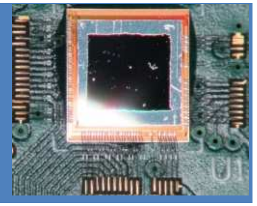
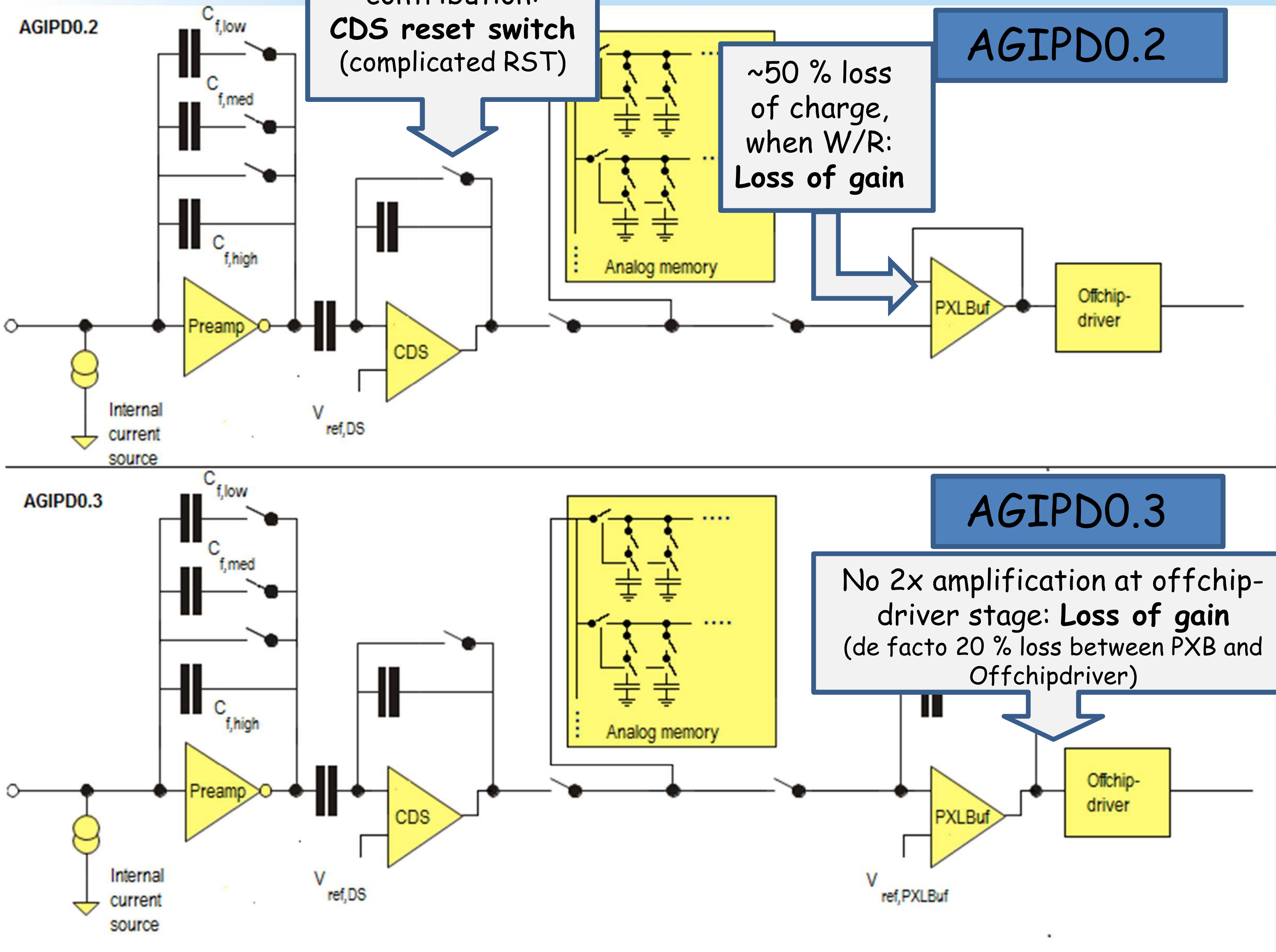
The AGIPD prototype chips

	AGIPD 0.2 	AGIPD 0.3 	AGIPD 0.4 
Properties	- **Pixel matrix:** 16 x 16 / **Pixel size:** 200 um x 200 um - **Dynamic gain switching with three gain stages**: **High** ($C_{f,high}$= 100 fF / 60 fF for some pixels in AGIPD0.4) - **Med** ($C_{f,medium}$=3 pF) - **Low** ($C_{f,low}$= 10 pF)		
Preamplifier	-'**Standard** preamp[1]' -'**Fast** preamp[2]' -'**Standard** preamp' with **protection diode** between the input and VDD ---------------------------- [1] CMOS inverter with a DC gain of ~20 [2] As 'standard', but twice the channel width with respect to standard preamplifier → faster, drags higher current	- '**Standard** preamp' - '**Fast** preamp'	-'**Standard** preamp' with either **60 fF or 100 fF** feedback capacitance - '**Standard** preamp' with **protection diode** between the input and VDD (100 fF) - 'Standard preamp' with a **pmos protection switch** (100 fF)
CDS stage (correlated double sampling)	**Operational amplifier with capacitive feed-back**, AC coupled to preamp: $C_{coupling}/C_{f,CDS}$=2 - Rather complicated reset scheme to remove the offset of the opamp	**Operational amplifier with capacitive feedback**, two different options of AC coupling to preamp: $C_{coupling}/C_{f,CDS}$=1 and 2 - Simple reset switch	**Operational amplifier With capacitive feed-back**, two different options of AC coupling to preamp: $C_{coupling}/C_{f,CDS}$=1 and 2 - Simple reset switch

The AGIPD prototype chips

	AGIPD 0.2 	AGIPD 0.3 	AGIPD 0.4 
Storage cells	Two different kinds of storage cells: - **Switches:** Low power pFET Regular VT pFET - ***Capacitor:*** Thick gate nFET - **'Active storage cells'**, buffered in order to keep a zero voltage drop over column switch to reduce leaking	Two different kinds of Storage cells: - **Switches:** Low power pFET Regular VT pFET - ***Capacitor:*** Thick gate nFETs	-**Switches:** Regular VT pFETs -***Capacitor:*** Thick gate nFETs
Pixelbuffer	**Voltage follower**, i.e. voltage sensitive - precharging of parasitic capacitance is necessary with either CDS stage or precharge scheme - readout of pixel possible with directly connecting the readout chain to the pixel buffer	**Operational amplifier with capacitive feedback,** i.e. charge sensitive	**Operational amplifier with capacitive feedback**, i.e. charge sensitive

Status: Noise performance AGIPD0.2 & AGIPD0.3



Main noise contribution:
CDS reset switch
(complicated RST)

~50 % loss of charge, when W/R:
Loss of gain

AGIPD0.2

AGIPD0.3

No 2x amplification at offchip-driver stage: **Loss of gain**
(de facto 20 % loss between PXB and Offchipdriver)

Approach:

Different CDS stage
→**Simple reset scheme**
(From AGIPD0.2)

Charge sensitive pixelbuffer
→ operational amplifier with capacitive feedback
(From AGIPD0.2)

Different scheme to drive signals off the chip
→**Column buffers**
(From AGIPD0.3)

Very high gain mode
→$C_{f,Preamp}$**=60 fF**
(From AGIPD0.4)

Summary: AGIPD noise contributions

Component	AGIPD0.2 (std preamp)[a]	AGIPD0.2 (std preamp)[b]	AGIPD0.3	AGIPD0.4 ($C_{f,high}$=100 fF)	AGIPD0.4 ($C_{f,high}$=60 fF)
	10 SCR, 200 ns, $V_{ref,DS}$= 0.6 V	1 SC W/R, 2 µs, $V_{ref,DS}$= 0.6 V	1 SC W/R, 200 ns, $V_{ref,DS}$= 0.5V	1 SC W/R, 200 ns, $V_{ref,DS}$= 0.65 V	1 SC W/R, 200 ns, $V_{ref,DS}$= 0.65 V
Preamp (Reset switch)	153 ± 1 ~~(317 ± 2)~~	212 ± 3	115 ± 3	210 ± 3	150 ± 3
CDS (Reset switch)	251 ± 2 (236 ± 2)	258 ± 3	239 ± 5	221 ± 2	133 ± 2
Readout chain *($PXLBuffer^2$+$Offchip^2$)* (Reset switch)	273 ± 2	561 ± 7	438 ± 7[c] (197 ± 4)	311 ± 1 (191 ± 1)	225 ± 3 (144 ± 1)
Σ (oversampled)	401 ± 2 (281 ± 2)	654 ± 8 (413 ± 5)	512 ± 10 (383 ± 8)	436 ± 1 (394 ± 1)	301 ± 4 (270 ± 3)
Gain (ADC/keV)	16.38 ± 0.10	8.34 ± 0.10	6.09 ± 0.12	11.18 ± 0.02	15.99 ± 0.20

[a,b]Overall noise of standard preamp + protection diode (oversampled): 10 SCR: 438 ± 8 (325 ± 5) | 1 SCWR: 661 ± 8 (422 ± 5)

[c]Noise contributions AGIPD0.3 readout chain: Pixelbuffer= 332 ± 7 | Offchip= 285 ± 6

'Presummary': AGIPD0.4 status

AGIPD

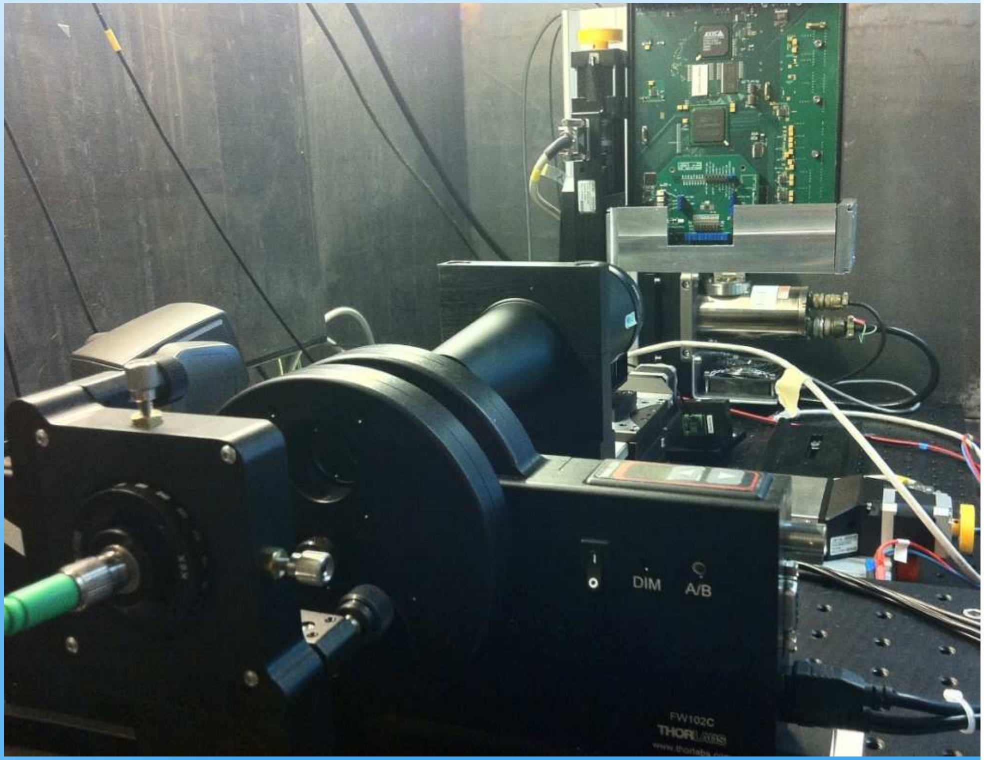
Component	Status	Result
Noise	• C_f= 60 fF • CDS gain HIGH (x2) • Offchip x1.5 decided	Noise (ENC): (301 ± 4) e- (270 ± 3) e- (oversampled) okay !
Protection measures	• Diodes • Nmos switches	Basically decided
Speed (Write to SC)	• (Up to now) Just measured @ 10 MHz not speed optimised	Some changes
Speed (Read from SC)	• (Up to now) Not worried at all about readout speed	Should be fine
Dynamic range	• With CDS gain HIGH and 60 fF: Good linearity up to few 1000x12.4keV bad	…, but we'll make it good!

Protection measures

• Pixel destruction <u>possible</u> with IR laser (1030 nm) at full power and 5 MHz repetition frequency.

→ Probably conducting channel in sensor
(due to interaction depth of IR throughout sensor)

→With bias voltage of 120 V: Pixels die
→ No bias voltage, no dying pixels



• Opens possibility to examine the protection measures…

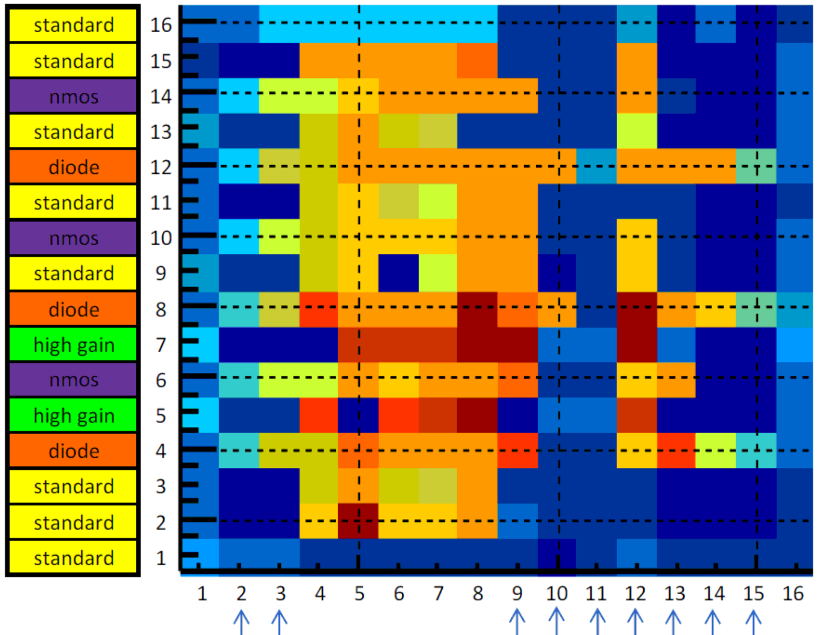
→Worst case scenario: 120 V swing within few ns

→Investigating the ability to destroy pixels for different voltages at protection circuits (Diode, nmos switch)
(Reference is always the standard pixel)

Protection measures

AGIPD0.4 - Input protection measurement

with IR laser at maximum intensity



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
V_{prot} (V)		2.5	2.5						2.1	2.1	3.3	3.3	1.6	2.0	2.5	
Rate (MHz)		5	5						80	5	5	5	5	5	5	
Bias voltage (V)		120	120						120	120	120	0	120	120	120	

Evaluated data… Measurements performed under the same conditions

Remarks:

Measurement with IR laser at maximum intensity
Data evaluated for following conditions: Repetition rate: 5 MHz / Bias voltage: 120 V
No pixels damaged when pulsing with 80 MHz and/or 0 V bias voltage Noise data: STANDARD pixel: row 6 / DIODE pixel: row 8 / NMOS PIXEL: row 10
Single dead pixel may be occurring due to user misoperation → wrong movement of laser beam

V_{prot}	1.6 V	2.0 V	2.5 V	3.3 V
NONE (Standard / High gain)				
Number of surviving pixels	0 % (8)	0 % (8)	0 % (8)	0 % (8)
Noise (ADC)	13.15 +/- 0.12	13.21 +/- 0.13	13.57 +/- 0.13	13.32 +/- 0.13
DIODE				
Number of surviving pixels	100 % (3)	100 % (3)	100 % (3)	0 % (3)
Comments	Reduction of pulseheights at 2.5V most probably due to partial covering of Al backside contact			
Noise (ADC)	13.46 +/- 0.12	13.33 +/- 0.13	13.29 +/- 0.13	13.48 +/- 0.12
NMOS				
Number of surviving pixels	33 % (3)	0 % (3)	0 % (3)	0 % (3)
Noise (ADC)	13.43 +/- 0.12	13.33 +/- 0.12	13.39 +/- 0.12	13.54 +/- 0.13

Protection measures

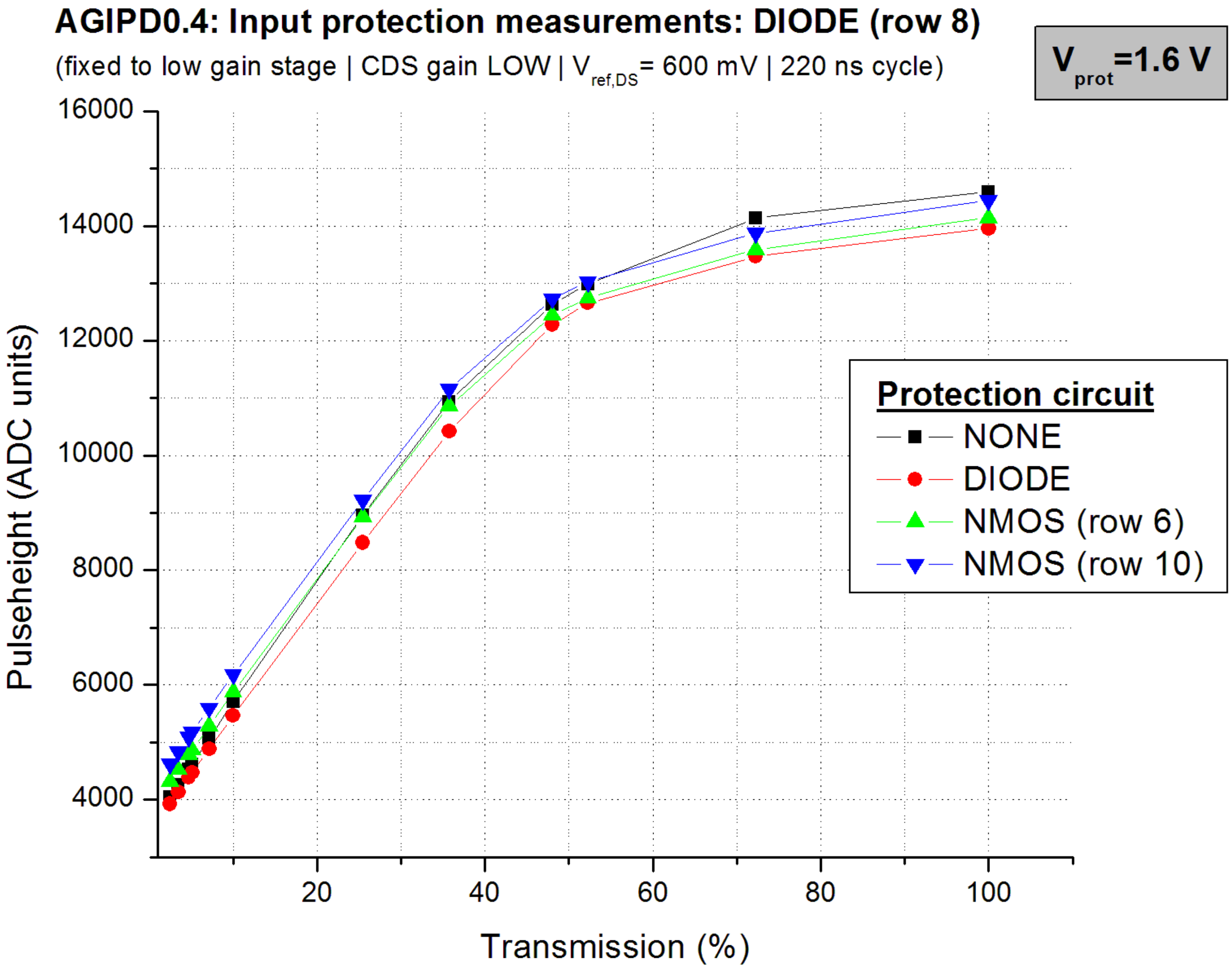
Leaking through protection curcuit?

→ 1.6 V worst case scenario

→Looking at bending of curves for high pulses

→Nmos curves *bend* clearly for transmission >50 %

→Diode *like* Standard, yet radiation hardness to be tested



Speed (Writing)

- 220 ns write-switch-reset cycle @ 80 MHz

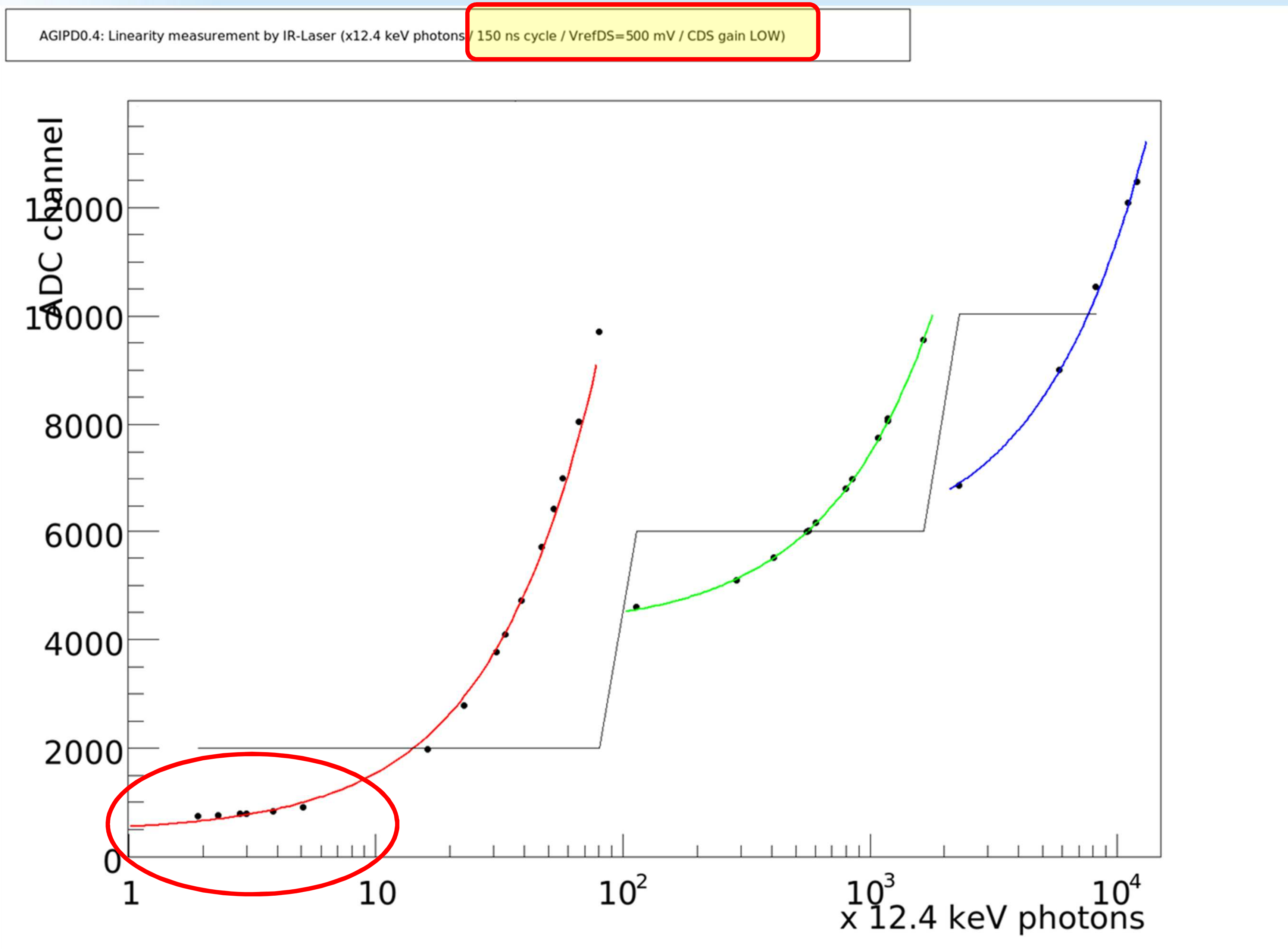
→ 17 clks = 212.5 ns

- Investigated 150 ns cycle

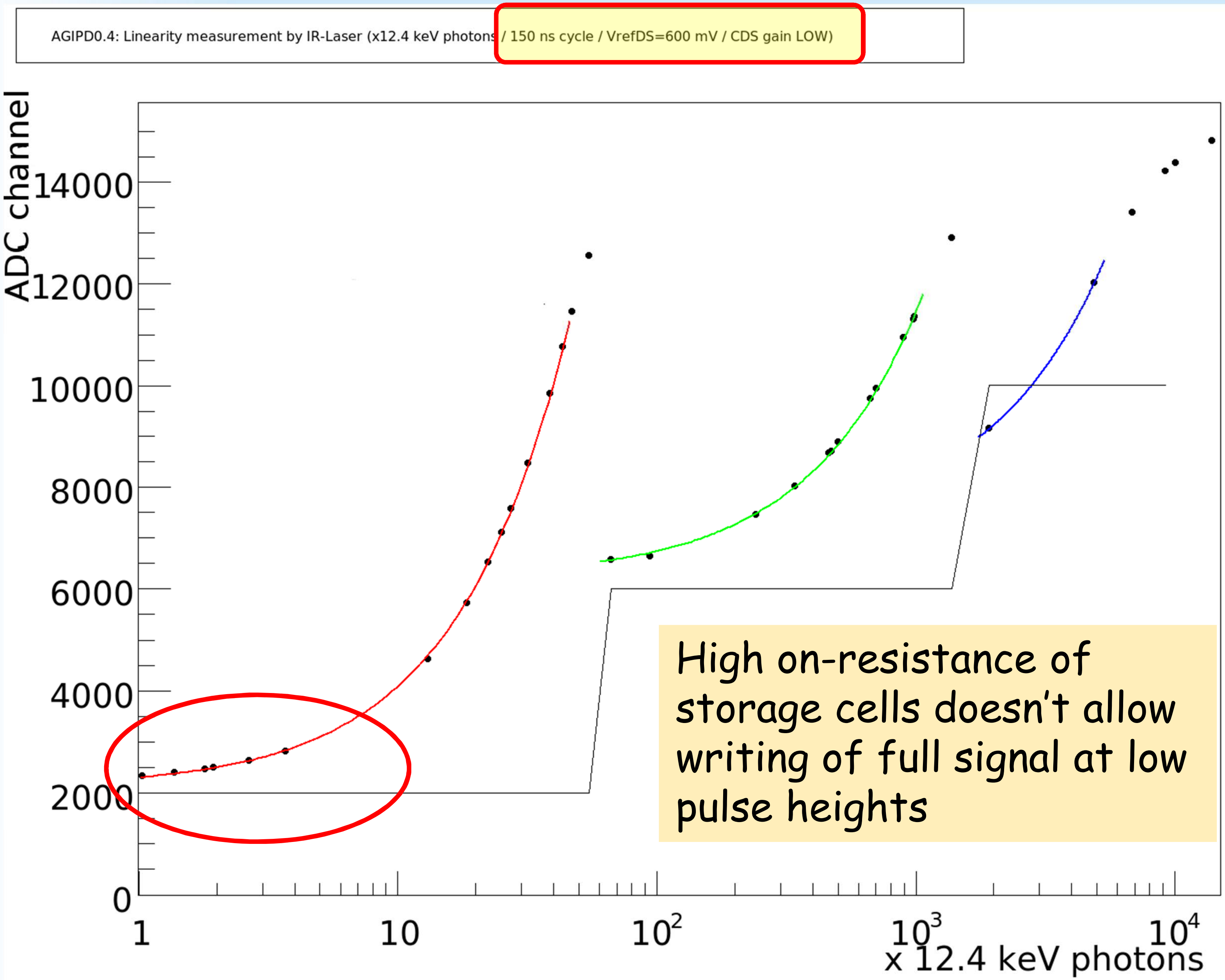
→Only 12 clks
(Reducing RST time by 2, Reducing Integration time by 3)

```
        ////////////////////////////////////////
        // Integration, Write & Reset cycle //
        ////////////////////////////////////////

SB(en_tst_curr);
REPEAT(1);

for(memclk=0;memclk<1;memclk++) {

        SB(rst_preamp);
        SB(set_g1_ext);
        SB(set_g2_ext);
        SB(ds_sw1);

        SB(memcol_clk);SB(clk_dac);
        REPEAT(1);
        CB(memcol_clk);CB(clk_dac);
        REPEAT(1);

        SB(en_amem);SB(en_dmem);
        REPEAT(1);

        CB(en_extgain);
        CB(set_g1_ext);
        CB(set_g2_ext);
        REPEAT(3);
        CB(rst_preamp);
        REPEAT(1);
        CB(ds_sw1);

        REPEAT(10);

        CB(en_amem);CB(en_dmem);

}

REPEAT(1);
CB(en_tst_curr);
REPEAT(1);
```

Speed (Writing)

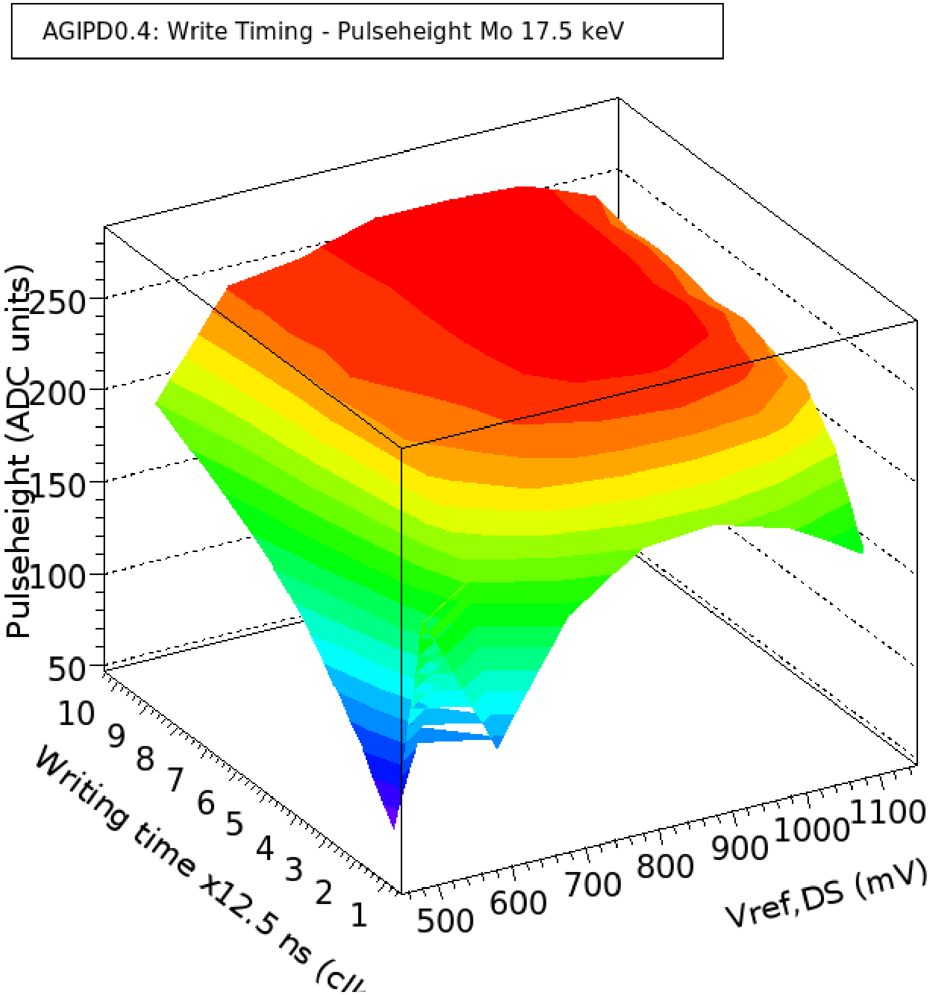


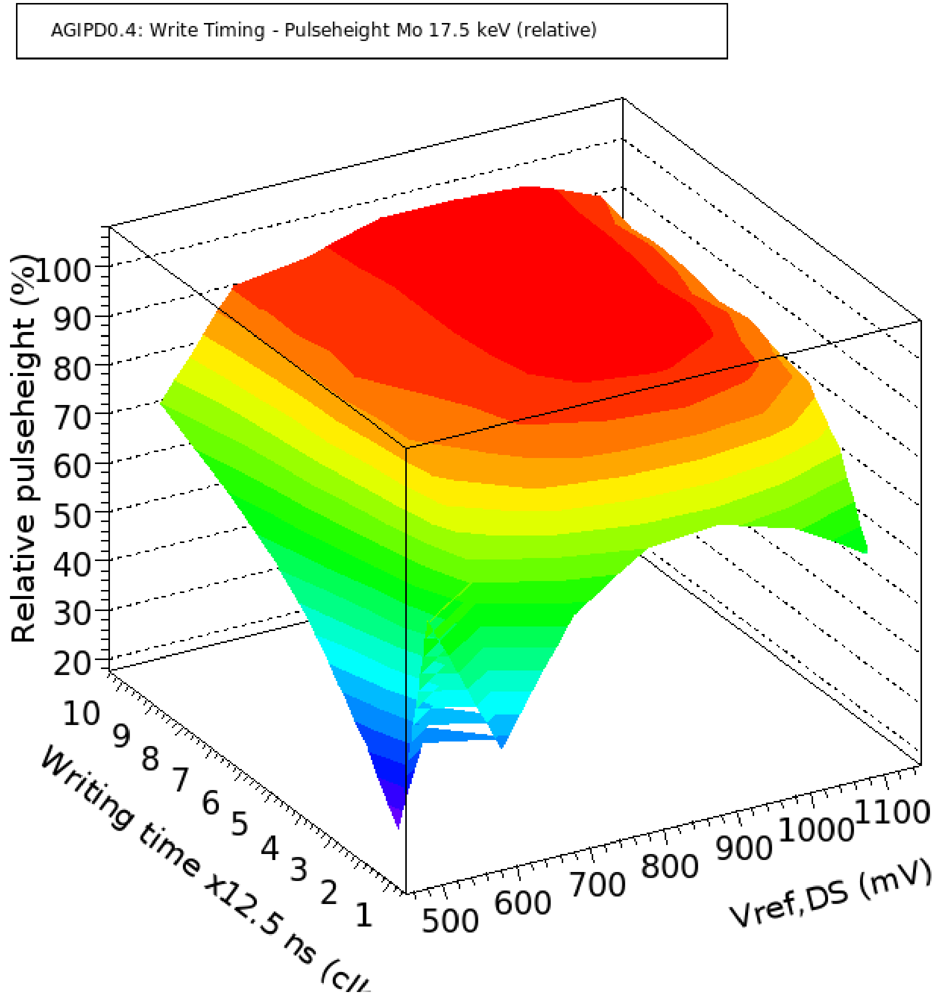
Speed (Writing)



High on-resistance of storage cells doesn't allow writing of full signal at low pulse heights

Speed (Writing)





- @ $V_{ref,DS}$= 500 mV: Signal height never higher than 70 % of maximal height due to incomplete writing on storage cell

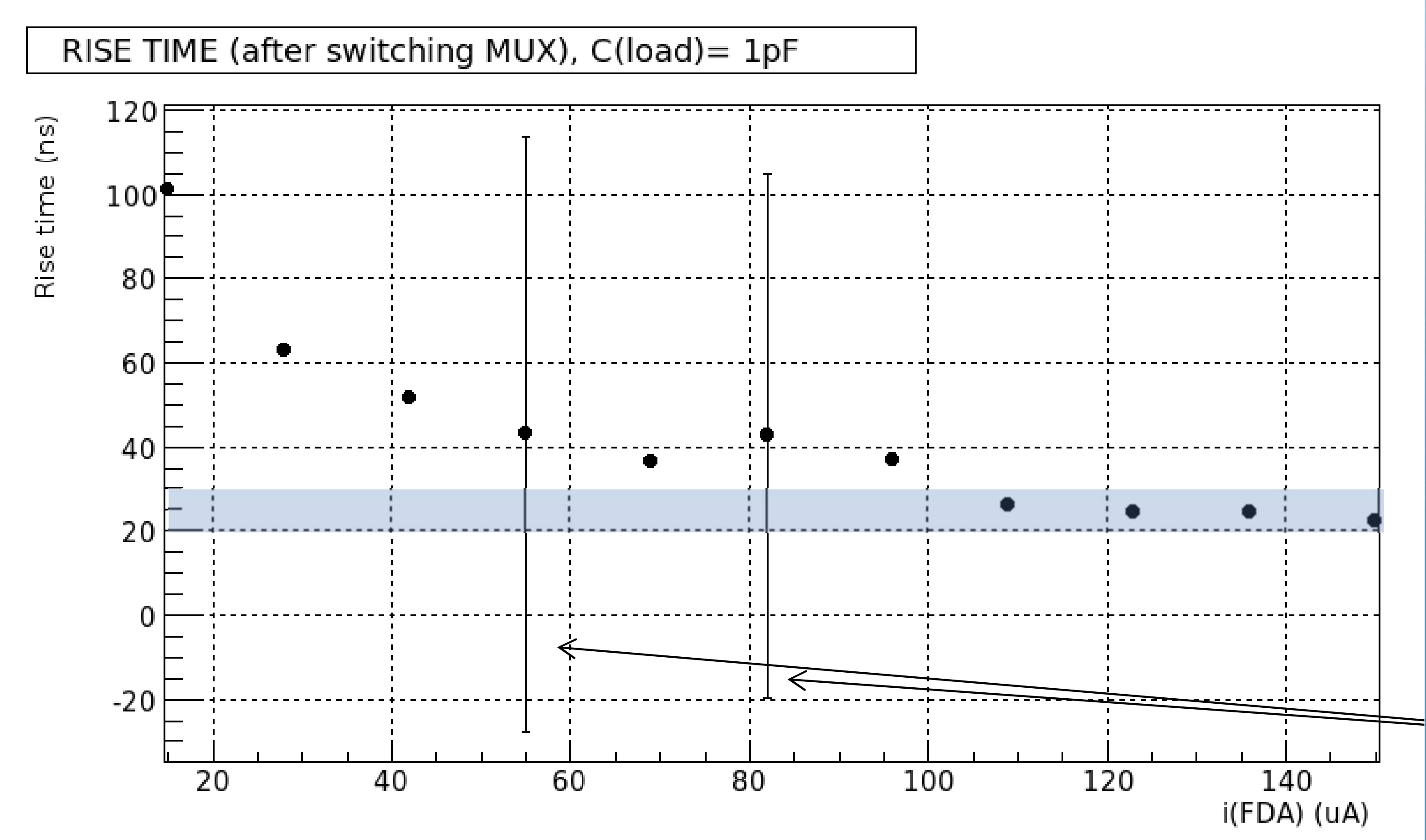
→Choosing $V_{ref,DS}$= 600 mV: Losing "only" 10 – 15 %

→ New CDS STAGE: faster, linear up to 1300 mV

Speed (Reading)

New Chipoutputbuffer:

- Fully differential
- Can drive up to 100 Ω
- Can drive that in 30 ns …that needed to be verified!



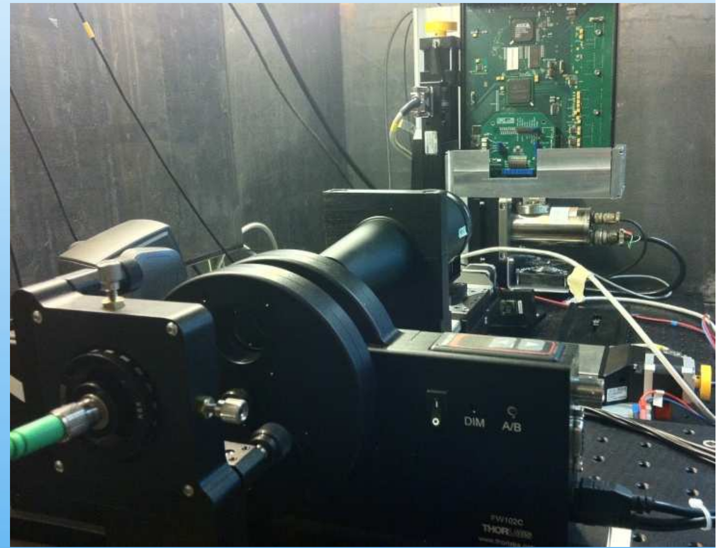
No sync between ADC clock and pattern clock

Dynamic Range

<u>Laser Setup:</u>

- Red (660 nm) and IR (1030 nm) laser diodes
- Repetition rate: 5 … 80 MHz (divider up to 16)
- Power: <11.5 mW (red) / <15 mW (IR)
- 2x Filter wheel → 36 combinations

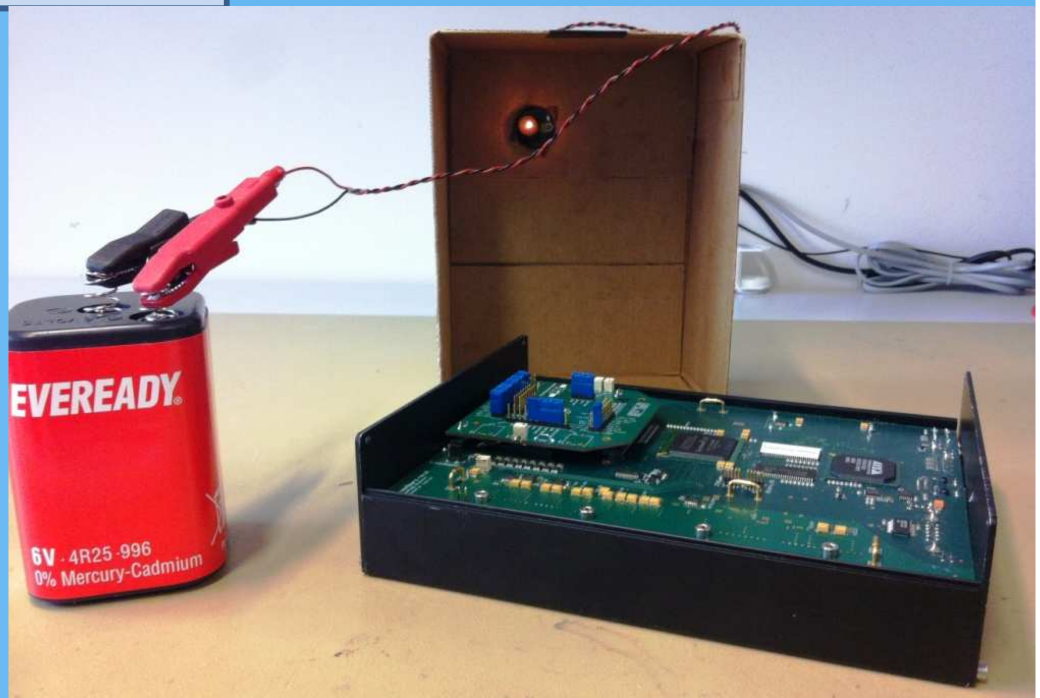
BUT shot-to-shot fluctuations,
difficult to measure noise



<u>Lamp Setup:</u>

almost perfect constant current source

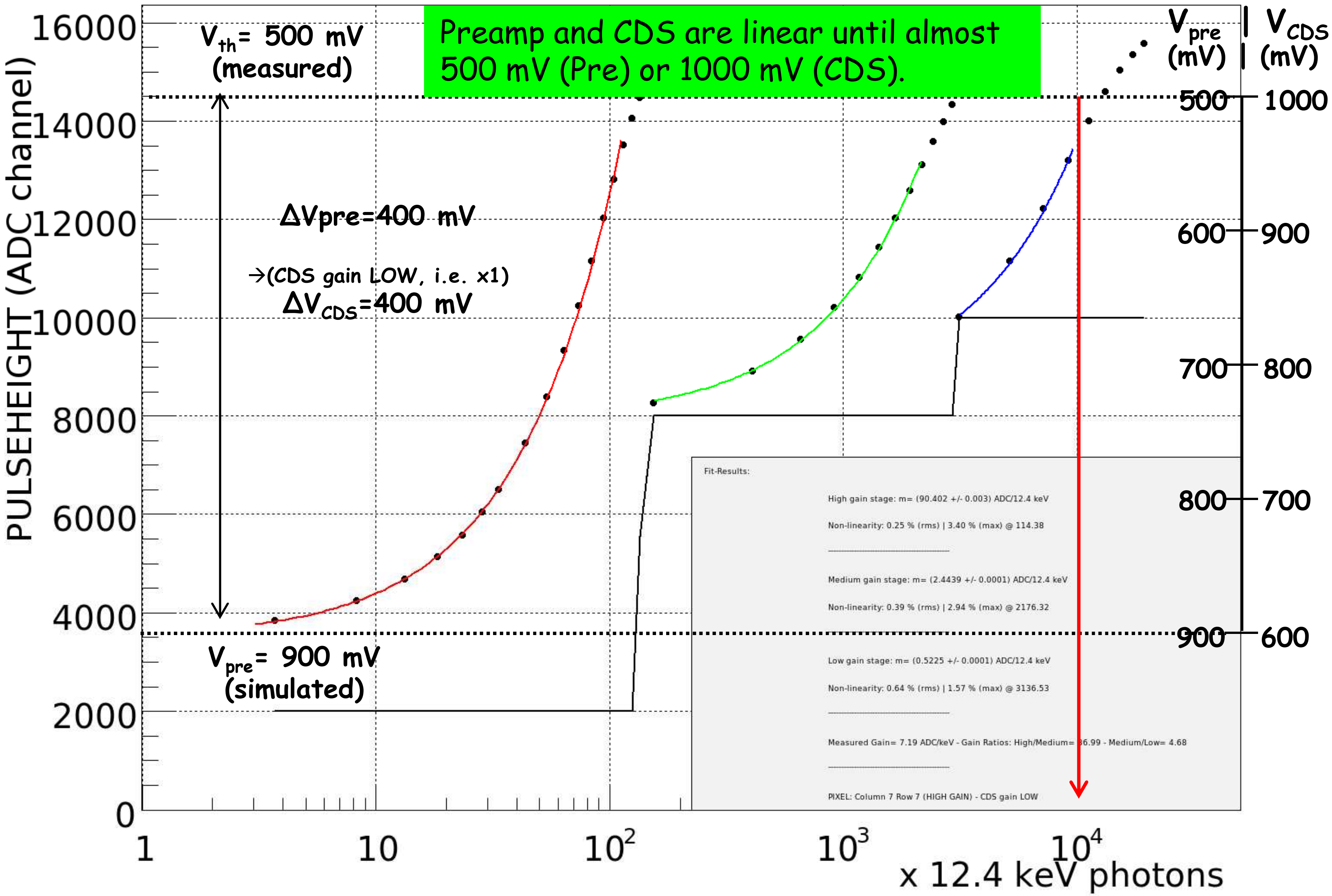
- simple,
- reliable,
- cross calibration possible by energy calibration



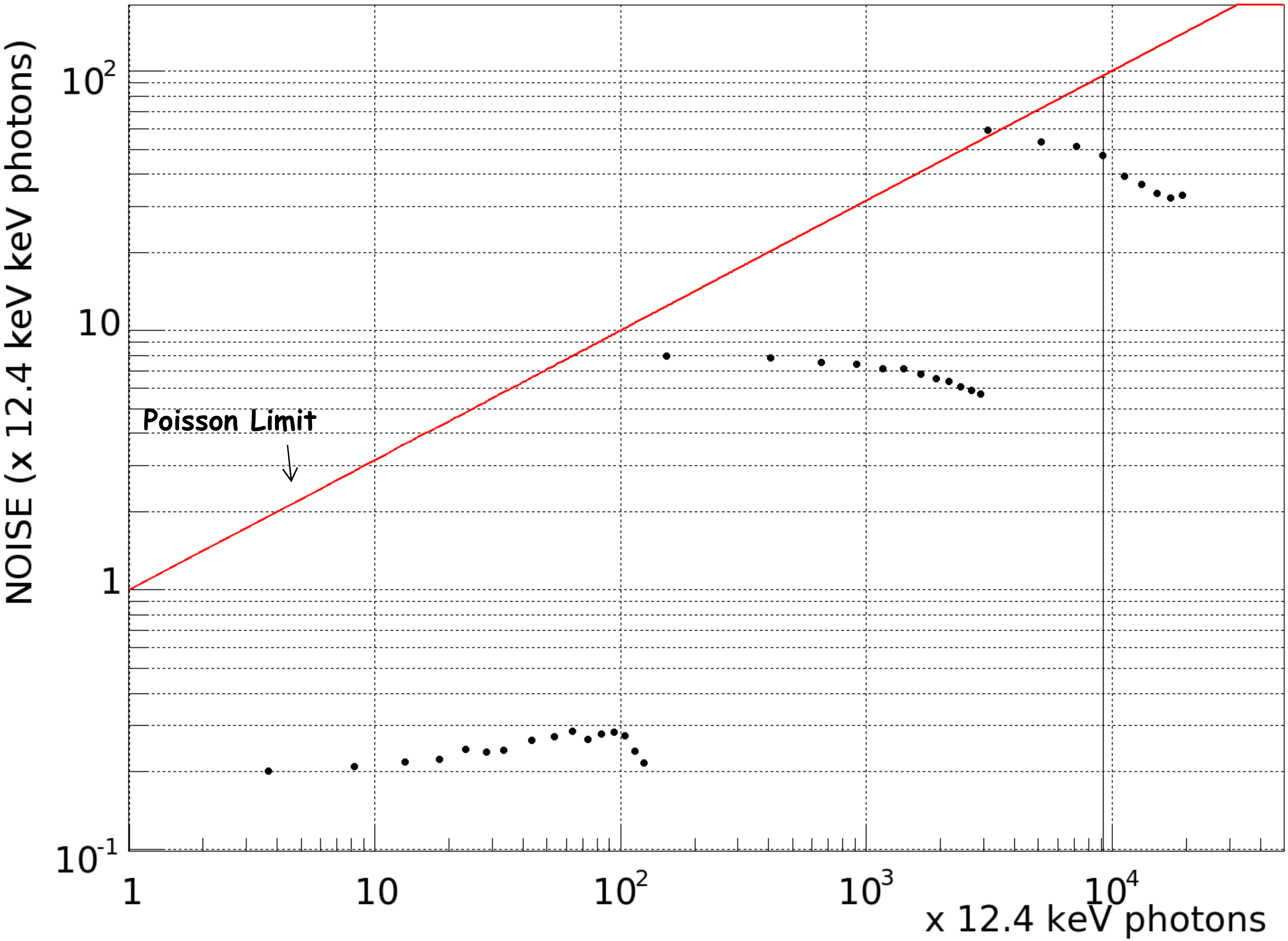
Dynamic Range

AGIPD0.4: Linearity measurement by Flashlight (x 12.4 keV photons) - Pixel: Column 7 Row 7 (High Gain) - Classical RST (220 ns cycle / VrefDS=600 mV / CDS gain LOW / Cfhigh=60 fF)

60 fF / CDS gain LOW



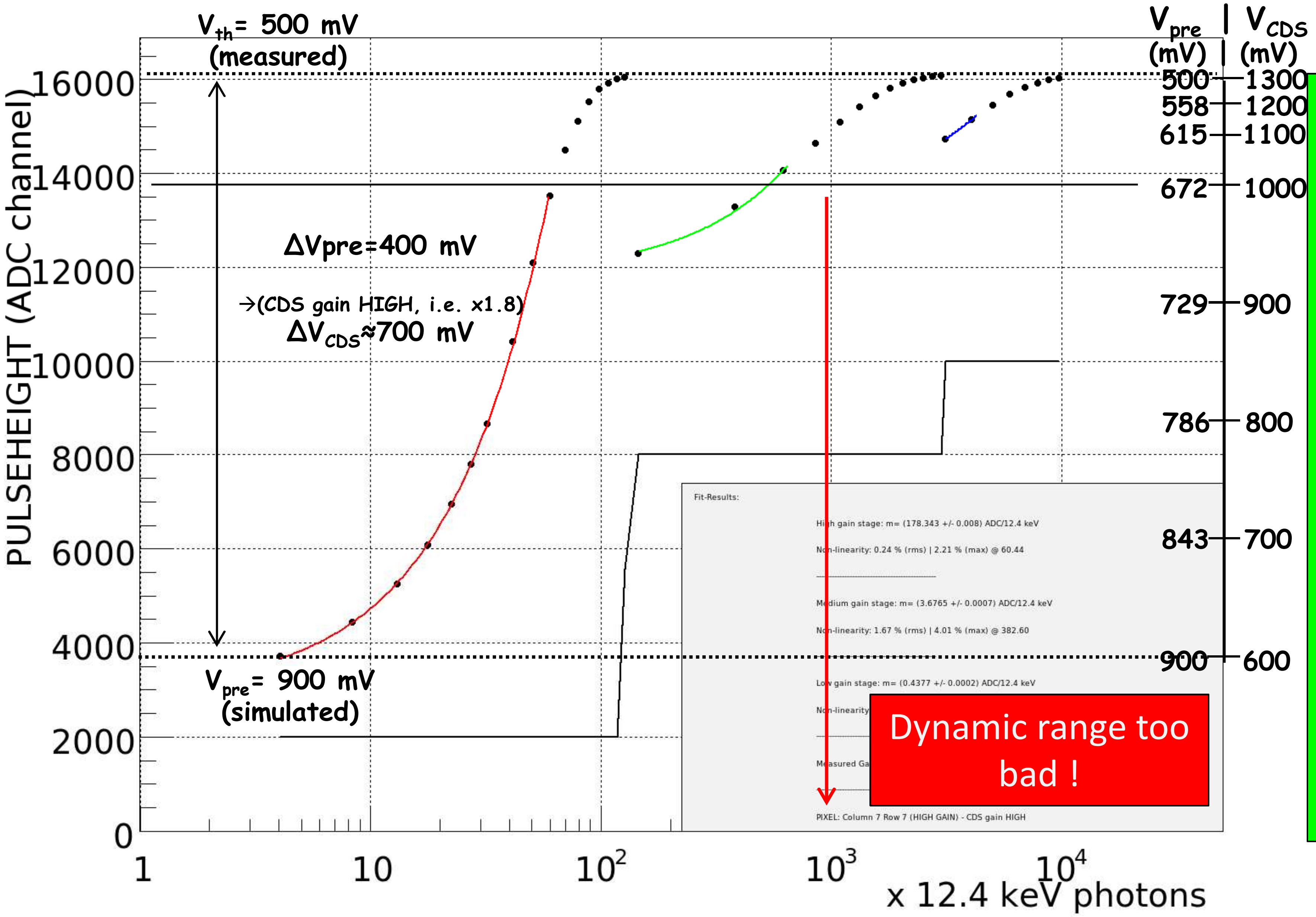
AGIPD0.4: Linearity measurement by Flashlight (x 12.4 keV photons) - Pixel: Column 7 Row 7 (High Gain) - Classical RST (220 ns cycle / VrefDS=600 mV / CDS gain LOW / Cfhigh=60 fF)



Dynamic Range

AGIPD0.4: Linearity measurement by Flashlight (x 12.4 keV photons) - Pixel: Column 7 Row 7 (High Gain) - Classical RST (220 ns cycle / VrefDS=600 mV / CDS gain HIGH / Cfhigh=60 fF)

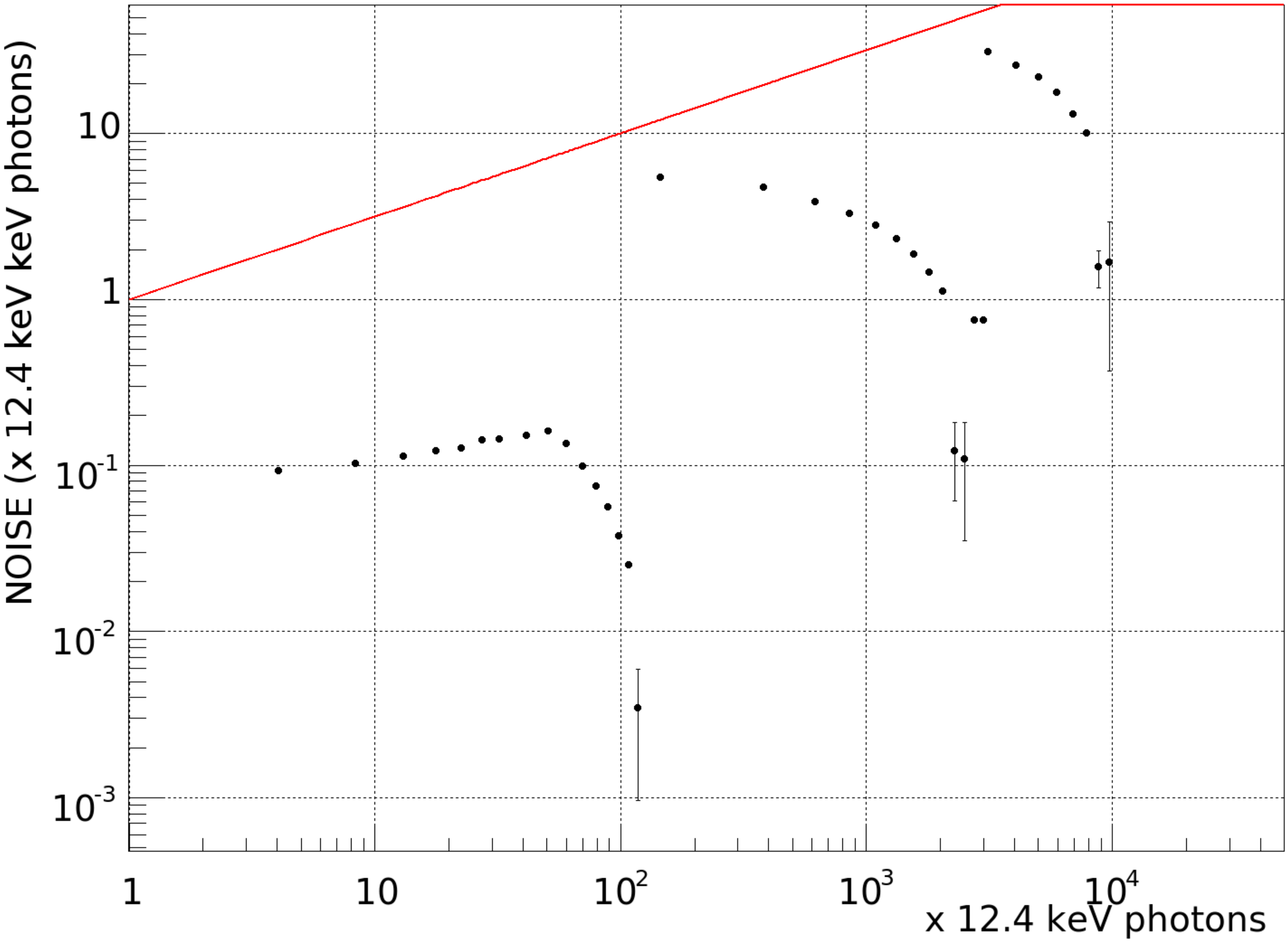
60 fF / CDS gain HIGH



Conclusions:

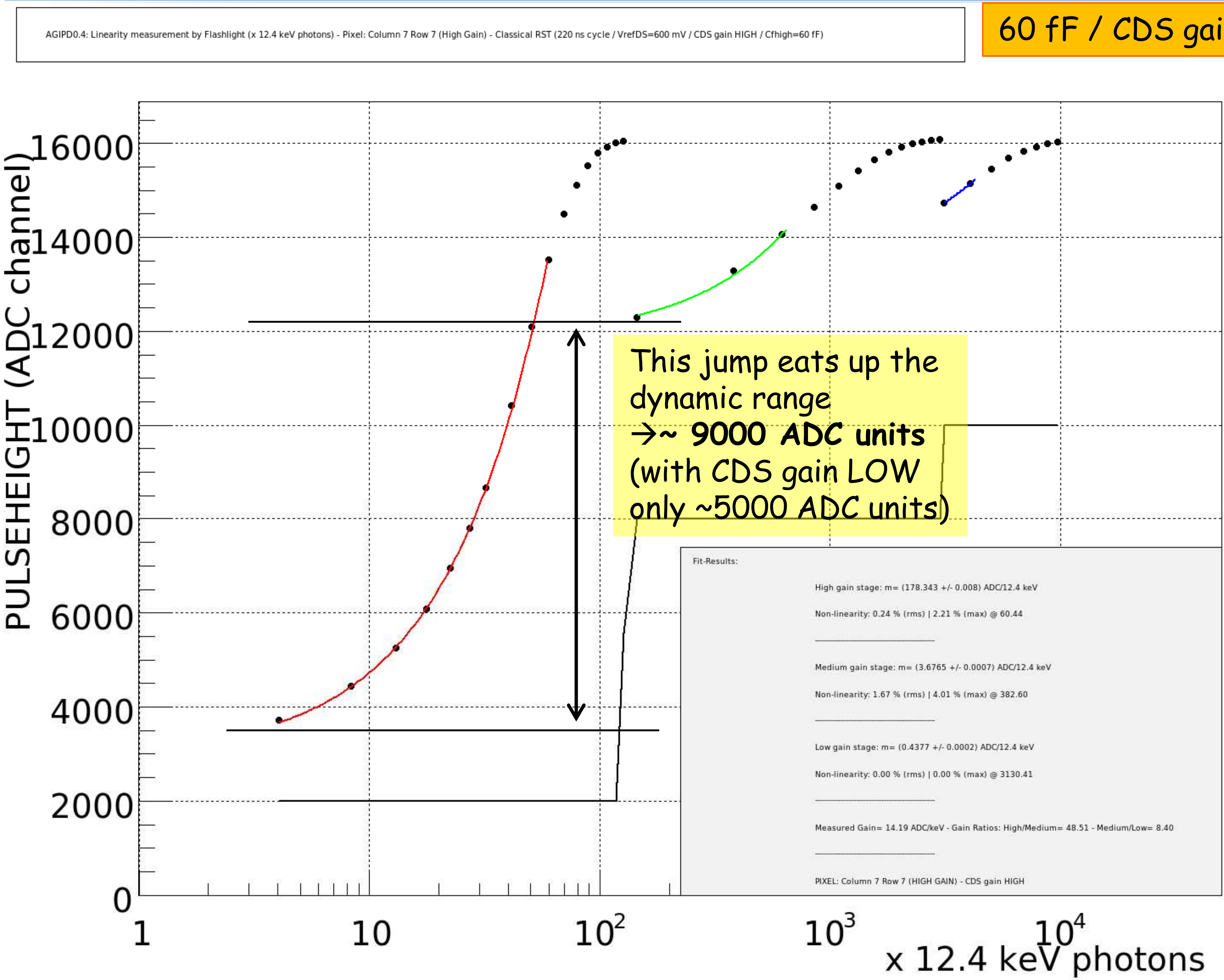
We know:
Preamp is linear, CDS gain change doesn't affect Preamp
→CDS stage gets non-linear for voltages higher than 1.05 V
→ Supported by simulation
→ **New CDS stage** to cover full dynamic range (designed to be **linear up to 1300 mV**)

AGIPD0.4: Linearity measurement by Flashlight (x 12.4 keV photons) - Pixel: Column 7 Row 7 (High Gain) - Classical RST (220 ns cycle / VrefDS=600 mV / CDS gain HIGH / Cfhigh=60 fF)

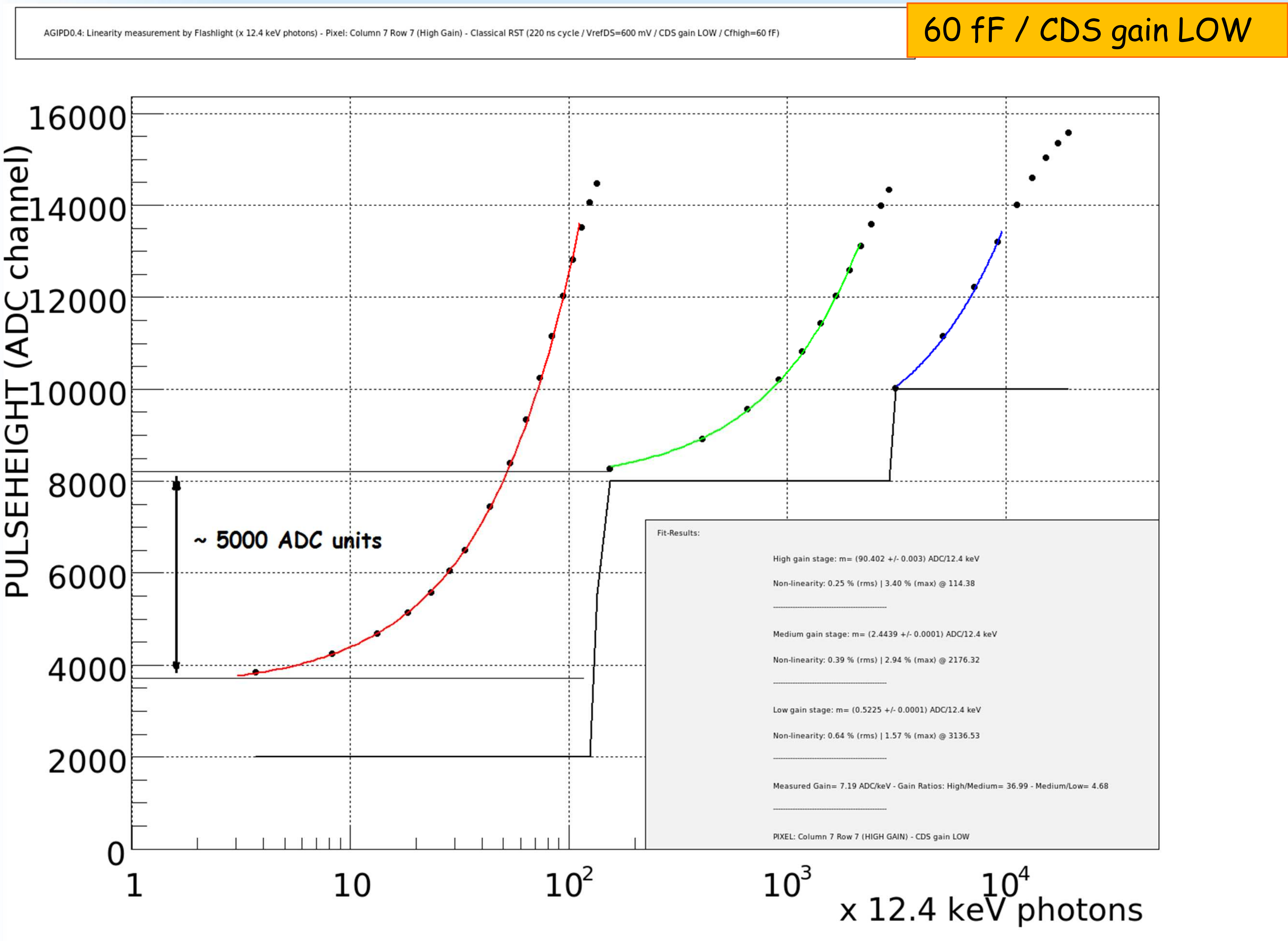


Dynamic Range

60 fF / CDS gain HIGH

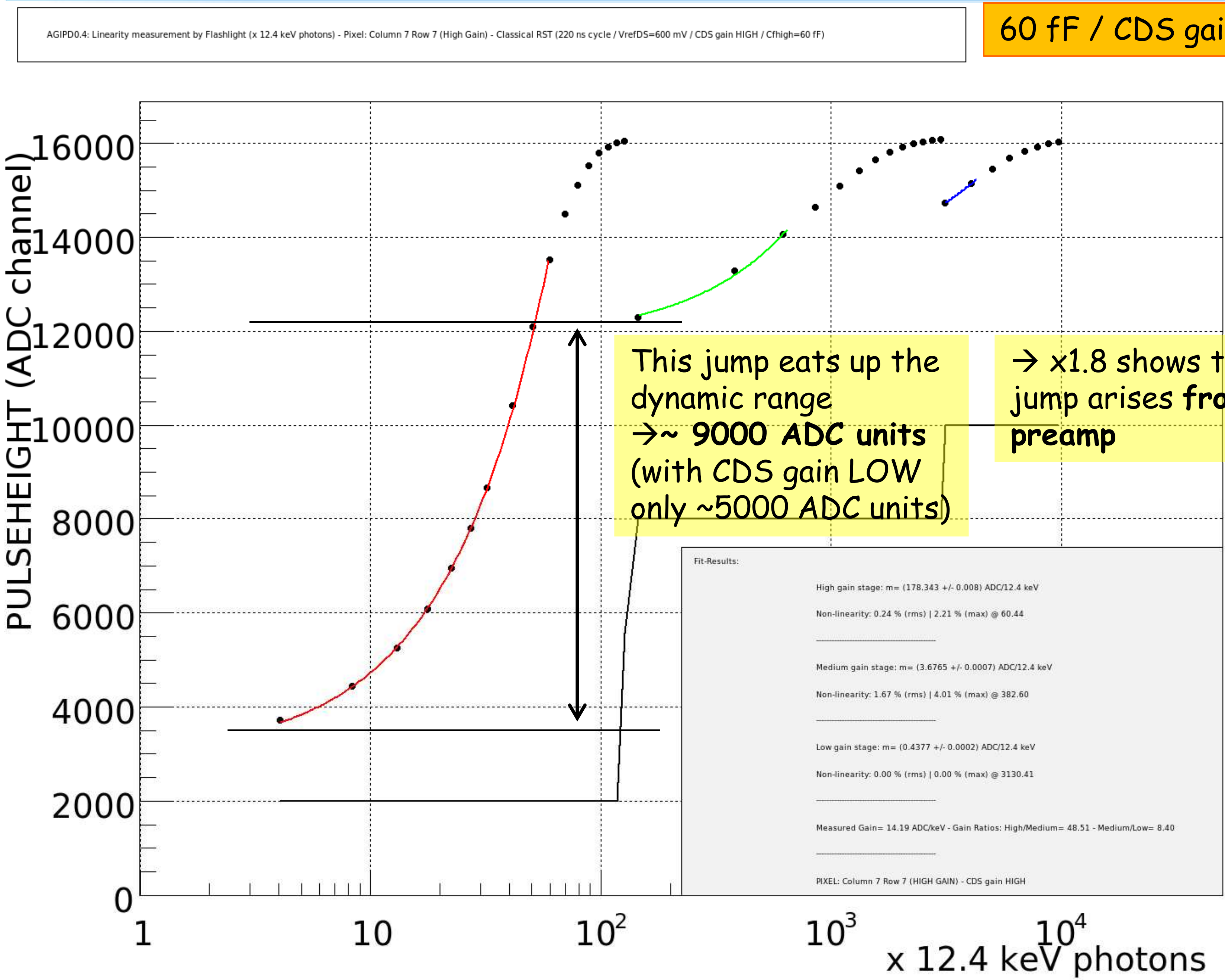


Dynamic Range



Dynamic Range

60 fF / CDS gain HIGH



This jump eats up the dynamic range
→~ **9000 ADC units**
(with CDS gain LOW only ~5000 ADC units)

→ x1.8 shows that jump arises **from preamp**

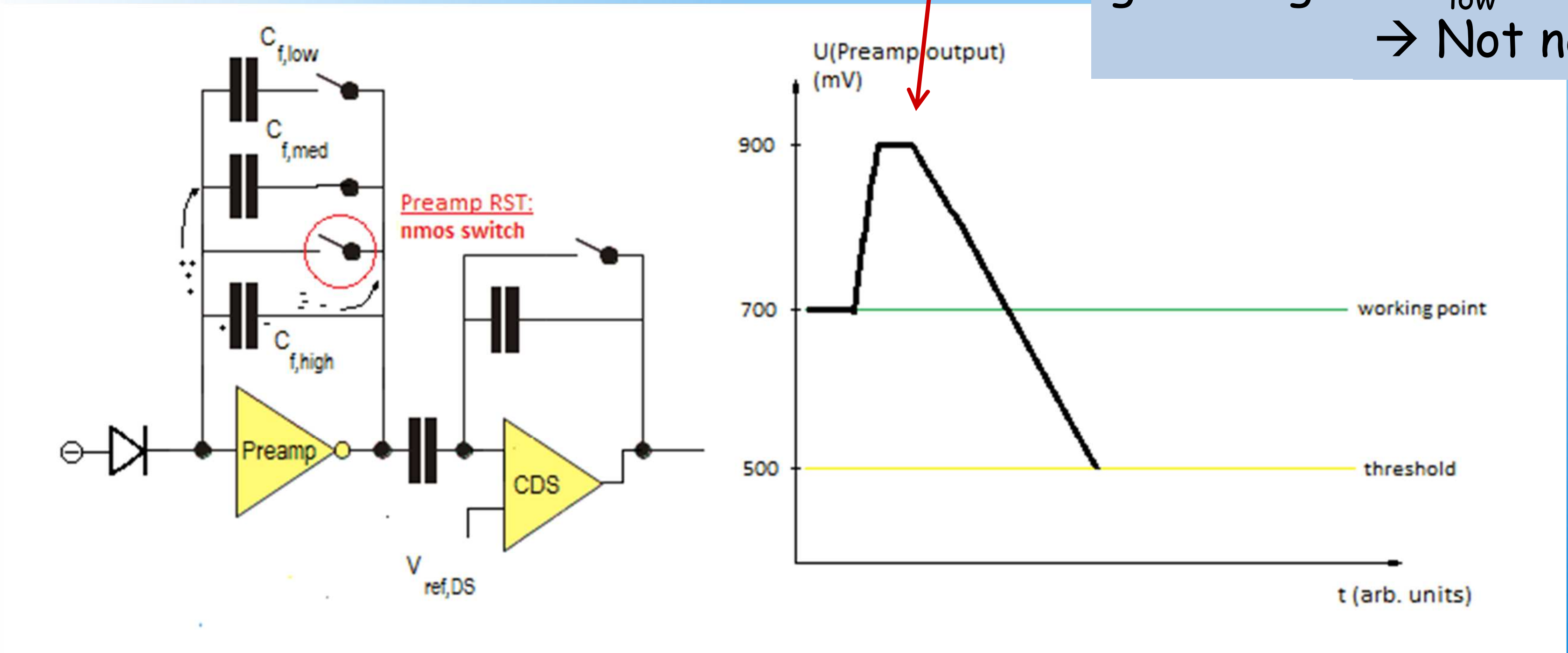
Dynamic Range

Jump is due to an actually wanted charge injection in the $C_{f,high}$ in order to increase the dynamic range of the high gain stage

Reset phase

CDS sampling point

Redistribution of charge Between, when switching to low gain stage: $\Delta U_{low} = \Delta U_{med} \cdot 0.235$
→ Not negligible



$\Delta U_{highInj} = \Delta Q_{PreRSTInj} / C_{f,high}$

→ Change from 100 fF to 60 fF increased voltage jump by 66 %

Redistribution of charge between $C_{f,high}$ and $C_{f,med}$: $\Delta U_{med} = \Delta U_{high} \cdot C_{f,high} / (C_{f,high} + C_{f,med})$
$= \Delta U_{high} \cdot 0.023$
$\approx$ few mV

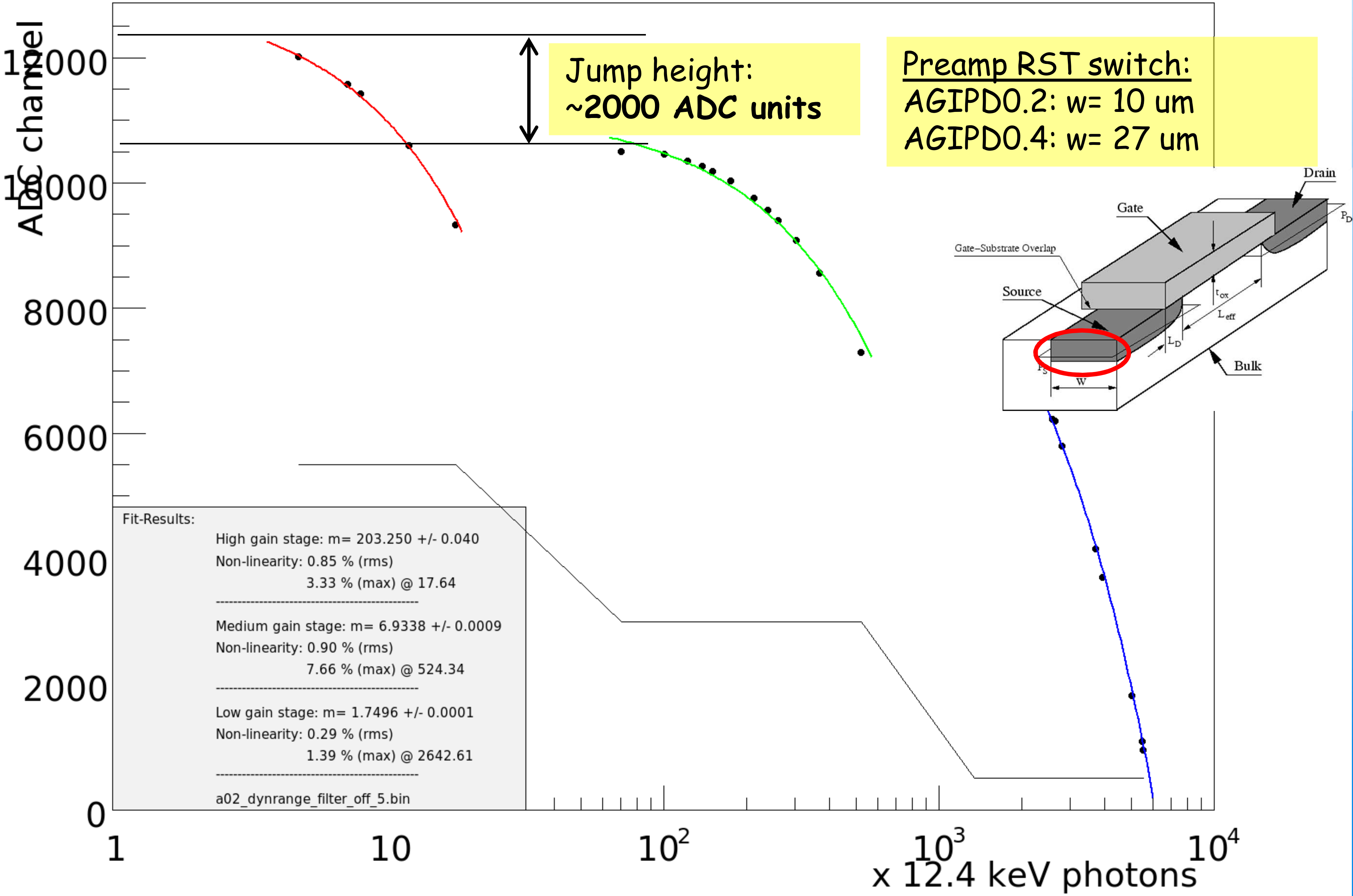
Dynamic Range

AGIPD0.2: Linearity measurement by IR-Laser (x12.4 keV photons)

AGIPD0.2: 100 fF / CDS gain HIGH

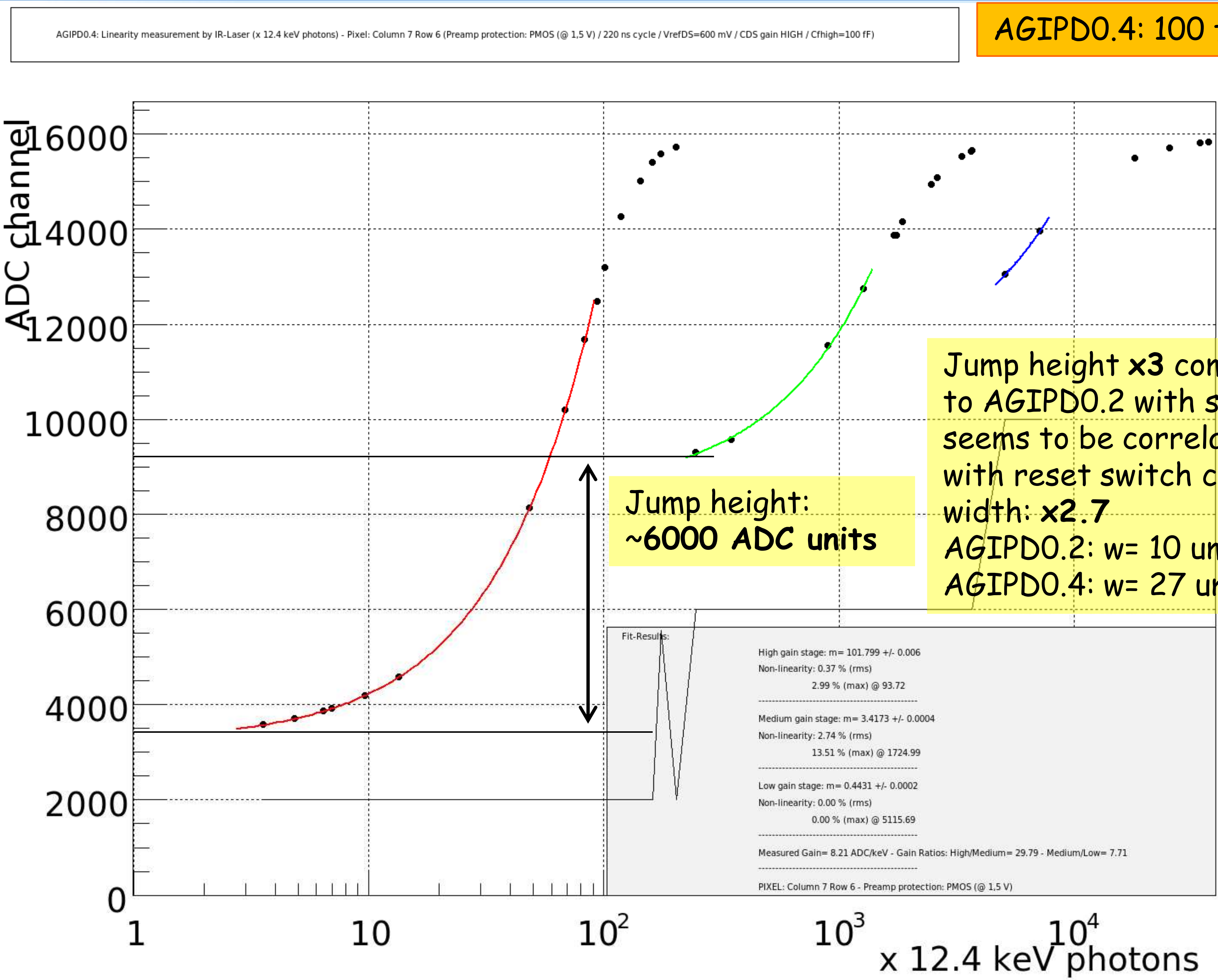
Jump height:
~2000 ADC units

Preamp RST switch:
AGIPD0.2: w= 10 um
AGIPD0.4: w= 27 um



Dynamic Range

AGIPD0.4: 100 fF / CDS gain HIGH

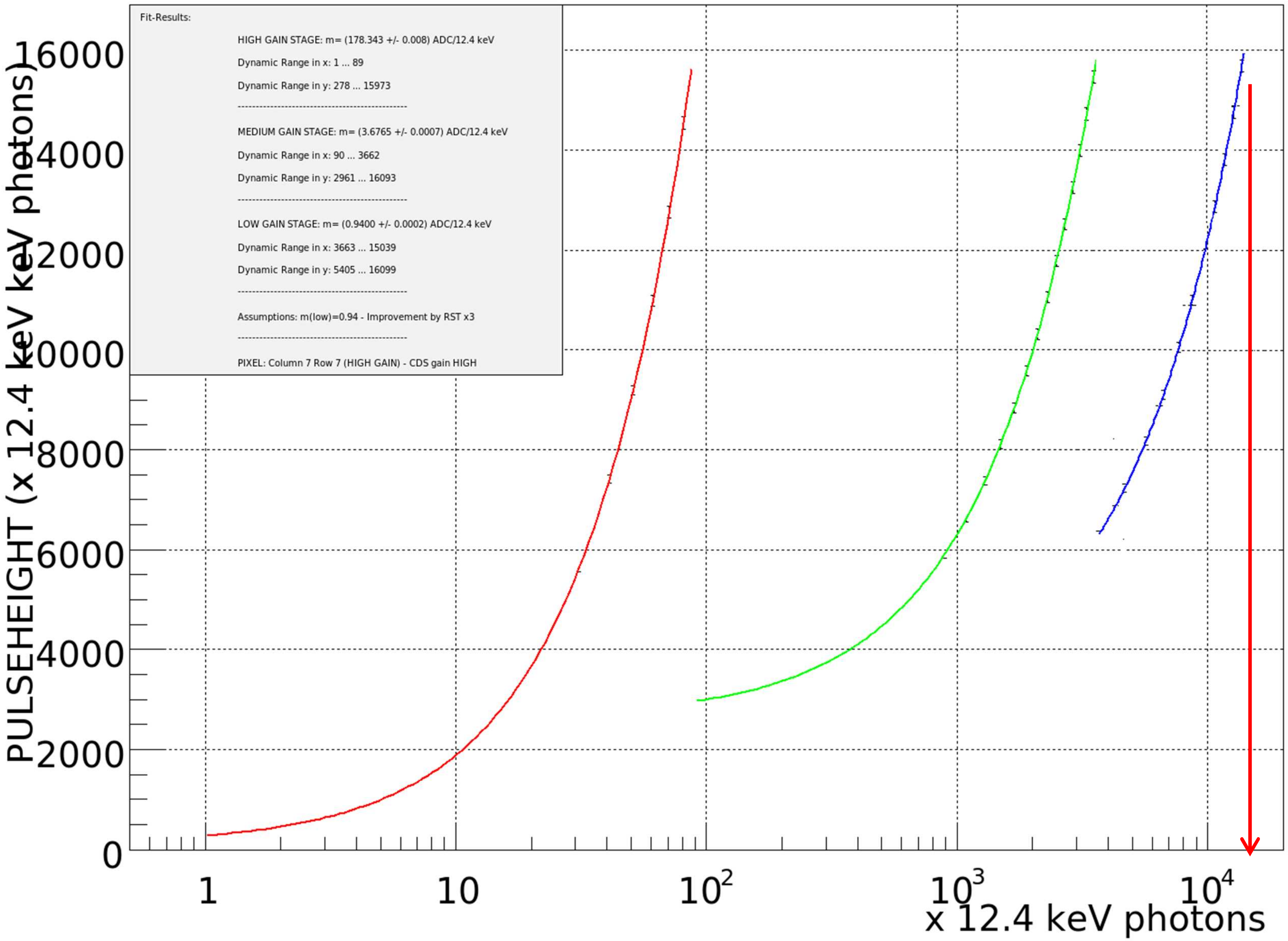


Jump height:
~6000 ADC units

Jump height **x3** compared to AGIPD0.2 with same C_f, seems to be correlated with reset switch channel width: **x2.7**
AGIPD0.2: w= 10 um
AGIPD0.4: w= 27 um

Dynamic Range

AGIPD1.0: Expected Dynamic Range with Smaller Preamp RST & Improved CDS stage (up to 1.3 V) (CDS gain HIGH / Cfhigh=60 fF)



__Proposed improvements in AGIPD1.0:__

- **Better CDS** (up to 1300 mV)
- ***Smaller Preamp RST switch*** (w=5 um)

→ Very conservative, unrisky changes !

'Real' summary

Component	Updated status	Result
Noise	• C_f = 60 fF • CDS gain HIGH (x2) • Offchip x1.5	Noise (ENC): (301 ± 4) e- (270 ± 3) e- (oversampled) **(Still) okay !**
Protection measures	•Diodes • ~~Nmos switches~~	Radiation hardness to be tested → *critical* **Okay !** **(If rad test positive)**
Speed (Write to SC)	Writing within >150 ns successful	$V_{ref,DS}$ needs to be increased to 600 mV → Improving CDS stage **Okay !**
Speed (Read from SC)	Reading time after switching MUX ~30 ns → 30 MHz	**Okay !**
Dynamic range	Should be possible to get to > 1 · 10^4 x 12.4 keV photons	→ Improved CDS stage → Smaller PCRS1 switch **Most probably: Okay !**

You made it… ☺

Thanks for your attention!