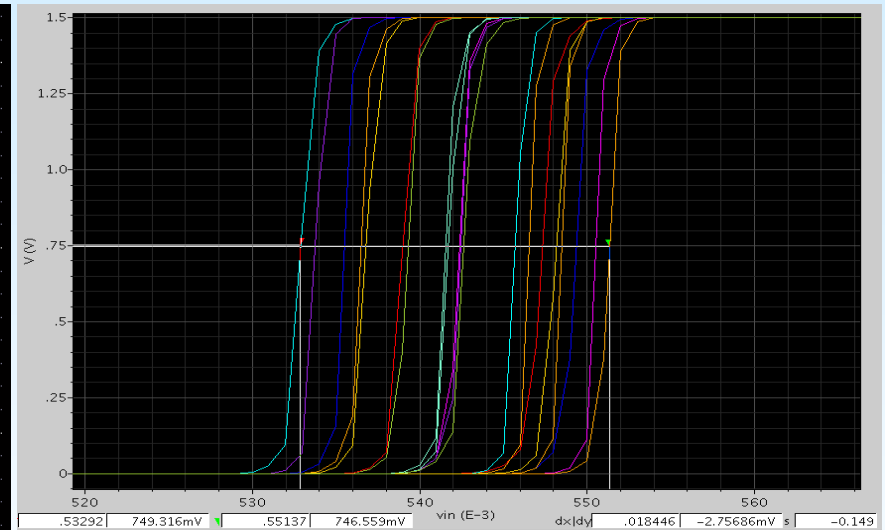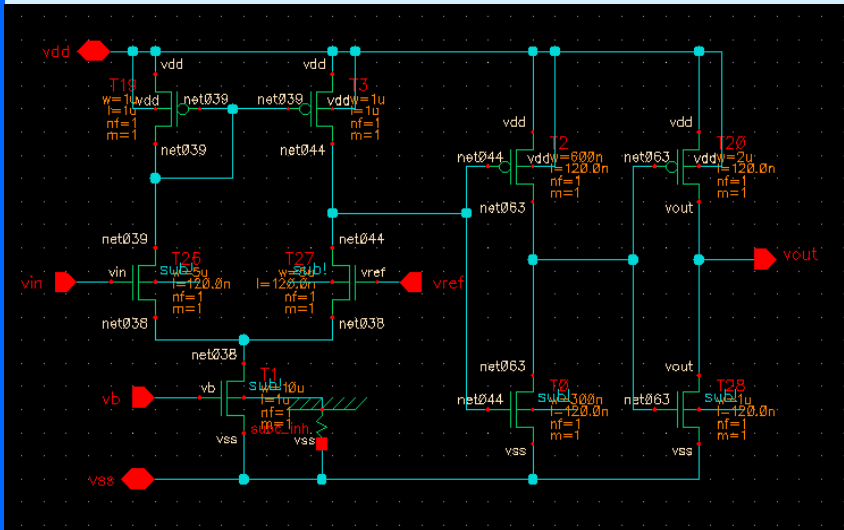# Improvements in Readout ASIC Design

Xintian Shi
05.10.2010
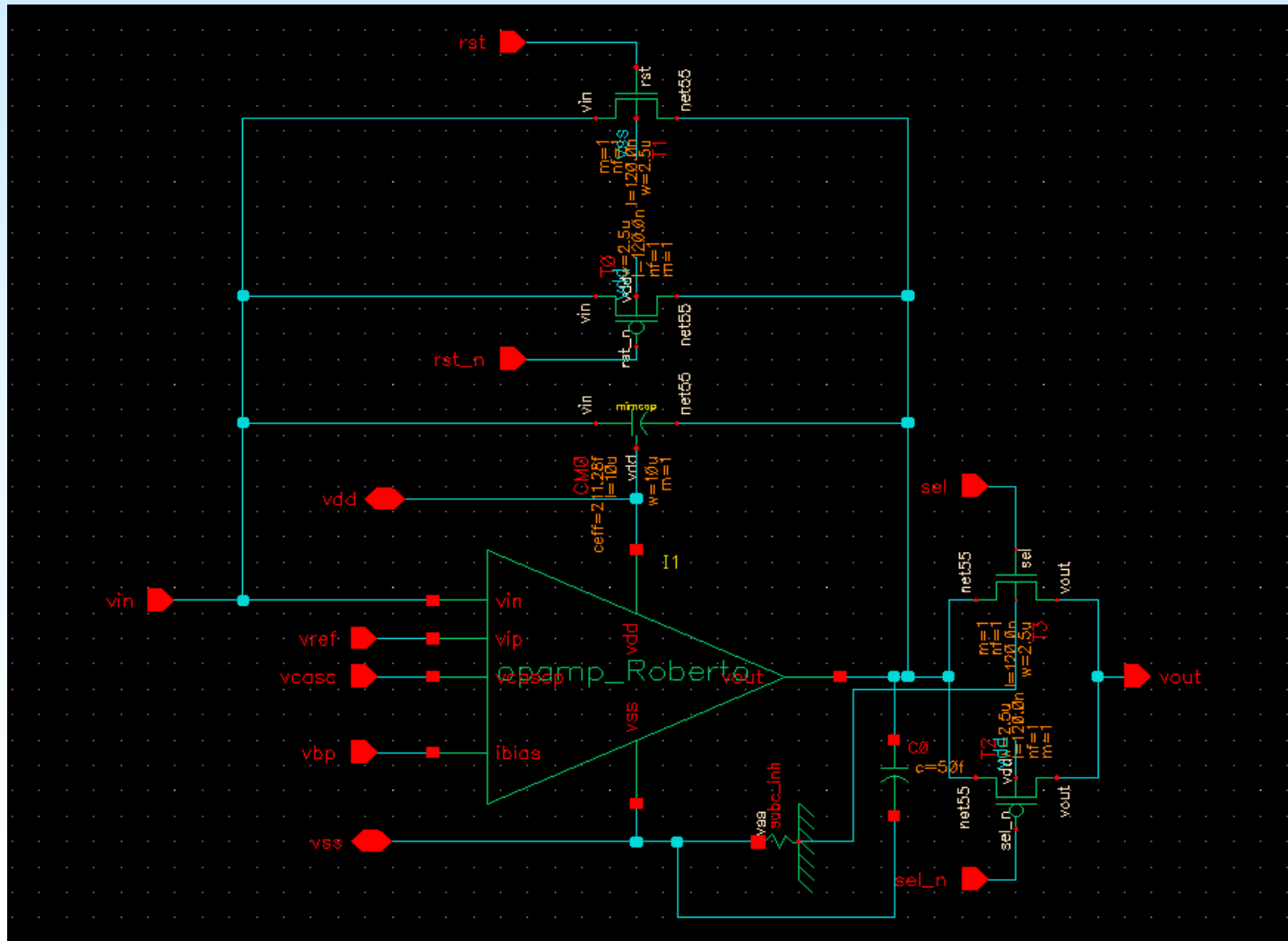
Discriminator

- Differential input stage.
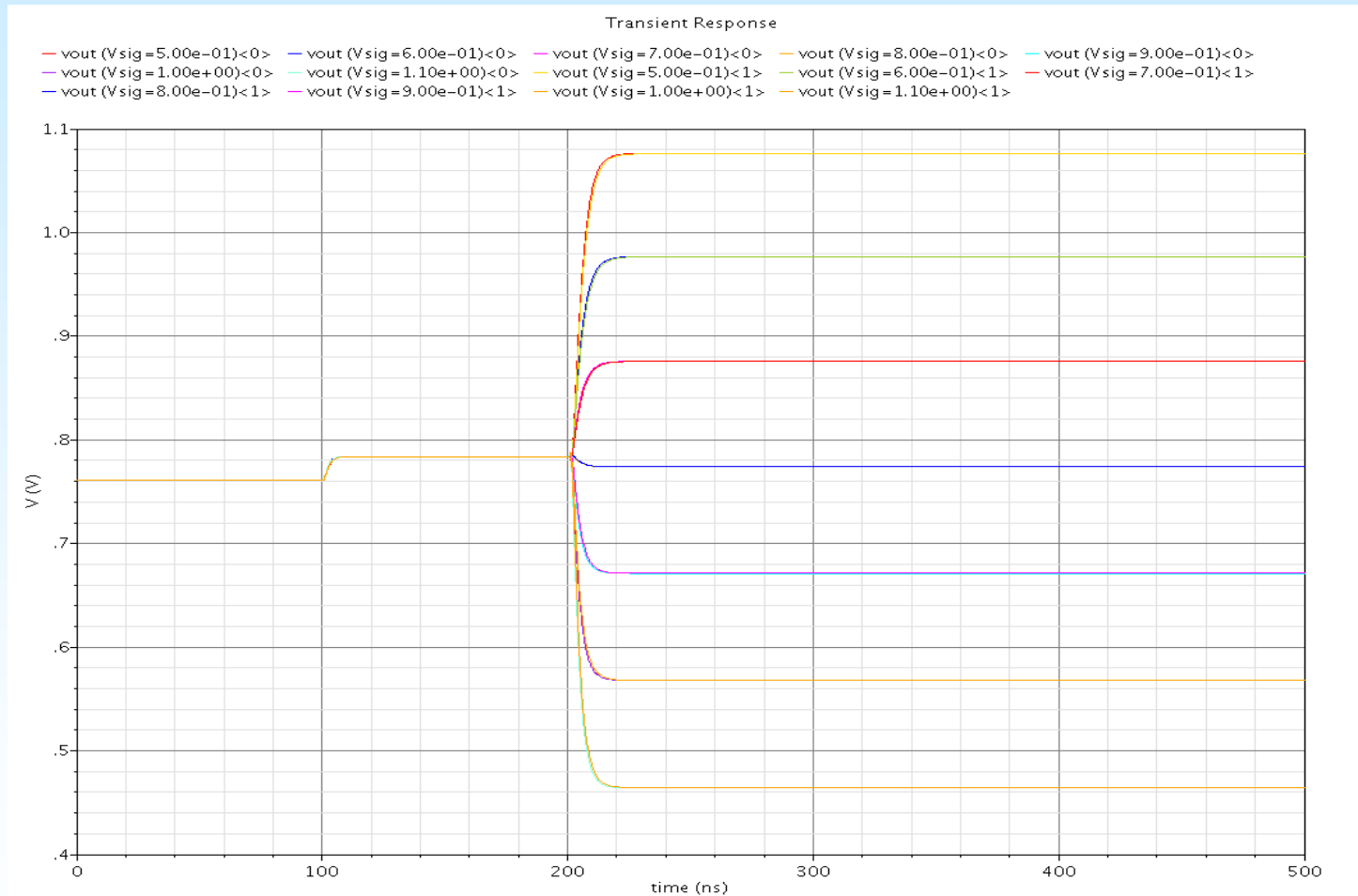- Threshold mismatch < 20 mV (corresponding to 5 photons, 10 times less than the old one).

Charge readout buffer

Charge readout buffer

Transient simulation with Vin from 0.5 V – 1.1 V and the parasitic capacitance of 100 fF / 200 fF.
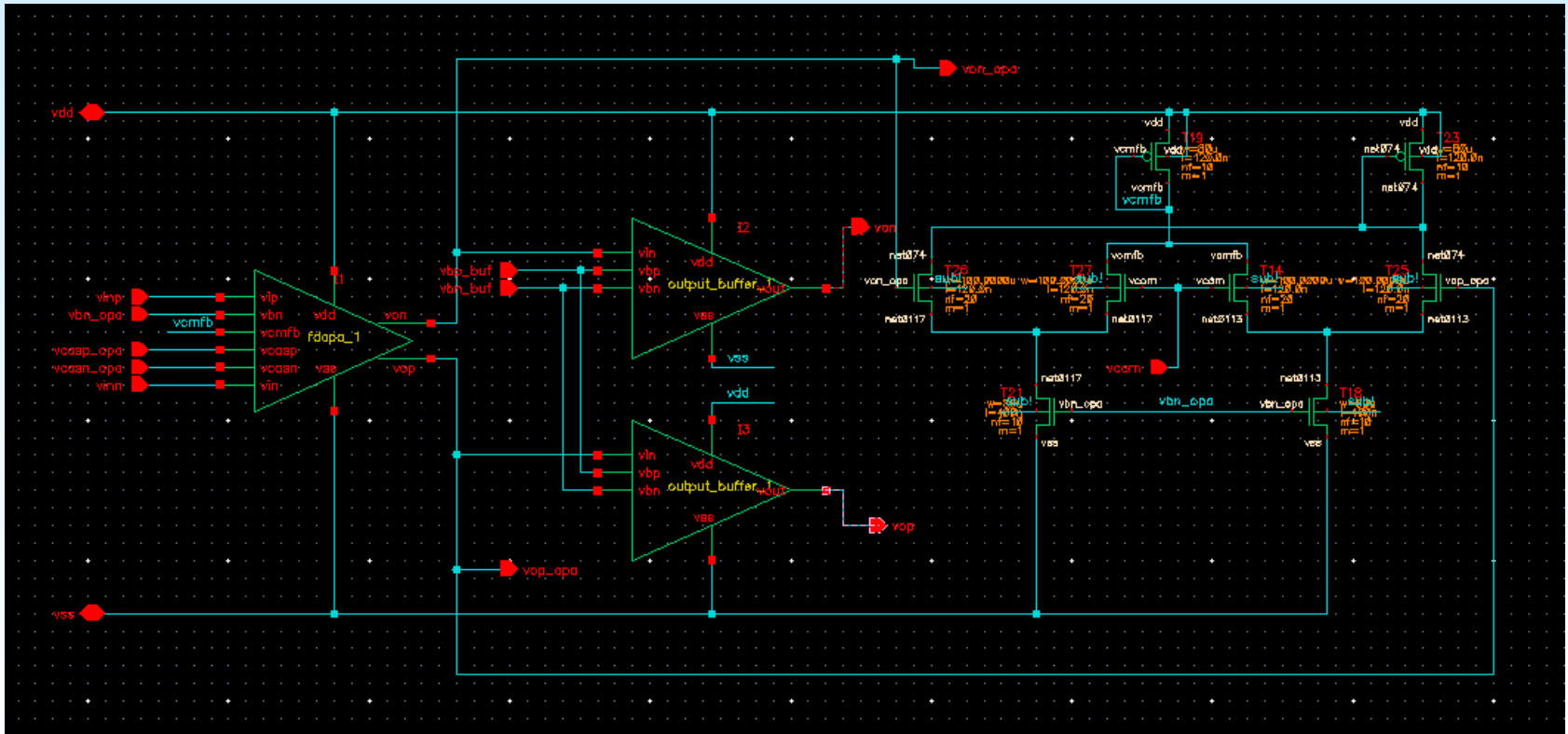
Charge readout buffer

- Linearity is very good and independent on the parasitic capacitance on the bus.
- Readout speed is limited by the switches in the storage cell.
- With a negative gate voltage (-0.5 V) of the switches, 50 MHz readout speed is possible.
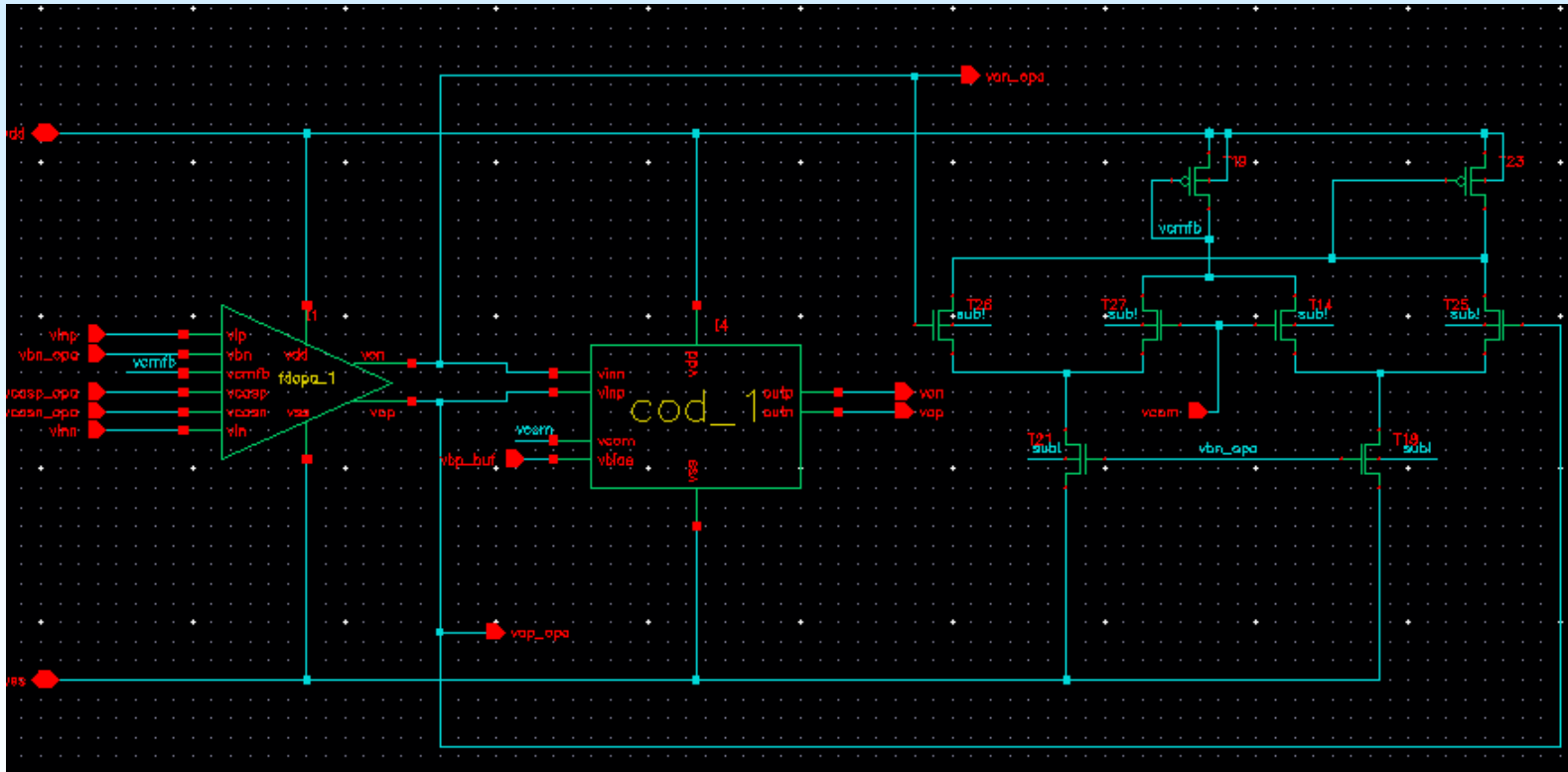
Analog voltage off-chip driver

Analog voltage off-chip driver

- Single ended input -> differential output
- Can drive either a 100 Ohm resistive load or an pure   capacitive load.
- Settling time < 25 ns with Rl = 100 Ohm, Cl = 5 pF.
- Linearity error < 1% with an input voltage range of 0.5 V – 1.0 V.
- Current consumption ≈ 11 mA for a fully differential output .
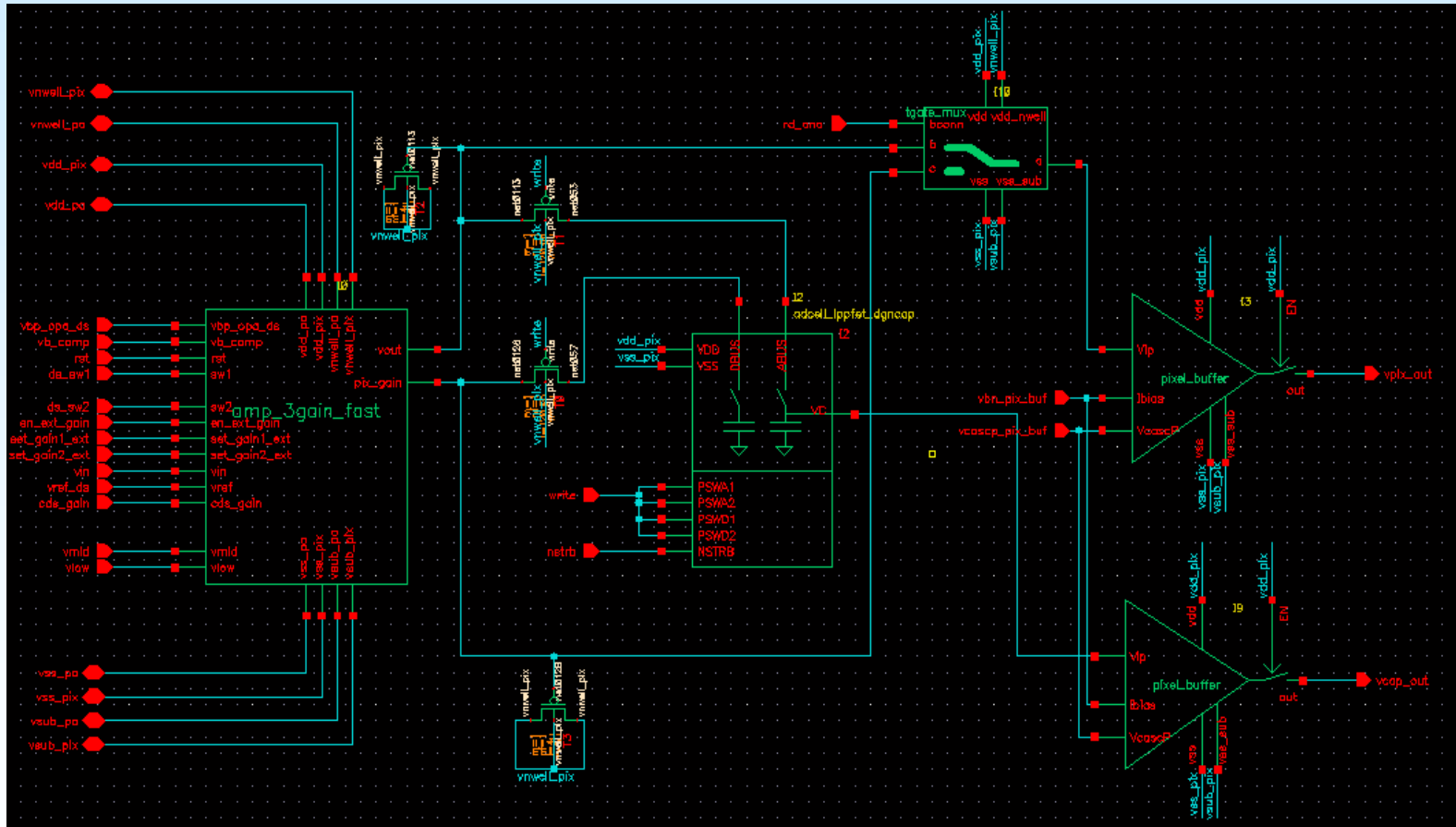
Analog current off-chip Driver

Analog current off-chip Driver

- Single ended input -> differential output
- Settling time < 20 ns with RI = 1K Ohm, CI = 2 pF.
- Linearity error < 1.2% with an input voltage range of
  0.5 V – 1.0 V.
- Current consumption ≈ 2 mA for a fully differential output .

Write/read storage cell

Write/read storage cell

- The speed to access the storage cell is limited by the switches in the storage cell, and is becoming a bottleneck.
- Using a negative gate voltage to improve the access speed is needed.
- A test circuit including the preamplifier and storage cell was implemented in Gotthard test chip.

Future work

- The bottleneck of speed is accessing the storage cell. Implementing level-shifts has to be done.

- The circuits on the PCB are needed for simulating the output drivers with the load close to the real situation.