Development of Radiation Hard Si Pixel Sensors for the 4th Generation Photon Science Experiment at XFEL

Ajay K. Srivastava[a, 1] , E. Fretwurst[a], R.Klanner[a], I. Pintilie[c], J. Zhang [a,b]

[a]*Institute for Experimental Physics, University of Hamburg, Hamburg 22761, Germany*

Internal note (within AGIPD collaboration)

Abstract—Science at the European XFEL (x-ray Free Electron Laser) requires precision pixel detectors which need to withstand a dose of up to 1 GGy of 12 keV X-ray (10^{16} γ/cm^3/pixel) for three years operation. Test structures, eg. CMOS capacitors and CMOS gated diodes, fabricated by CiS, Erfurt, Germany have been irradiated with synchrotron radiation white light source at DESY DORIS III. Capacitance-voltage (C/V), conductance-voltage (G/V), current-voltage (I/V) and Thermally Depolarization Relaxation Current (TDRC) measurements have been performed. From these measurements oxide charge densities (N_{ox}) and interface densities (D_{it}), capture cross-sections of D_{it} (σ_{eff}), width of gaussian σ^{rms}_{it},, and energy level E_c-E_{it} have been extracted and implemented into the semiconductor device simulation program Synopsys TCAD. Results from measurements could be reproduced by TCAD simulation. This experience is used to design radiation tolerant p$^+$n silicon pixel sensors.

***Index Terms*—** Device simulation, radiation damage effects.

1. Introduction

RESEARCH at the European XFEL (X-ray Free Electron Laser) requires pixel sensors with unprecedented performance: Doses of up to 1 GGy 12 keV x-rays and a dynamic range from 1 to 10^5 12 keV photons per sub picoseconds pulse and pixel of (200 μm)^2 area [1].

A lot of progress has already been made in order to understand the radiation hardness of silicon sensors for XFEL environment and the important observation has been found that after a few MGy of irradiations, saturation of charge occurs [2] and on this basis the microscopic parameters proposed for the simulation using experimental results [3].

In XFEL environment (no bulk damage for E_r<300 keV), the surface charges (oxide charges and interface charges) will degrade macroscopic performance of Si sensors: increases of depletion voltage and surface current, change of interstrip capacitance and interstrip resistance. TCAD simulation was used for the understanding of influence on Si microstrip strip sensor from surface charges after 1 and 10 MGy x-ray irradiation. The final goal of the present work is to develop radiation hard Si pixel sensor for Adaptive Gain Integrating Pixel Detector (AGIPD) at XFEL [4].

In this paper, we have shown the detailed comparison between simulations and measurements for non-irradiated and irradiated CMOS capacitor (annealed 60 min 80^{0}C) and Si microstrip sensor. The p$^+$n Si pixel sensor is proposed within Adaptive Gain Integrating Pixel Detector (AGIPD) collaboration.

2. Test structures design and simulation technique

CMOS capacitor (see Fig.1) and AC coupled Si strip test structure sensor (see Fig.2) is used for the detailed comparison with simulation and experimental results and produces x-ray radiation damage results. On this basis, the optimal radial hard Si sensor design is proposed using 2- D synopsys TCAD device simulation [5]. The geometrical and physical paramaters for both designs are described in the Table.1, 2 and Table.3 and 4.

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A.K. Srivastava, E. Fretwurst and R. Klanner is with the Institute for Experimental Physics, University of Hamburg, Hamburg, 22761, Germany (e-mail:ajay.srivastava@desy.de;Eckhart.fretwurst@desy.de; Robert.klanner@desy.de).

[b]J. Zhang is also with Marie Curie Initial Training Network (MC-PAD).

[c]I. Pintilie is with National Institute of Material Physics, Bucharest, Romania.

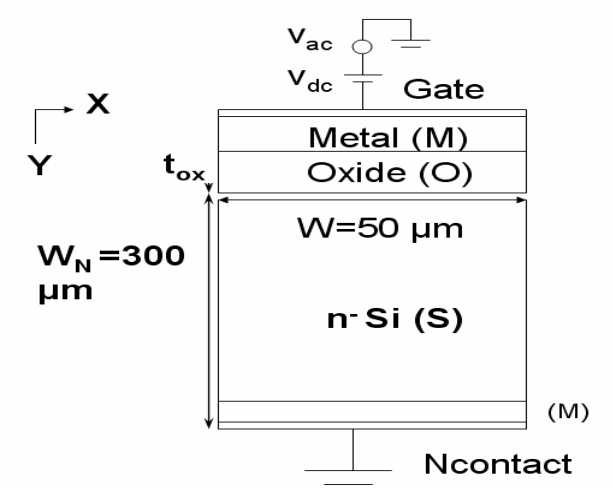


Figure.1: Schematic of the CMOS capacitor for the simulation.

Table.1: List of geometrical parameters for CMOS Capacitor

S.No.	Geometrical paramaters	Values
1.	MOS gate width(W)	10 µm
2.	Diameter	1.5 mm
3.	Full volume of MOS test structure (2-D)	X=10 µm , Y=300 µm
4.	Default gate length (L) in 2-D simulation	1 µm

Table.2: List of physical and biasing parameters for CMOS capacitor.

S.No.	Physical paramaters	Values
1.	Oxide thickness (t_{ox})	0.405 µm
2.	Net doping concentration in bulk Si	$1.38x10^{12}$ cm-3
3.	Depth of net doping (d_d) [µm]	20-300 µm
4.	Doping concentration near to Si-SiO_2 interface	$7.5 x10^{11}$ cm-3
5.	Depth of surface doping profile (d_s) [µm]	0-20 µm
5.	Gate voltage (V_g)	Depends upon N^{fix}_{ox} /V_{fb}, D_{it}
6.	AC voltage (V_{AC})	0.1V
7.	Frequency (f)	10, 100 kHz

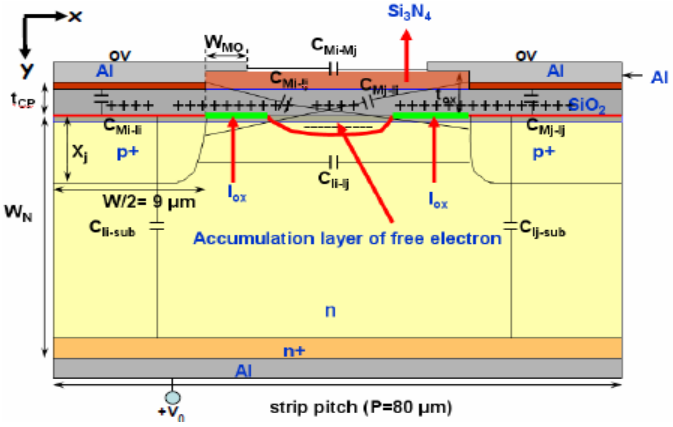


Figure.2: Schematic of 2 strips AC coupled Si sensor for the simulation.

Table.3: List of geometrical parameters for AC coupled Si sensor

S.No.	Geometrical paramaters	Values
1.	2 strip sensor pitch (P)	80 µm
2.	Width of strip (W)	18 µm
3.	Length of strips (L)	7.8mm
4.	Default length of strips (L) in 2-D simulation	1 µm
5.	Total area of 98 strips	0.643 cm^2
6.	Full volume of 2 strip sensors (2-D)	X=80 µm , Y=282 µm

Table.4 : List of physical and biasing parameters for AC coupled Si sensor

S.No.	Physical paramaters	Values
1.	Coupling oxide +nitride thickness (t_{ep})	200 nm+50 nm
2.	Field oxide +nitride thickness (t_{ox})	300 nm+50 nm
3.	Net doping concentration in bulk Si	$8.1x10^{11}$ cm-3
4.	Junction depth (X_j)	1 µm
5.	Thickness of n^+ (W_{n+})	1 µm
6.	Thickness of Al strips	1 µm
7.	Width of metal-overhang	1 µm
5.	Bias voltage (V_g)	100V, 500V
6.	AC voltage (V_{AC})	0.1V
7.	Frequency (f)	100 kHz, 1 MHz

2.1 Specification of the p^+n Si pixel sensor for AGIPD

The specs. for the sensors are given below:

Main specifications

- radiation tolerance: 0 ... 1 GGy
- $I_{pixel} < 1$ nA; $I_{tot} < 3$ mA (minimize I_{dark})
- inter-pixel capacitance $C_{pixel} < 0.5$ pF (minimize C_{pixel})
- flatness: < 25 mm (minimize flatness)
- minimize dead region (aim for 0.5 mm)
- breakdown voltage > 500 V
- interstrip resistance > 20 GΩ

In this note, we have optimized the pixel design for breakdown voltage V_{BD}, Interstrip capacitance C_{int}, Surface current I_{ox}, and Interstrip resistance R_{int} and minimize the region of low electric field for no charge loss.

2.1.1 AGIPD sensor

The p^+n Si pixel sensor will be circular bump bonded with usually Indium of diameter (10-25 micron) to the automatic gain switching readout ASIC electronics (see Fig.3). The window will open in the final passivation for bump bonding with each pixel.
The detailed descriptions of readout ASIC electronics are presented in [4].

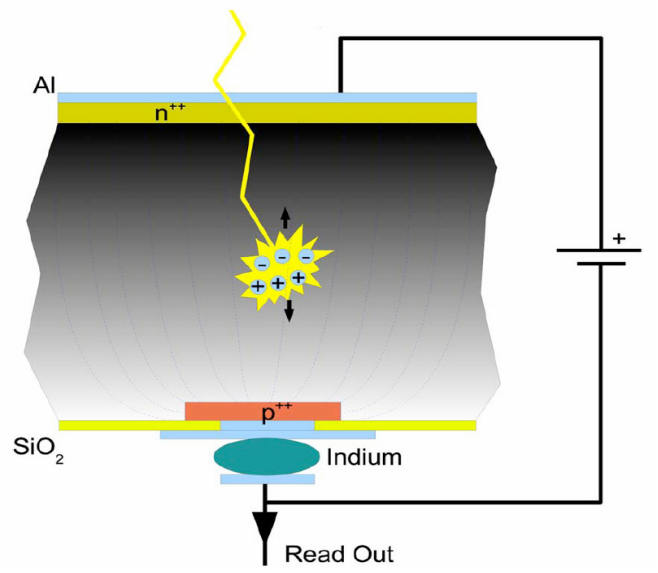


Figure.3: cross-section of one DC coupled p^+n Si pixel sensor (bump bonded with readout).

3. Physics of breakdown voltage V_{BD}, Interstrip capacitance C_{int}, Surface current I_{ox}, and Interstrip resistance R_{int}

In reverse bias p^+n silicon pixel sensor, the voltage at which the current increases sharply is called the avalanche breakdown voltage V_{BD}. The critical electric field for the breakdown is 3 x 10^5 V/cm and the impact ionization coefficient (α_n, or α_p or both) should be equal to one.
The interstrip capacitance is the creation of series noise in the readout ASIC electronics therefore the sensor design should be carefully optimized. The cross-talk is also measurable and this is calculated by ratio of capacitance of neighbors with total capacitance i.e. sum of detector capacitance and bump bonding capacitance, and charge sensitive preamplifier capacitance. In an array of silicon pixel sensor, the interstrip capacitance is the sum of the all neighboring adjacent pixels and diagonal pixels. A lot of work has been already done to calculate the C_{int} in 3x 3 pixel array using analytical methods, HSPICE circuit simulator, and 2-D, 3-D ISE TCAD [6-7].
In an irradiated silicon pixel sensor by 12 keV X-rays, the flow of dark surface current I_{ox} is also the creation of parallel shot noise in the readout ASIC electronics due to high interface trap density at Si-SiO_2 interface of sensor.
The measurement of interstrip resistance R_{int} gives the qualitatively information about spatial resolution.

4. Strategy for simulation

It is known from previous studies [8] on pixel sensor that the C_{int} is strongly influenced by the gap between the pixel and also dark surface current I_{ox} increases with gap. Therefore it is important to optimized the gap for 500 V operation without any avalanche breakdown in order to limit charge explosion effect (plasma of high e/h densities) [9], low $C_{int,}$ dark current (within specs) and R_{int} > 20 GΩ.

The p^+n Si pixel sensor for the outer region will be investigated later.

In the first step, we have compared the experimental and simulation result using TCAD device simulation of non-irradiated CMOS capacitor. The fixed oxide charge density (Nox) is used from the experiment. The parameters are determined i.e interface densities (D_{it}), width of gaussian $\sigma^{rms}_{it,}$, and energy level E_c-$E_{it,}$ and the calculated capture cross-sections of D_{it} (σ_{eff} = 7 x 10^{-17} cm^2) are used here from the non-irradiated gated diode measurements [Sri]. For non-irradiated CMOS capacitor, it is very difficult to get the microscopic parameters from experiment.

In the next step, we have compared with experimental data on 60 min 80^0C 5 MGy irradiated CMOS capacitor. The fixed oxide charge densities (N_{ox}), interface densities (D_{it}), width of gaussian $\sigma^{rms}_{it,}$, and energy level E_c-E_{it} is used from the

experiment and the calculated capture cross-sections of D_{it} (σ_{eff} = 7 x 10^{-17} cm^2) are used here from the non-irradiated and irradiated gated diode measurements [Sri[2]]. It is believed that the capture cross-section of D_{it} changes with time and after some time it will attain the pre- damage value [10].

It has been found that the slope of the irradiated C/V_g curve is very sensitive to the interface densities (D_{it}), width of gaussian σ^{rms}_{it},, and energy level E_c-$E_{it.}$

In order to get good qualitatively agreement with experimental data, we have refine the microscopic parameters specially width of gaussian $\sigma^{rms}_{it.}$ and E_c-E_{it} within ± 0.05 eV (from experimentally measured TDRC, D_{it} versus E_c-E_{it}) . It should be noted the taken values are within the experimental error and it the precise accurate estimation of σ^{rms}_{it} is not possible because of the offset problem of the TDRC curve. The model calculations should be carefully performed for the shallower and deeper interface trap to get microscopic parameters using the complex RC network inside the CMOS capacitor because surface damage is a complex business of surface charge effects.

The following two Gaussian interface trap model are used in TCAD device simulation [11].

6. Simulation results

In this section, we have presented the simulation results performed within the framework of the AGIPD collaboration for the development of adaptive gain integrated hybrid silicon pixel detectors at XFEL.

6.1 Simulation results of test structure

The doping profiles of CMOS capacitors are extracted from the experiment (C-V and G-V) and verified using analytical expressions [Sri]. The knowledge of accurate doping profiles is important for C-V modeling of CMOS capacitor.
In the first set of simulation results, we have shown the detailed comparison of experimental results and simulation results of non-irradiated CMOS capacitor. The results are shown in Fig.4. The following microscopic parameters are extracted from TCAD: D_{it}=2.66x10^{11} cm^{-2} eV^{-1}, E_c-E_{it}=0.4 eV, σ^{rms}_{it} = 0.1 eV. It can be seen that the capacitance is well described qualitatively in all regions at 10, and 100 kHz. The flatband shift is also observed with increasing frequency from 10 to 100 kHz due to high value of interface trap density. It is also observed that there is also change of capacitance in strong accumulation region of CMOS capacitor. This is due to the uncorrected series resistance of undepleted bulk of Si [Sri] or may be due to unwanted dielectric loosy layer formed and increases at Si- SiO_2 interface with increasing frequency and thus gives an unobvious effect i.e. decreases of oxide capacitance in strong accumulation [Sri].

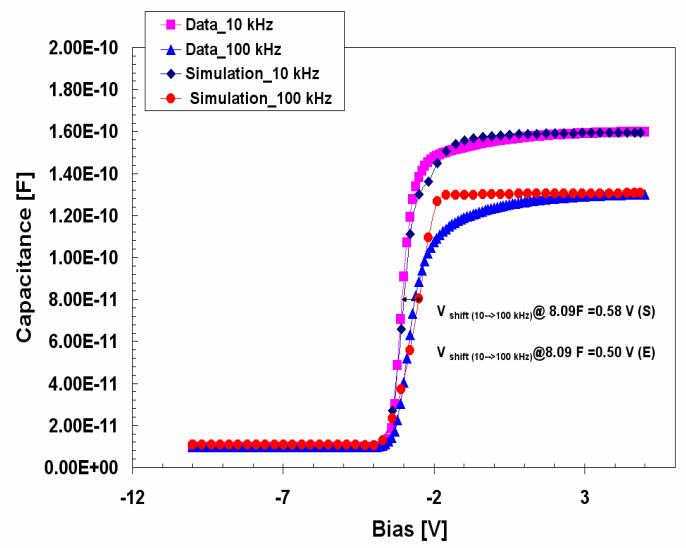
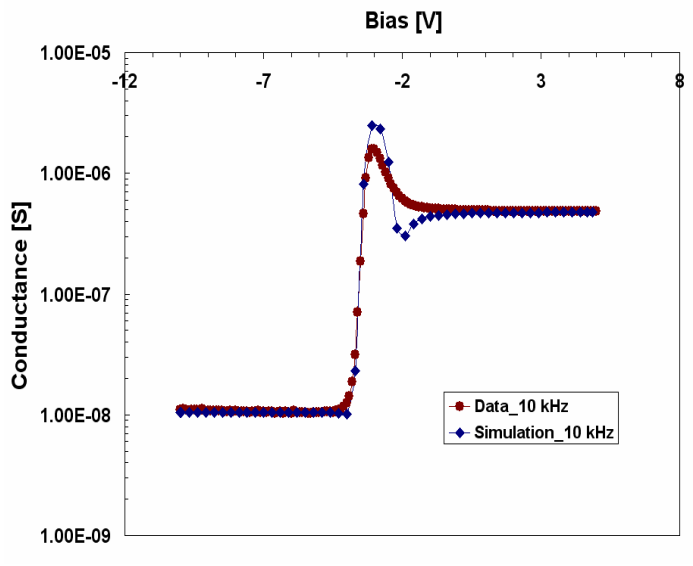


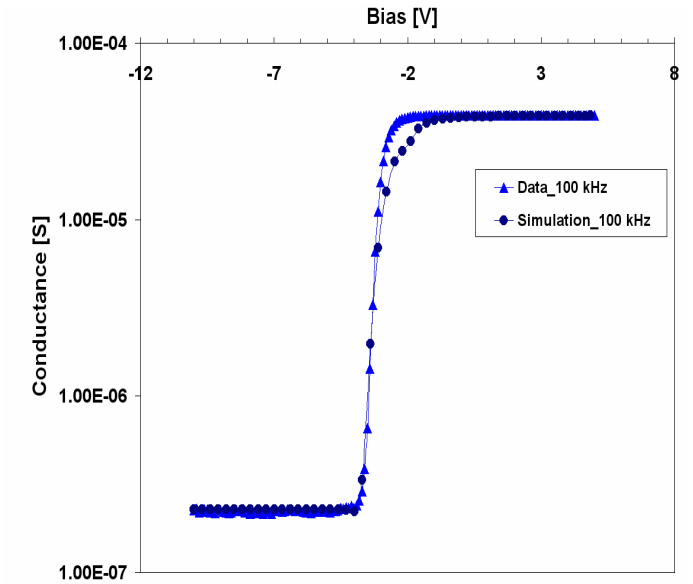
Figure.4: Comparision of experiment and simulation of capacitance-voltage (C/V_g) for non-irradiated CMOS capacitor at 1 and 100 kHz frequency.

The comparison of experimental and simulated conductance–voltage (G-V) characteristics of non- irradiated CMOS capacitor is shown in Fig.5 (a, and b) at 10 and 100 kHz.
Here we have also explained the importance of G-V characteristics for surface charge effects. The three regions (G_{acc}, G_{peak} and G_{inv}) of G-V curve are already described in our first preliminary note on non-irradiated CMOS capacitor [Sri]. Here I have discussed our observation on the basis of simulation results. G_{acc} is depend on the series resistance of the undepleted bulk of Si and G_{peak} gives the information about the charge carrier distribution at Si-SiO_2 interface. Whereas, G_{inv} is strongly depend on the Temperature of measurement and also doping in the space charge region. It is observed that G_{acc}, G_{peak} and G_{inv} increases with frequency. The good agreements in G_{acc}, G_{peak} and G_{inv} with experimental results are only possible in the presence of accurate doping profile and microscopic parameters. This is strongly verified our observed microscopic parameters for non-irradiated CMOS capacitor.
It is noted that the conductance is well described qualitaveley in the accumulation, depletion and inversion region and the peak range problem occurs due to sharply decrease of conductance in the accumulation region at 10 kHz. The reason is possibly due to the measurements because the previous measurement on gated diode shows the simulated G-V curve at 10 kHz [Sri].

[2] Sri is referenced by [11].



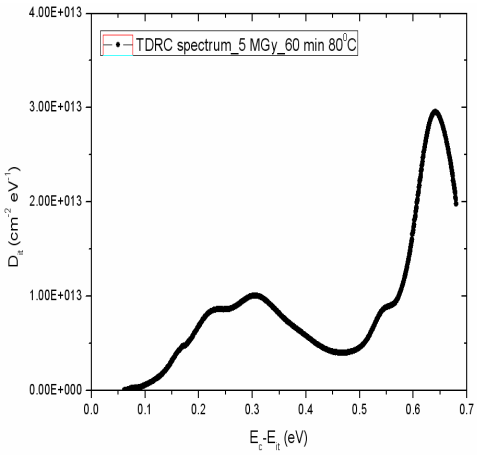
(a)



(b)

Figure.5: Comparison of experiment and simulation of conductance-voltage (G/V_g) for non-irradiated CMOS capacitor at (a) 1 and (b) 100 kHz frequency.

Now, we have compared the experimental result of 60 min 80^0C annealed 5 MGy irradiated CMOS capacitor with simulation. The date was taken from TDRC measurement (see Fig.6a). The strategy used the same as per non-irradiated CMOS capacitor: firstly to compare with simulation and then refine E_c-E_{it}, σ^{rms}_{it} (close to experimental value) in order to get good agreement in C/V and G/V (see Fig.6a and b).



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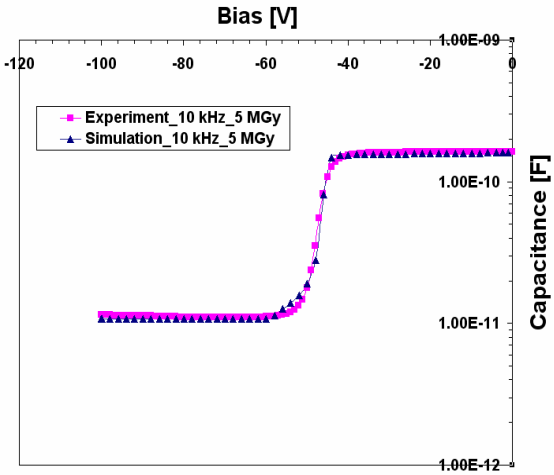

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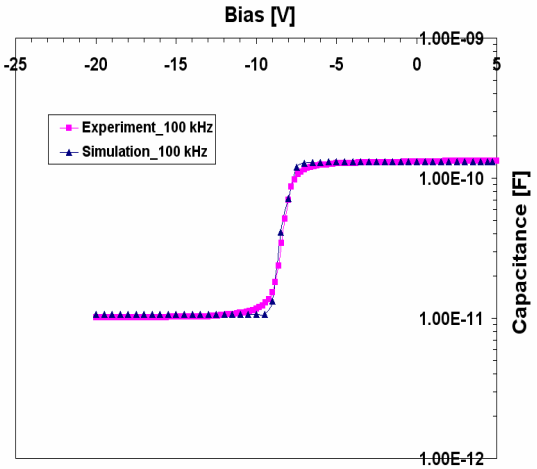
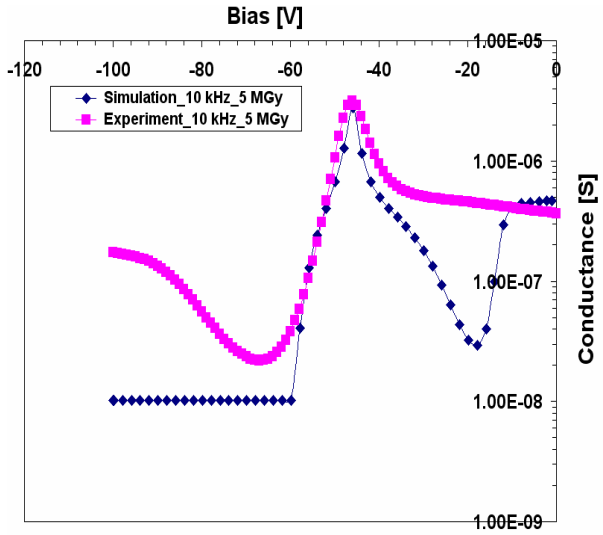


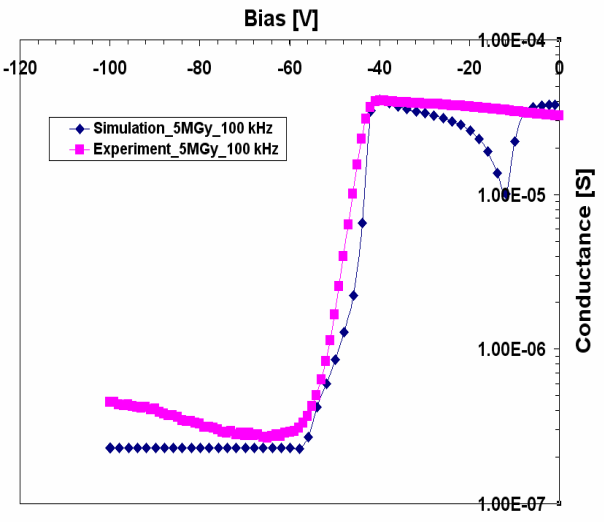
(c)

Figure.6: (a) TDRC measurement result and comparisons of experiment and simulation of capacitance-voltage (C/V_g) for 5 MGy irradiated CMOS capacitor after 60 min 80^0C at (b) 1 and (c) 100 kHz frequency.

For 5 MGy irradiated CMOS capacitor, the C/V curve is in good agreement with experimental results for the following parameters: microscopic defect: Acceptor, E_c-E_{it}: 0.35 eV, Gaussian distribution σ^{rms}_{it}: 0.06791 eV and Donor, E_c-E_{it}: 0.60 eV , Gaussian distribution σ^{rms}_{it} : 0.0065 eV with N_{ox}=2.3 x 10^{12} cm^{-2} and Acceptor, D_{it}=1x10^{13} cm^{-2} eV^{-1} , Donor, D_{it}=4x10^{13} cm^{-2} eV^{-1}.
The comparison of experiment with simulation for G-V characteristics is shown in Fig.7 and b.



(a)



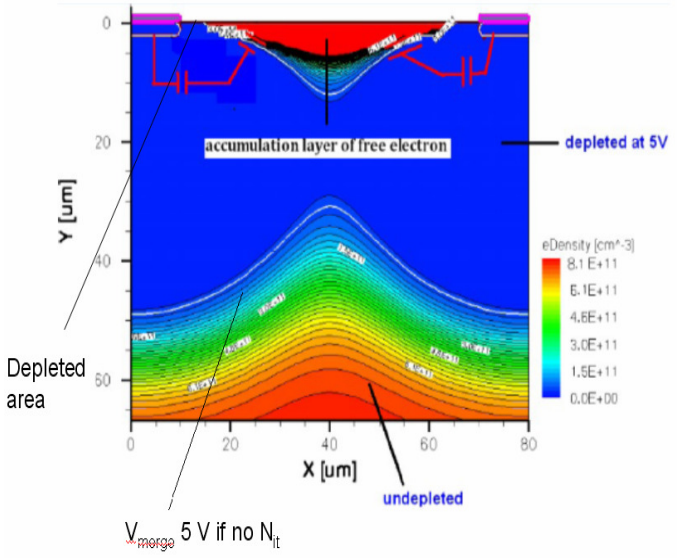
(b)

Figure.7: Comparision of experiment and simulation of capacitance-voltage (G/V_g) for 5 MGy irradiated CMOS capacitor after 60 min 80^0C at (a) 1 and (b) 100 kHz frequency.

The G-V curve (G_{peak}) is qualitatively good agreement in simulation at 10 and 100 kHz frequency. In experimental measured G-V curve, G_{inv} is increasing at 10 and 100 kHz frequency, the reason is still not clear. In simulation, it seems to be constant as expected like from non-irradiated CMOS capacitor. In simulated G-V curve, in accumulation region of CMOS capacitor, G_{acc} is attaining the same positions as expected at 10 and 100 kHz like from non-irradiated CMOS capacitor but in experimental curve, it is not observed.
Finally, the results are cross-checked with analytical expressions [Sri].

6.2 Simulation results of test structure AC coupled p^+n silicon strip sensor

In the framework of AGIPD collaboration, 98 Si strip sensors were irradiated by 10 keV x-ray doses of 1 MGy and 10 MGy and annealed up to 60 min 80^0C. The simulator is used to compare the experimental results of dark current, total back-plane capacitance, and interstrip capacitance with simulation results and present x-ray radiation damage results. In order to check accuracy of simulator and validation of out design, the simulation results are verified using analytical expressions for leakage current, back-plane capacitance, interstrip capacitance for ideal case when there is no fixed charge in the oxide and at Si-SiO_2 interface. The good agreement in leakage current but for back-plane, interstrip, and total detector capacitance within the agreement of 10-23-30 % with analytical expressions for the w/p=0.2 [12]. It is important to mention that the 100 % agreement is achieved for w/p=0.6 (see section 6.3).
The microscopic defects (N_{ox}, D_{it}) for 1 MGy and 10 MGy were taken from experiment [3] and E_c-E_{it} and gaussian distribution σ^{rms}_{it} for both shallower and deeper interface trap from previous simulation. There is no comparison with simulation has been made for 1 and 10 MGy with C/V and G/V because of unavailability of data.
The following parameters: microscopic defect: Acceptor, E_c-E_{it}: 0.35 eV, Gaussian distribution σ^{rms}_{it}: 0.06791 eV and Donor, E_c-E_{it}: 0.60 eV , Gaussian distribution σ^{rms}_{it} : 0.0065 eV with N_{ox}=2.08 x 10^{12} cm^{-2} and Acceptor, D_{it}=4.2x10^{12} cm^{-2} eV^{-1} , Acceptor, D_{it}=1x10^{13} cm^{-2} eV^{-1} were used only for 1MGy. The capture cross-sections of both interface trap (shallower and deeper), σ_{eff}= 7 x 10^{-17} cm^2 were used.



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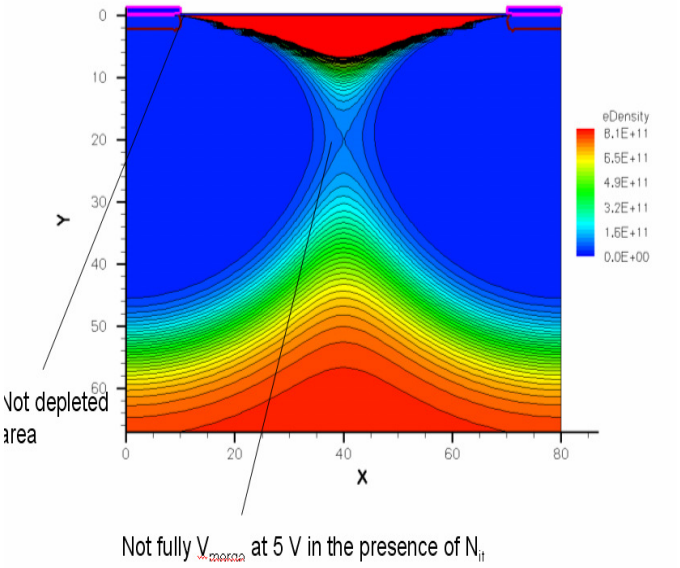
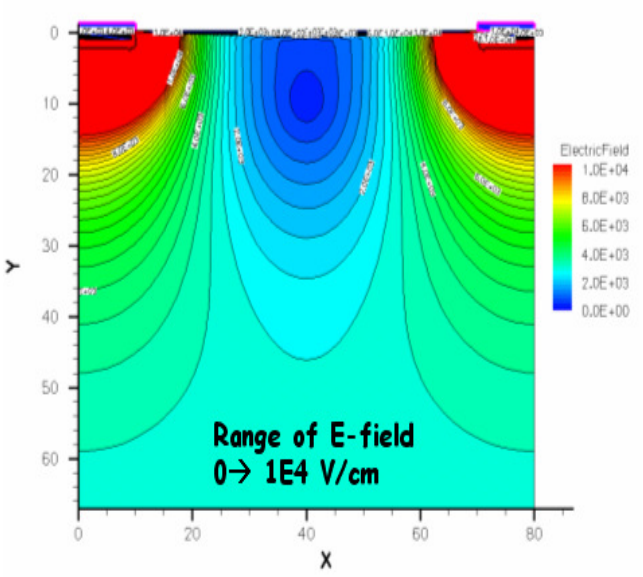


(b)

Figure.8: e-density inside AC coupled Si strip sensor at 5V (a) Nox ~ 1 MGy, D_{it} = 0 (b) Nox and D_{it} both ~ 1 MGy irradiated doses

In 1 MGy irradiated sensor, the effect of Nox and D_{it} on depletion behavior is clearly shown in Fig.8. In the presence of N_{ox} (no D_{it}), the depletion merge (V_{merge}) at around 5 V but in the presence of N_{ox}+ D_{it} both, V_{merge} improved upto few volts (1-2 V). V_{merge} can be seen in 1/C2 versus bias characterstics of sensor.



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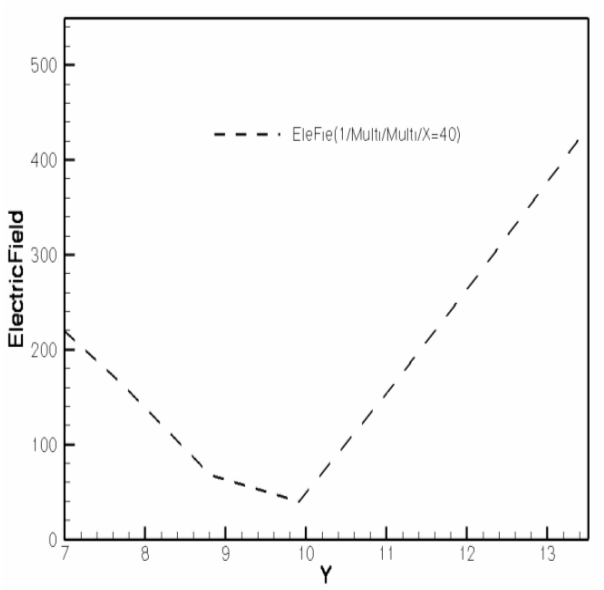
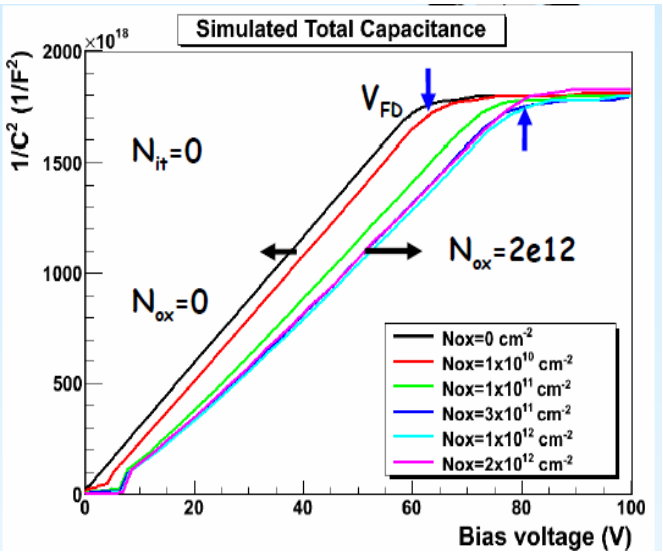


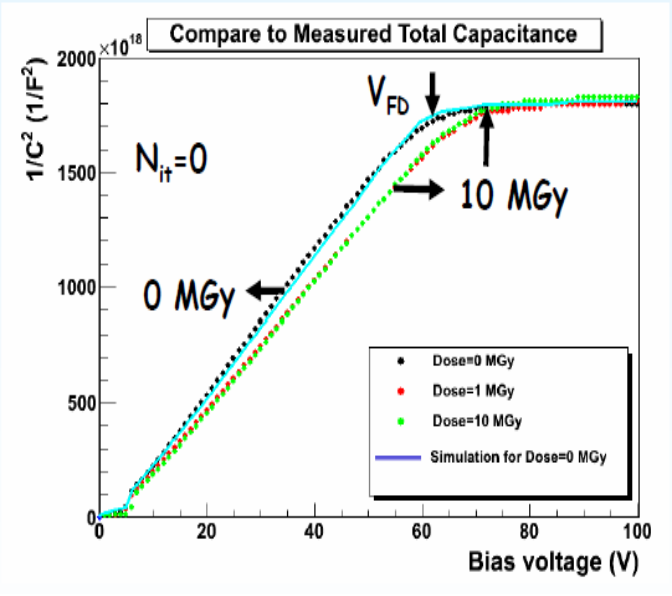
(b)

Figure.9: Electric field distribution inside 1 MGy irradiated AC coupled Si strip sensor at 100 V (a) E-field (range of E-field is 0 to 1x 10^4 V/cm.) (b) Electric field versus depth at X=40 µm.

The electric field minimum has been found at Y= 10 µm (see Fig.9a and b). This can be exempted from any loss of charge. This is because of no electric field lines are passing through the small volume of the sensor.



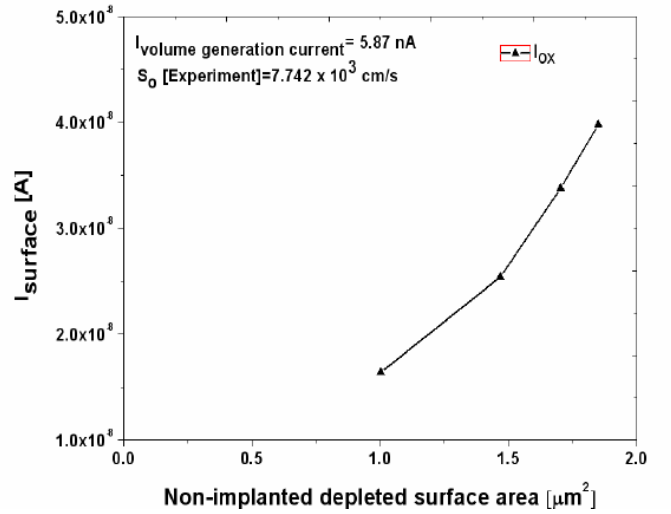
(a)



(b)

Figure.10: (a)$1/C^2$ versus bias voltage for different fixed oxide charge (D_{it}=0) at 100 kHz frequency (b) $1/C^2$ versus bias voltage for different irradiated sensor. Comparison of experiment with non-irradiated sensor for N_{ox}=2x 10^{10} cm^{-2} at 100 kHz frequency.

It is shown in Fig.10a, N_{ox} increases (0 to 1 x 10^{11} cm^{-2}) the full depletion voltage up to 10-15 V because of delayed depletion depth and for further increase in N_{ox}, V_{FD} saturate.
he good agreement in experimental data and simulation is observed in total back-plane capacitance of non-irradiated strip sensor for N_{ox}= 2x 10^{10} cm^{-2}. The effect of (N_{ox} + D_{it}) in irradiated sensors on full depletion voltage can be seen in Fig.10b. In 1, 10 MGy irradiated sensor (N_{ox} + D_{it}), there is a 1-2 V of full depletion voltage changes and it is due to change of an effective oxide charges at Si-SiO_2 interface.



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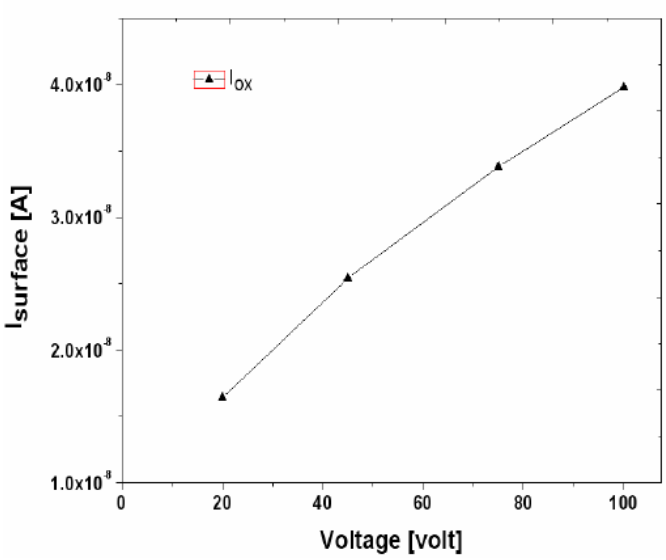


(b)

Figure.11: (a) Surface generation/recombination current versus non-implanted surface depleted area and (b) voltage in 1 MGy irradiated sensor

It has been found that the generation/recombination surface current increases with non-implanted surface depleted area and also with voltage. There is a disagreement in expected experimental current of 9 µA/cm^2. This is because of the high value of the effective capture cross-section of the shallower and deeper traps. In order to make a good agreement in simulated surface current at every voltage with experimental

data, we have tune the effective capture cross-section of interface traps.
Firstly, it is important to see the effect of boundary conditions on surface current in order to verify the suitable boundary condition for the present simulation approach.

6.2.1 Effect on surface current in Gate boundary condition and Neumann boundary condition in 5 MGy irradiated (60^0C 80 min annealed)

When gate boundary conditions used it has been found that the surface current increases with voltage but saturate up to 60 V whereas in experimental the surface current continuously increases with voltage.
Therefore, Neumann boundary condition is an appropriate boundary condition for the comparison of simulated surface current with experimental data.

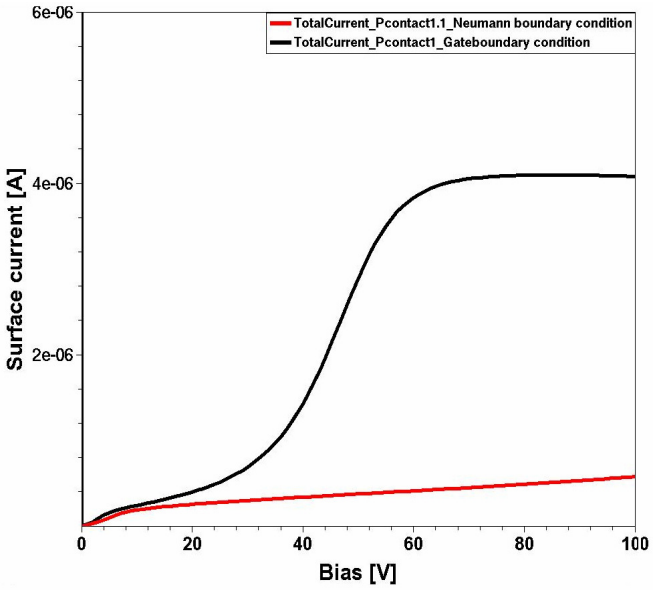
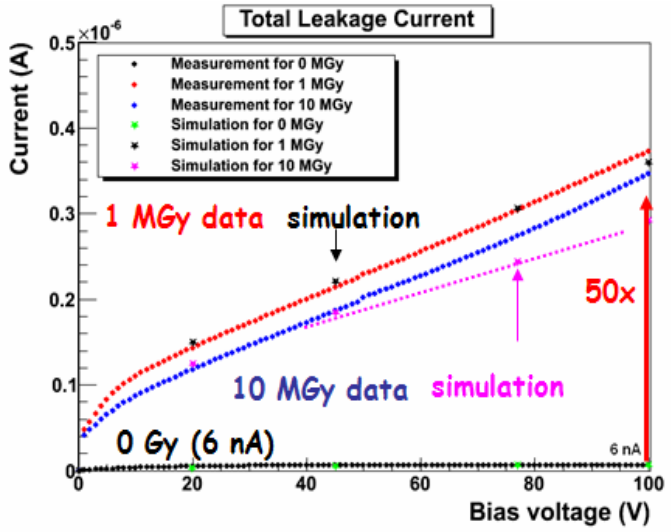


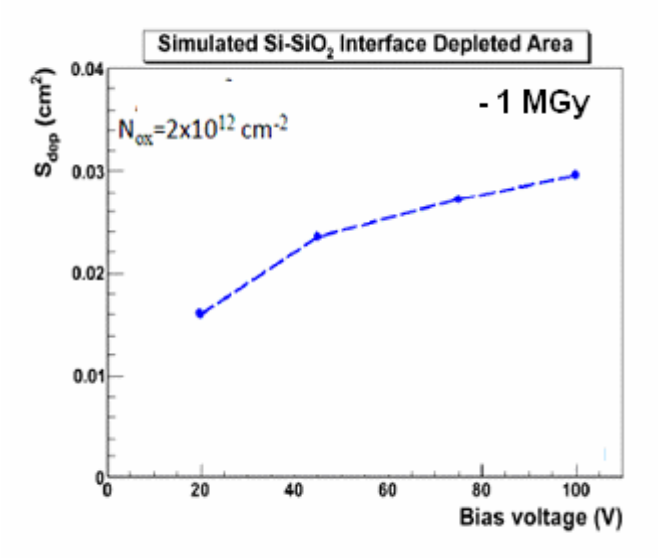
Figure.12: Surface current versus bias voltage for gate and Neumann boundary condition.

6.2.2 Comparison of simulated surface current with experimental data in an irradiated sensor

In order to make good agreement in simulation surface current and experimental data, we have tune the capture cross-sections of both interface trap and for the value of 2.75×10^{-15} cm^2. The surface current of 9 µA/cm^2 is in good agreement with the measurement results on gated diode (see Fig.13) [2].



(a)



(b)

Figure.13: Comparison of (a) simulated surface current and experiment for 1and 10 MGy irradiated sensor and (b) Total normalized depleted area for 98 strip AC coupled sensor.

6.2.3 Model parameters and comparison of simulated total back-plane capacitance (serial and parallel) and interstrip capacitance (serial and parallel) with experimental data in an irradiated sensor

There is model calculation performed which is based on the experiment result and analytical expressions given in books and on this basis; two level interface trap microscopic parameters for 1, 5 and 10 MGy irradiated doses are derived.

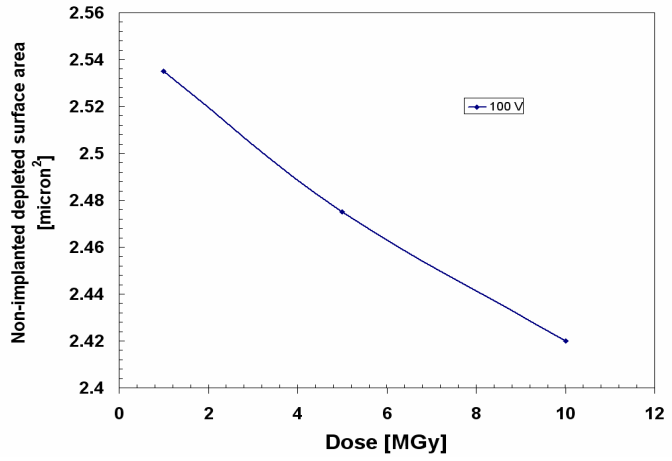
The parameters are shown in the below. The value of N_{ox} below is shown for immediately after irradiation where as D_{it} and other parameters are shown after annealing.

Parameters for 1, 5 and 10 MGy:
1 MGy: N_{ox}= 3.3x10^{12} cm^{-2}
• E_c -E_{it} = 0.354 eV (acceptor)
- Gauss with rms = 0.1016 eV
- σ_{eff} = 1x10^{-16} cm^2
- D_{it} (0.354 eV) = 6.438x10^{12} cm^{-2} eV^{-1}
• E_c -E_{it} = 0.636 eV (acceptor)
- Gauss with rms = 0.045 eV
- σ_{eff} = 4x10^{-15} cm^2
- Dit (0.636 eV) = 7.118*1012 cm-2 eV-1

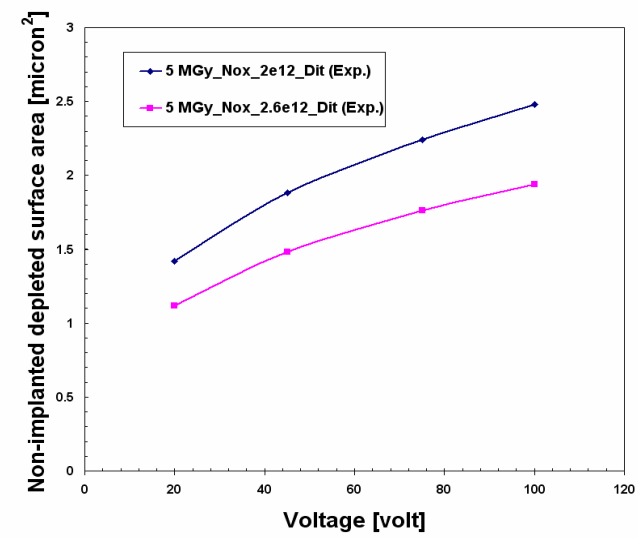
5 MGy: N_{ox}= 3.1x10^{12} cm^{-2}
• E_c -E_{it} = 0.354 eV (acceptor)
- Gauss with rms = 0.1016 eV
- σ_{eff} = 1x10^{-16} cm^2
- D_{it} (0.354 eV) = 5.861x10^{12} cm^{-2} eV^{-1}
• E_c -E_{it} = 0.636 eV (acceptor)
- Gauss with rms = 0.045 eV
- σ_{eff} = 4x10^{-15} cm^2
- D_{it} (0.636 eV) = 6.728x10^{12} cm^{-2} eV^{-1}

10 MGy: N_{ox}= 3.0x10^{12} cm^{-2}
• E_c -E_{it} = 0.354 eV (acceptor)
- Gauss with rms = 0.1016 eV
- σ_{eff} = 1x10^{-16} cm^2
- D_{it} (0.354 eV) = 5.024x10^{12} cm^{-2} eV^{-1}
• E_c -E_{it} = 0.636 eV (acceptor)
- Gauss with rms = 0.045 eV
- σ_{eff} = 4x10^{-15} cm^2
- D_{it} (0.636 eV) = 6.337x10^{12} cm^{-2} eV^{-1}

Therefore, in simulation we have used the N_{ox} = 2.3 x 10^{12} , 2.1x10^{12}, 2.0x10^{12} cm^{-2} for 1 MGy, 5 MGy and 10 MGy irradiated detectors (60 min 80^{0}C).



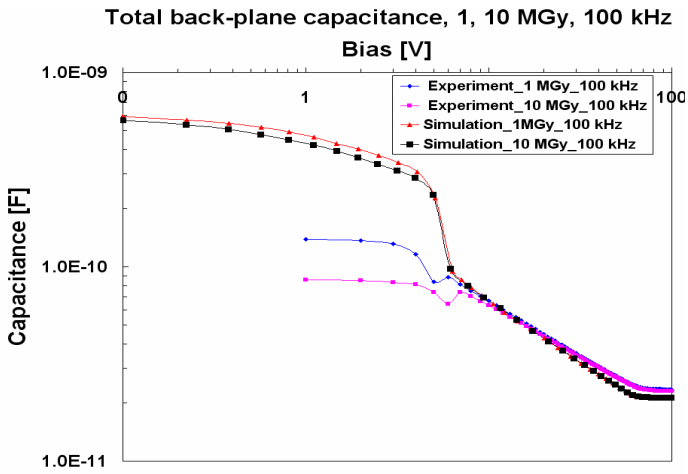
(a)



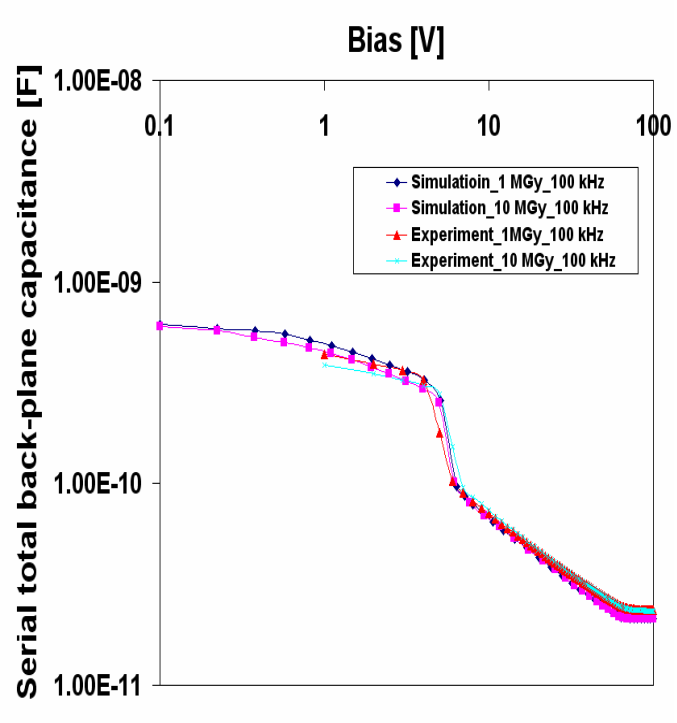
(b)

Figure.15: (a) Change of non-implanted depleted surface are with irradiated doses (b) Change of non-implanted depleted surface area with voltage with Nox is as running parameter.

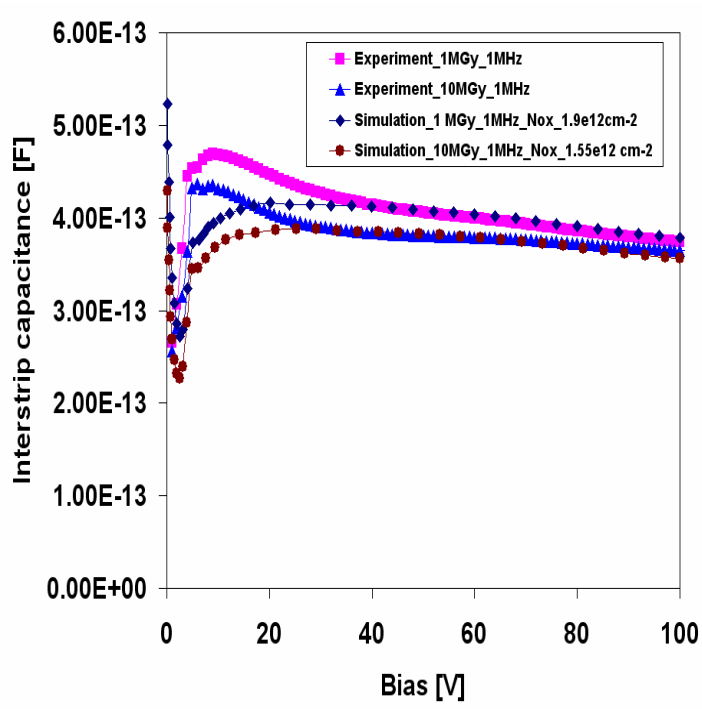
It has been found that in Fig.15 a there is a little decrease of non-implanted depleted surface area observed with increases of doses and thus we can say surface current will also little decrease and in fig.5, it can be seen that the non-implanted depleted surface area decreases with increasing N_{ox} for fixed D_{it} for 5 MGy irradiated sensors .



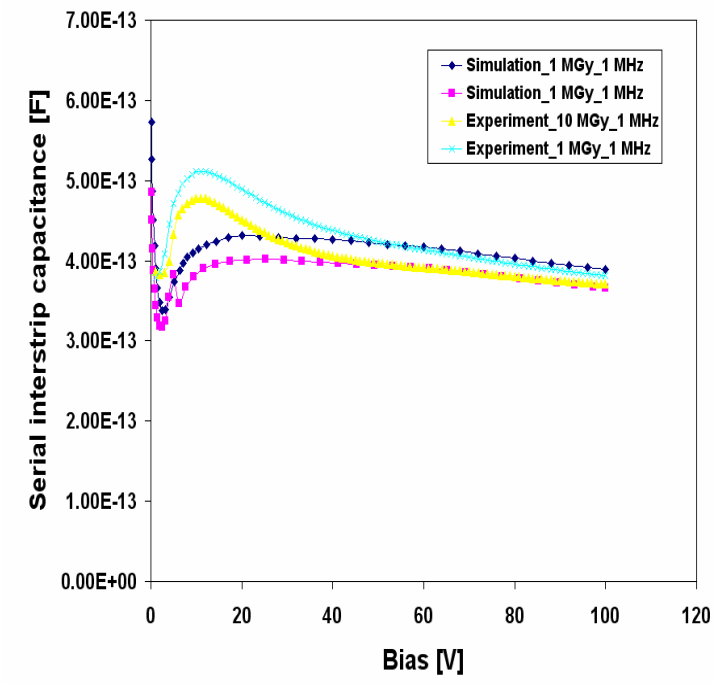
(a)



(b)



(c)



(d)

Figure.16 Total back-plane capacitance versus bias voltage for 1 MGy and 10 MGy irradiated and annealed (60 min 80^0C) at 100 kHz (a) parallel (b) serial and interstrip capacitances versus voltage for 1 MGy and 10 MGy irradiated and annealed (60 min 80^0C) at 1 MHz (c) parallel (d) serial .

It is well known that the capacitance can be measured in the parallel and serial mode. The serial mode is well accepted because of the appropriate model for simple pn junction. Here we have shown the results for both modes, it has been found that because of series resistance effect at different frequency (100 kHz) and at 1 MHz, the effect of series resistance will be very less, serial total back plane and interstrip capacitance capacitance is in qualitatively good agreement with simulated result.

In order to make it in good agreement with experimental data on 1 MGy and 10 MGy, the following N_{ox}= $1.9x10^{12}$ cm^{-2} for 1 MGy and N_{ox}=$1.55x10^{12}$ cm^{-2} for 10 MGy are extracted from simulation for same D_{it}.

This is in good agreement with our observation on annealed sensors and also that can be accepted because from the experimental measurements, it is difficult to get exact value of N_{ox} in the presence of C/V hysteresis effect in CMOS capacitor (due to N_{ox} mobile charge).

It should be noted that the exact information of D_{it}+ N_{ox} is important for the comparison with interstrip capacitance and for total back-plane capacitance, D_{it} and knowledge of accurate doping profile (uniform/non-uniform) is required.

6.3 Simulation results of p^+n Silicon pixel sensor for AGIPD

In the frame work of the AGIPD collaboration, 200x200 μm^2 of the pixel size is taken as a first consideration. This present simulation approach optimized the design parameters for the higher and stable performance of the sensors in terms of low interstip capacitance, dark current within the specs, and acceptable interstrip resistance in the XFEL environment.

In fig,17, the schematic of the cross-section of the two pixel sensor is shown. The pixel is made on 3-5 kΩ-cm high resistivity n-type FZ Si substrate material of thickness 500 µm and other process parameters are taken in order to keep in mind that there will no influence on the electric field up to 1500 V bias in the presence of surface charge variations and that will protect the sensor from avalanche breakdown. Firstly, we have done two dimensional simulation for an ideal sensor for the leakage current, back-plane capacitance, and interstrip and total back-plane capacitance. The analytical calculation performed for an ideal sensor and the simulation results for the leakage current, $C_{back\text{-}plane}$, C_{int}, and total detector capacitance is in 100% good agreement with theoretical calculation.

The leakage current of 2.56 pA and full depletion voltage of 197 V is found for non-irradiated 200x 200 μm^2 pixel.

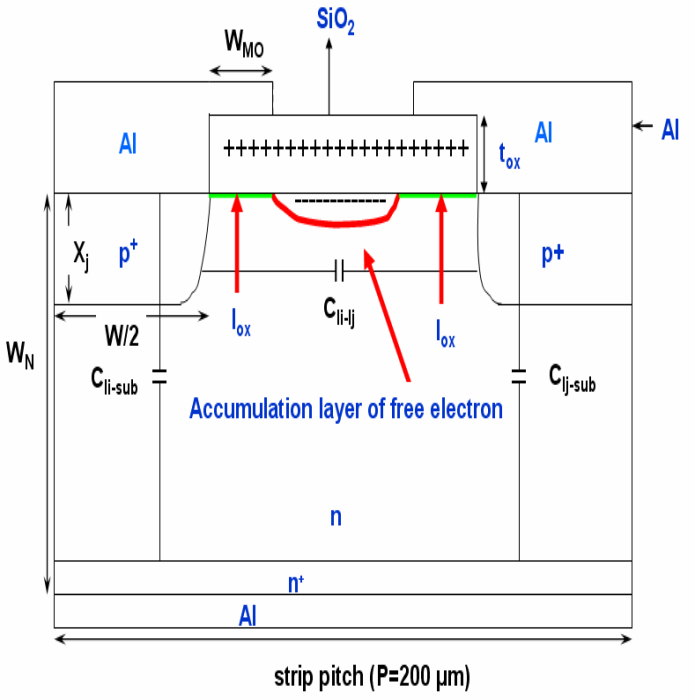
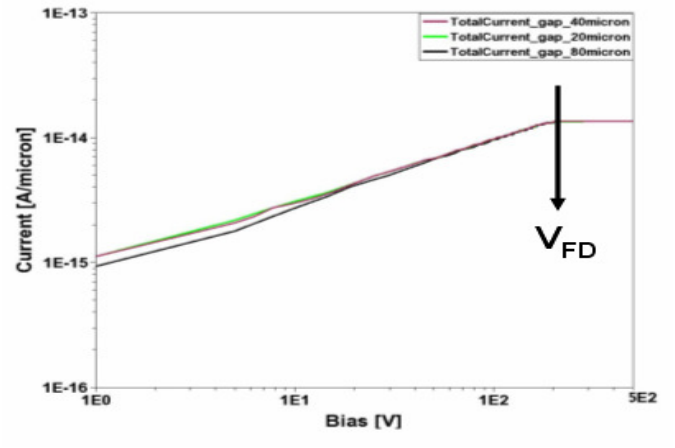
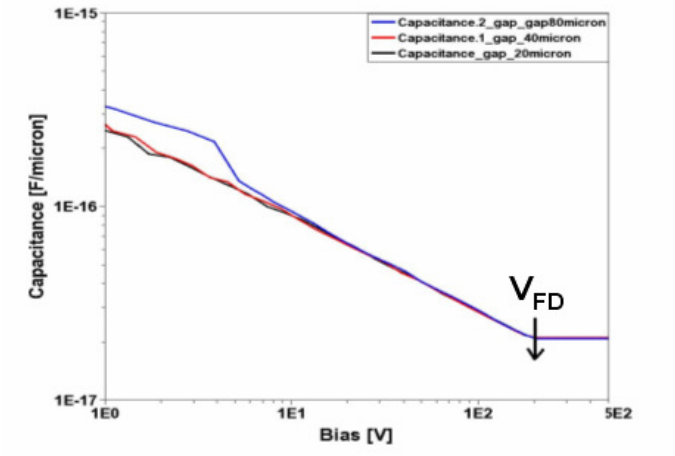


Figure.17: Schematic of the two pixel sensors used in the present simulation work.

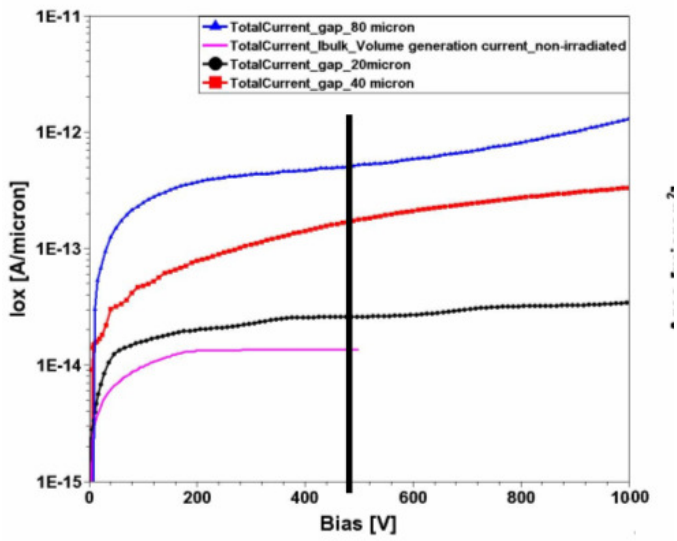


(a)

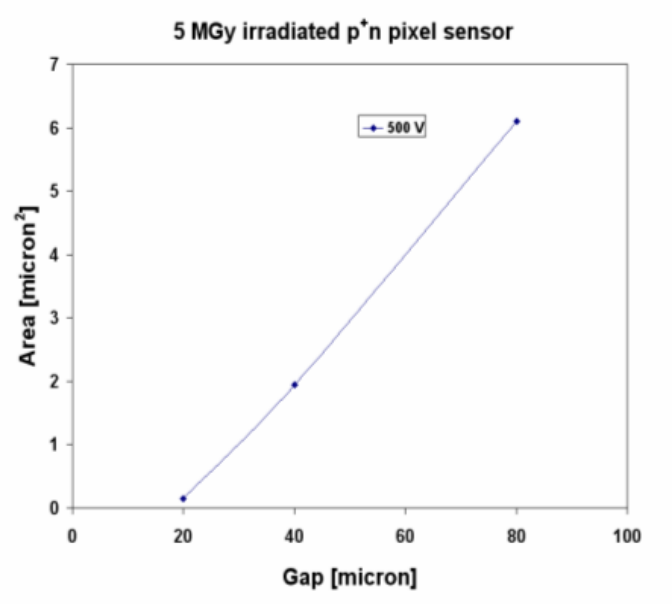


(b)

Figure.18: I-V curve and C-V for the non-irradiated sensor (N_{ox}=3 x 10^{11} cm^{-2}).



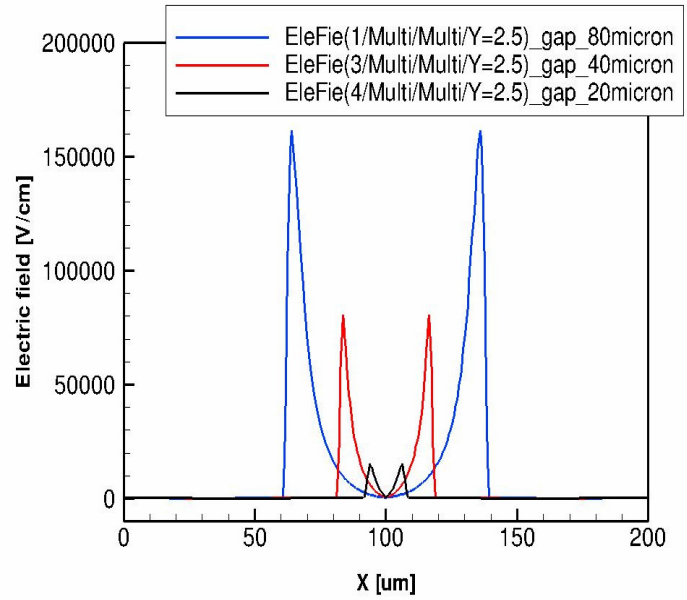
(a)



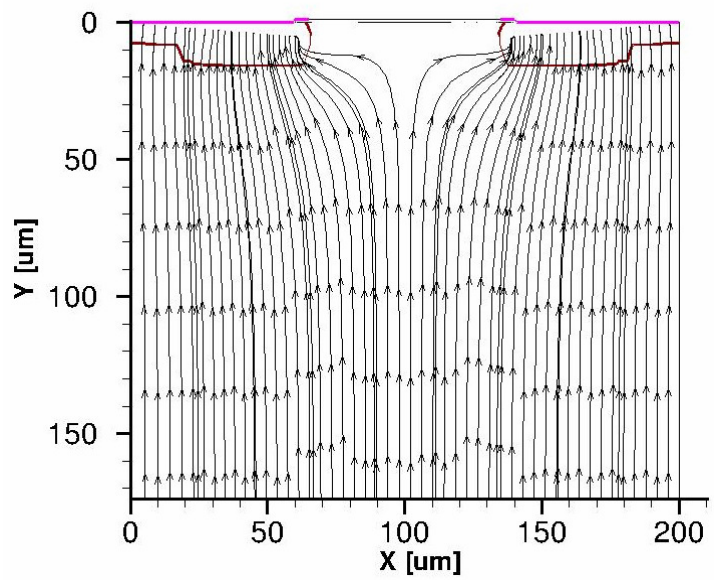
(b)

Figure.19 (a) Surface current versus bias voltage (V_{bias}= 500 V). The gaps between the pixels are as running parameters. (b) Non-implanted depleted area versus gap for 5 MGy irradiated sensor (annealed 60 min 80^0C).

The influence of the gaps on the pixel dark surface current is shown in fig.19a for 5 MGy irradiated sensor (annealed 60 min 80^0C).
It is found that the dark surface current increases with gap this is because of the increases of the non-implanted depleted surface area (see fig.19b). The estimated dark current at 500 V for 80 micron gap is 9 µA/cm^2.



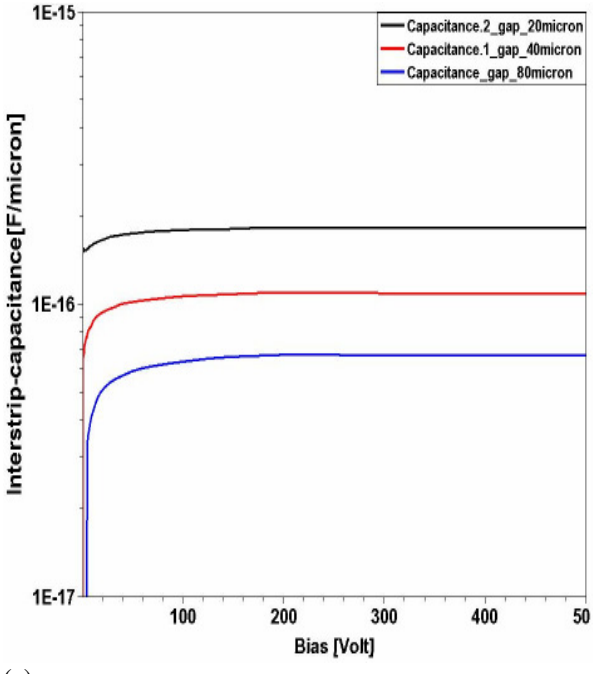
(a)



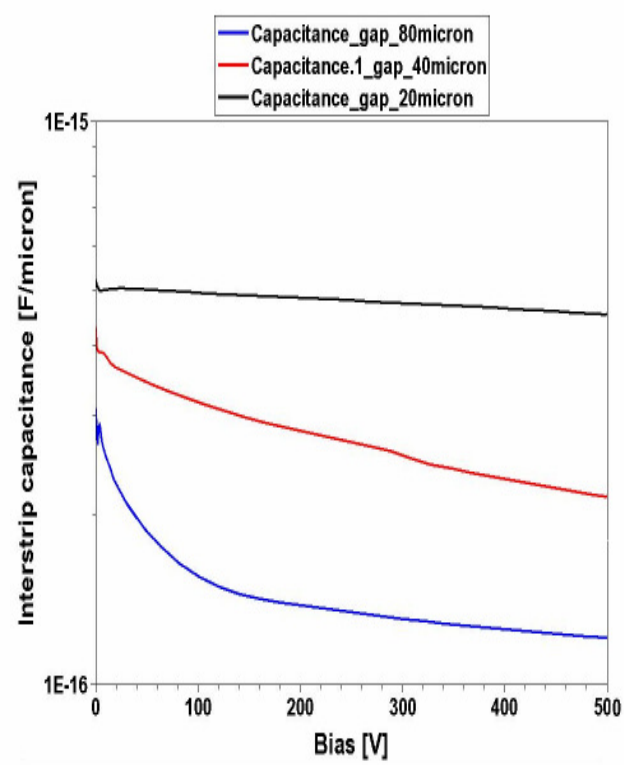
(b)

Figure.20: (a) Surface electric field versus distance X at Y= 6 µm. (b) Electric field lines inside the sensor at 500V.

It is found that the peak amplitude of the electric field at curvature of junction increases (< 200 kV/cm) with gap size as expected and there is a minimum electric field region at the center of the sensor around 10 micron depth from the Si-SiO^2 interface but there is no charge loss expected because of no files lines passing through this area (See fig.20b).



(a)



(b)

Figure.22 Interstrip capacitance versus bias voltage for non-irradiated (a) and 5 MGy irradiated (b)

The interstrip capacitance decreases with increases gap for non-irradiated and irradiated pixel sensor and the minimum interstrip capacitance is obtained for 80 µm gap (see Fig.22). The estimated value of the C_{int} at full depletion for 200x200 μm^2 (sensor pixel array) is 110 fF and the acceptable dark surface current at full depletion is 100 pA for 5 MGy irradiated sensor (annealed 60 min 80^0C).
In Fig.23, I have shown the interstrip resistance verus gap gap for non-irradiated and irradiated pixel sensor (annealed 60 min 80^0C). It is clear that the R_{int} decreases with increases gap and R_{int} for 5 MGy dose is less than the non-irradiated sensor. For 80 µm gap, R_{int} =22 GΩ obtained for 5 MGy irradiated sensor (annealed 60 min 80^0C).

Outlook

In the next step, the aim is to simulate the 3D geometry of the sensor pixel array for the capacitance calculations and compare the simulated results with analytical expressions. The behaviour of C_{int} versus voltage curve for different design with different gaps in the presence of N_{ox}+ D_{it} is always question and in the next work, I will propose the two strip lumped model in order to explain the shape of the curve. The design for the outer region of the pixel sensor will be also performed.

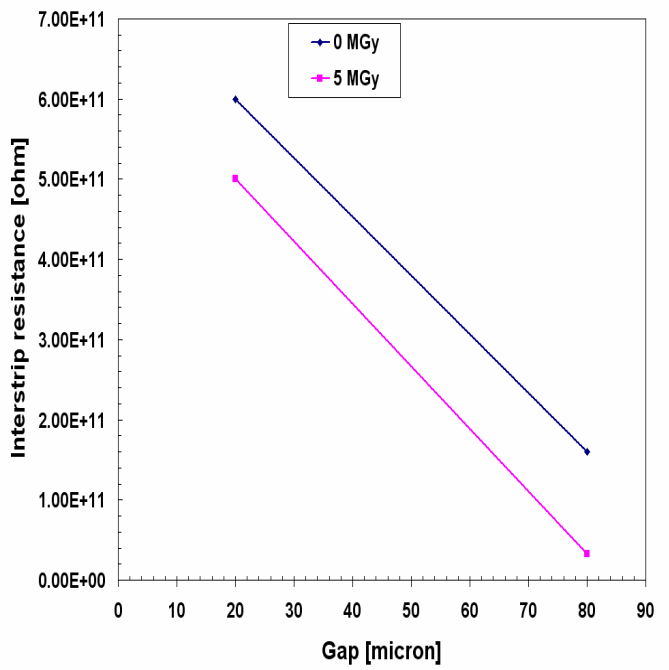


Figure.23: Interstrip resistance versus gap for non-irradiated and 5 MGy irradiated sensor (annealed 60 min 80^0C) at 500 V.

Conclusion

The detailed comparison of simulation is made with the experimental data on different test structures design and a good qualitatively understanding is obtained. On this basis, I have proposed the radiation hard design of p^+n pixel sensor for AGIPD with 80 micron gap for 200x200 μm^2 (sensor pixel array) to reduce the detector load noise (0.21 pF including contribution from bump bonding and automatic gain switching preamplifier load) at the readout of the ASIC electronics that will work up to 500 V with safety margin of 1000V. In this design, there is no chance to tunnel the electron to the oxide so for ASIC electronics; there will no problem of gate leakage current.

ACKNOWLEDGEMENT

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Ajay K. Srivastava s/o Later Durga Prasad Srivastava and Madhur Srivastava was born in Azamgarh (Utter Pradesh), India, on 03rd August 1974. He did Ph.D. degree from the Department of Physics and Astrophysics, University of Delhi, India in 2007. His Ph.D. dissertation mainly concerned with the "characteristics of silicon detector and study of some process in 14 TeV p-p interactions". He did mainly two dimensional numerical modelling of Si strip sensor taken into account with all relevant process and geometrical parameters using 2-D T-CAD process TMA SUPREM-4 and device simulator TMA MEDICI. His dissertation work is also on the experimental measurements i.e. I-V, C-V measurements of the silicon microstrip detector. In 2002, he worked as a Scientist in the Center for Detector and Related Software Technology (CDRST), Department of Physics and Astro physics, University of Delhi, India. During this work, he was responsible for research and development work of Si detectors measurements, (irradiation, development of front end electronics), which was currently fabricated at Bharat Electronics Limited (BEL), Bangalore, India. He worked on PAS measurement at Helsinki Institute of Physics, Finland. At present, he is working as Post-doctoral research scientist in the Institute of Experimental Physics, University of Hamburg, Germany from 2008. Now, he is involved in the two most prestigious experiments i.e. Development of Si sensor for the upgrade of the CMS tracker for the CMS experiment for s-LHC at CERN, Geneva and XFEL (X-Ray Free-Electron Laser) experiment at DESY, Hamburg, Germany. He is doing two-dimensional and three dimensional numerical modelling for surface damage in MOS capacitor, segmented p^+n and n^+n sensors for the AGIPD of the XFEL experiment at DESY, Hamburg, Germany and also perform 2-D and 3-D numerical modelling on new strixel sensors for CEC (Central European Consortium). He has published over than 30 papers in international journals, two CMS note, six national, more than ten international conference reports and proceedings. His research interests are in the general area of the two and three dimensional semiconductor device (Si sensors) modeling and simulation using Synopsys TCAD and I-V and C-V experimental measurement on Si sensors.