WP 2.4: Interface electronics

> **Electronics for the module**

> **Concepts for the quadrant**

> **What about 16 x 16 pixel**

>**Summary**

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HELMHOLTZ ASSOCIATION

AGIPD consortia meeting

DESY

Module electronics: analogue part: connector to backplane

> Better connector: SAMTEC , ERM8-075-01-L-D-RA-K-TR

75 pins/row: Mother and daughter each 150 pins.

SMD right angle: easier to route through impedance controlled.

Frame with some roughness:

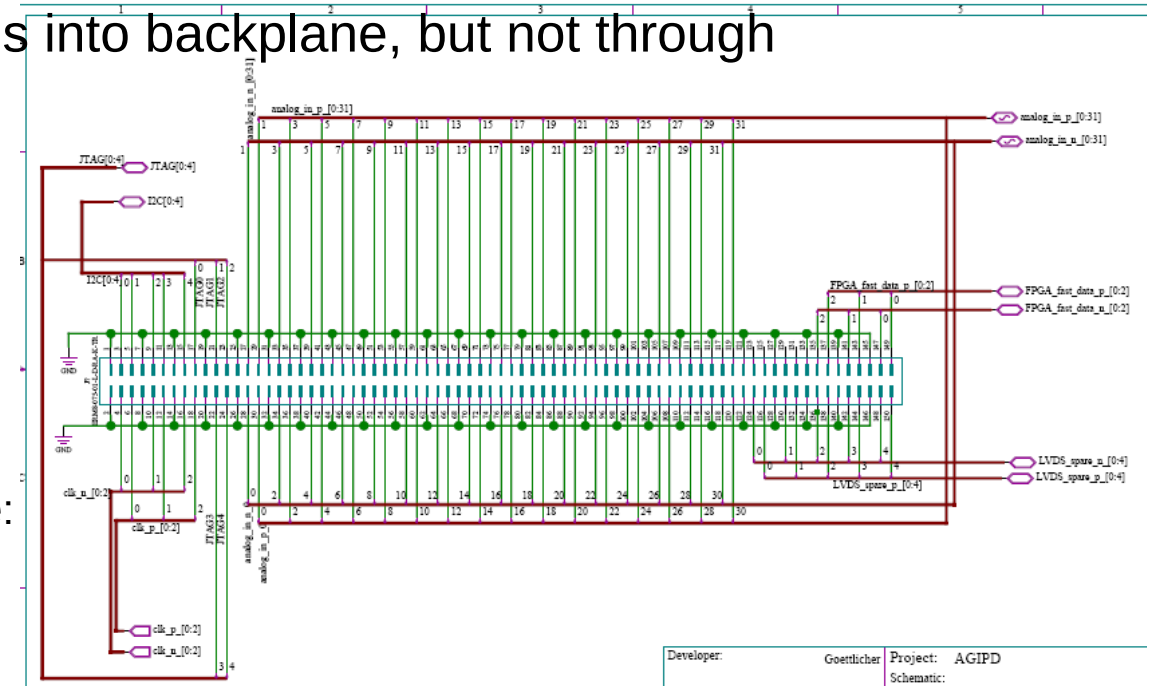
Hope for support of mechanics with some guides.

mechanical pins into backplane, but not through

On Mother:
- 32 analogue
- necessary control from quadrant

Daugther:
- 32 analogue
- a few spares

Other side of backplane:
- to be defined by HDI



Module electronics: analogue part: Signal chain

> Receiver: Differential ±1V

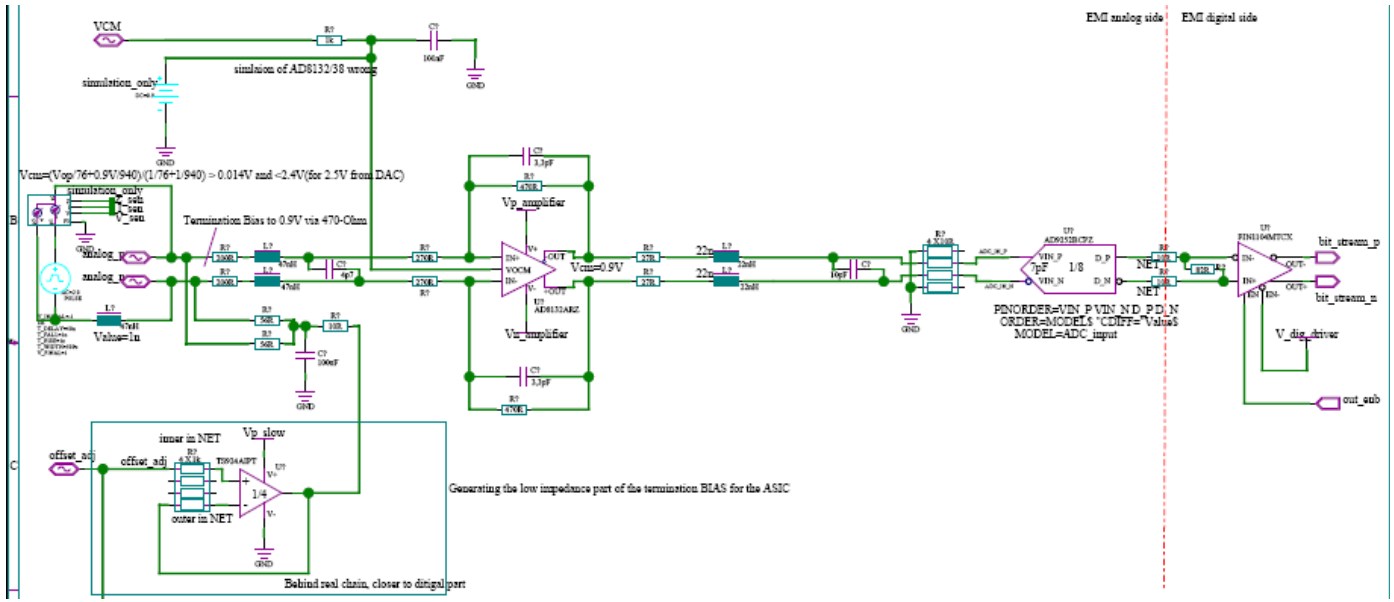
Common mode set by DAC, for flexibility at ASIC.

Filter: Allow settling for ADC within 20ns

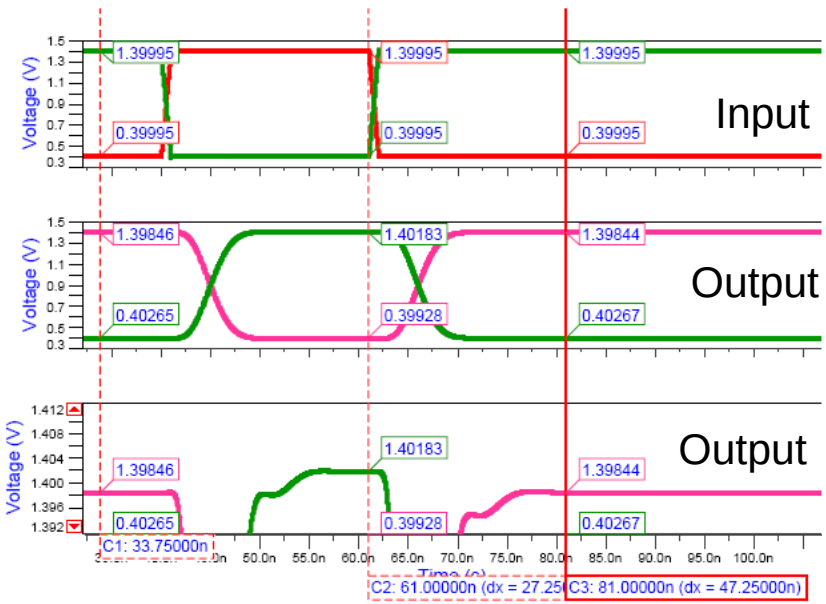
ADC: Multichannel, serial output, 50MS/s

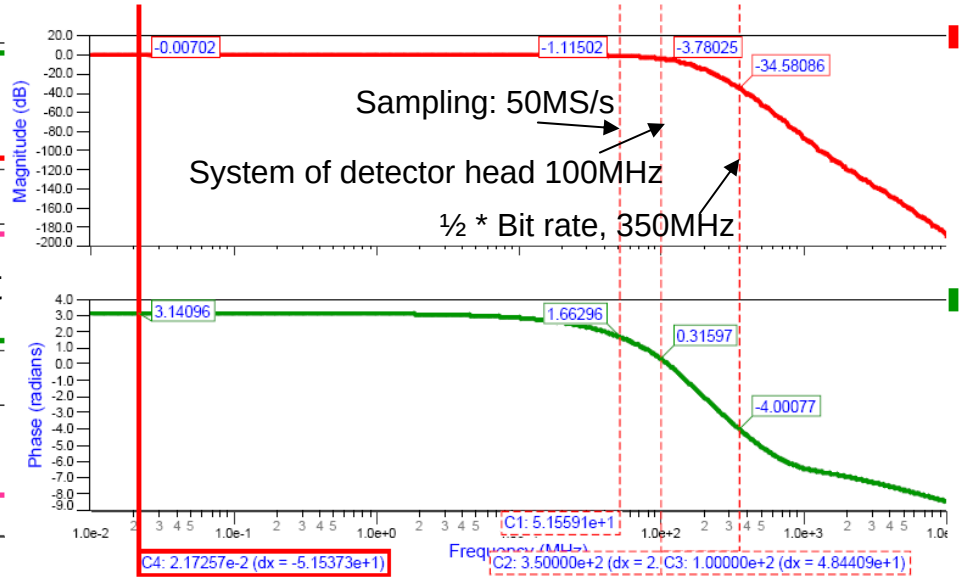
EMI-buffer without antennas on analogue part.

Single high speed amplifier for limited power



Module electronics: analogue part: Signal chain





> Long plateau for digitizing

> Return to baseline 20μV/V-step

…. Simulation

Timing ASIC&ADC to be

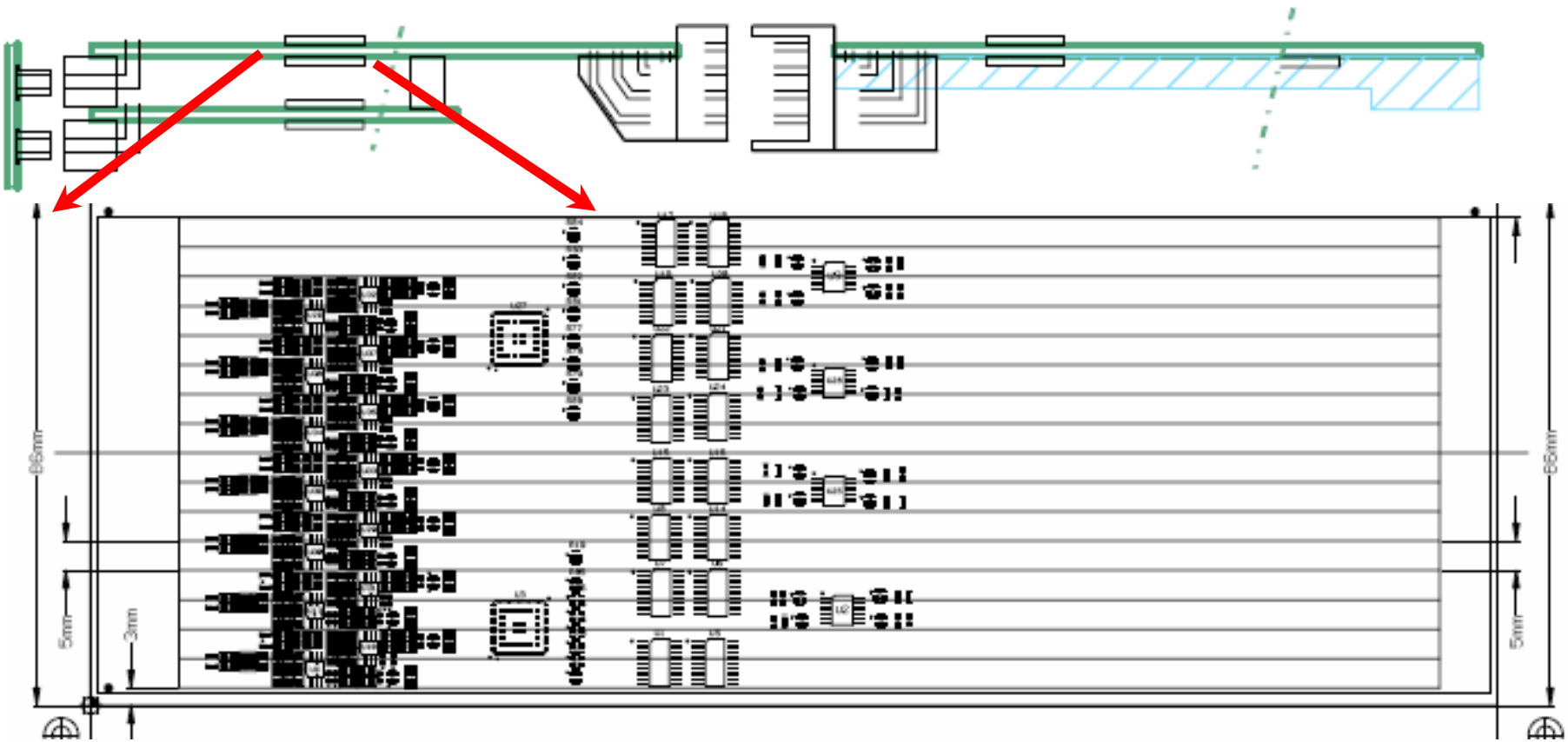
adjustable in quadrant, scan feature

3dB-point already at system-frequency (100MHz)

100dB/decade for high frequencies

Well suppressed bit rate-frequency

Module electronics: analogue part: Signal chain

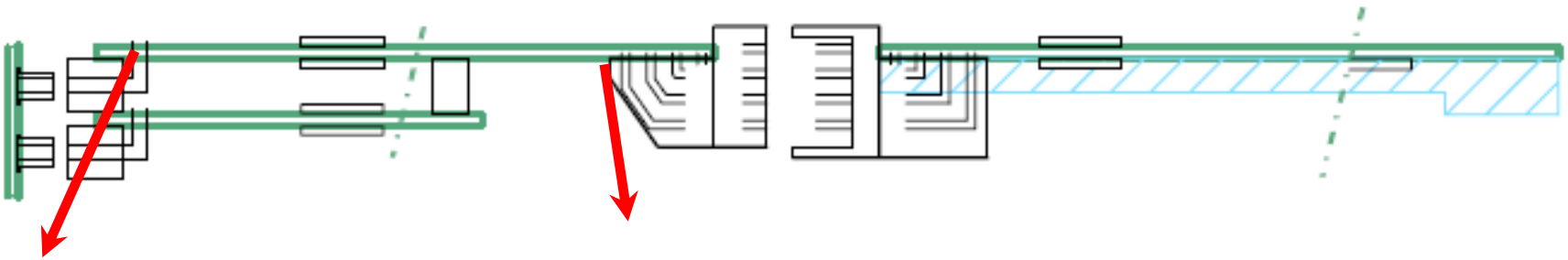


W. Baatz

> Trail of Layout: 16 channel on top, 16 channel on bottom,
> same on daughter: slim line 5mm/channel a bit staggered
> Length first compontent to ADC: ~9cm

> Plan: total board width 95mm, length <300mm

Module electronics: analogue part: Power



> Receiver/filter/ADC-driver needs pos. and neg. voltage

Power budget:	U	I	Comment
> ADC:	1.8V	2*32* 50mA = 3.2A	possible to cycle with train
> Receiver…	2.5V	2*32*10mA = 0.7A	possible to cycle with train
	-2V	…. 0.7A	

➢ *Common mode for termination of ASIC: 2.5V into 50Ω, difference voltage to drive: 1V?*

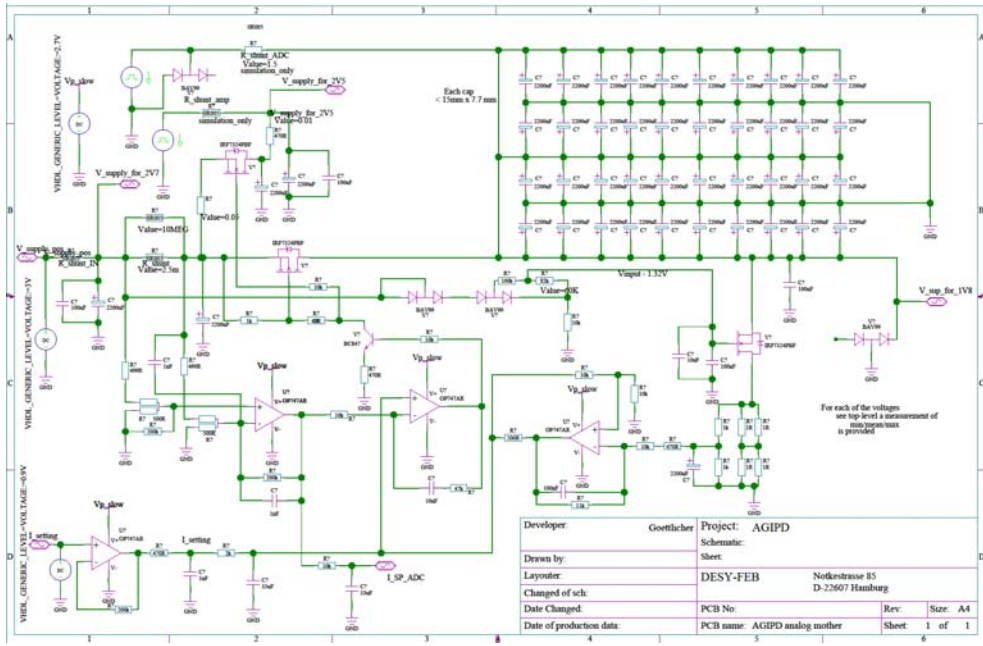
2.5V	*2*32*20mA = 1.3A cycling?, feedback to ASIC?*	
	Is 470Ω to 0.9V not OK + differential 100Ω.	
> I2C-SC	2.7V	low	permanent
> ADC-clk	2.5V	<300mA	possible to cycle with train
> LVDS buffer	3.3V	2*32*11mA= 0.7A	digital quality,from dig. Part

> Two supplies: greater ~ +3V, and ~ -3V(?)

Total power w/o cycling analog part: ~ 20W/module, to be added some spare

Use voltage differences for buffering and cycling the power with avoidance on noise and feedback to power supply.

Module electronics: analogue part: Power



> Algorithm:

Power supply stabilize U
Consumer stabilize I

> Needs

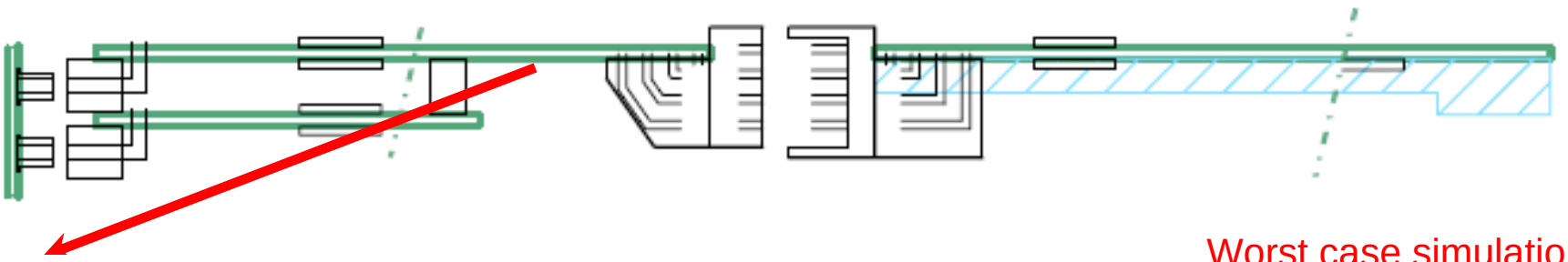
- Capacitor banks
  (Top + bottom)*(mother+daughter)
  ~ 40mm
- I-regulator for charger
  + avoidance of U-saturation

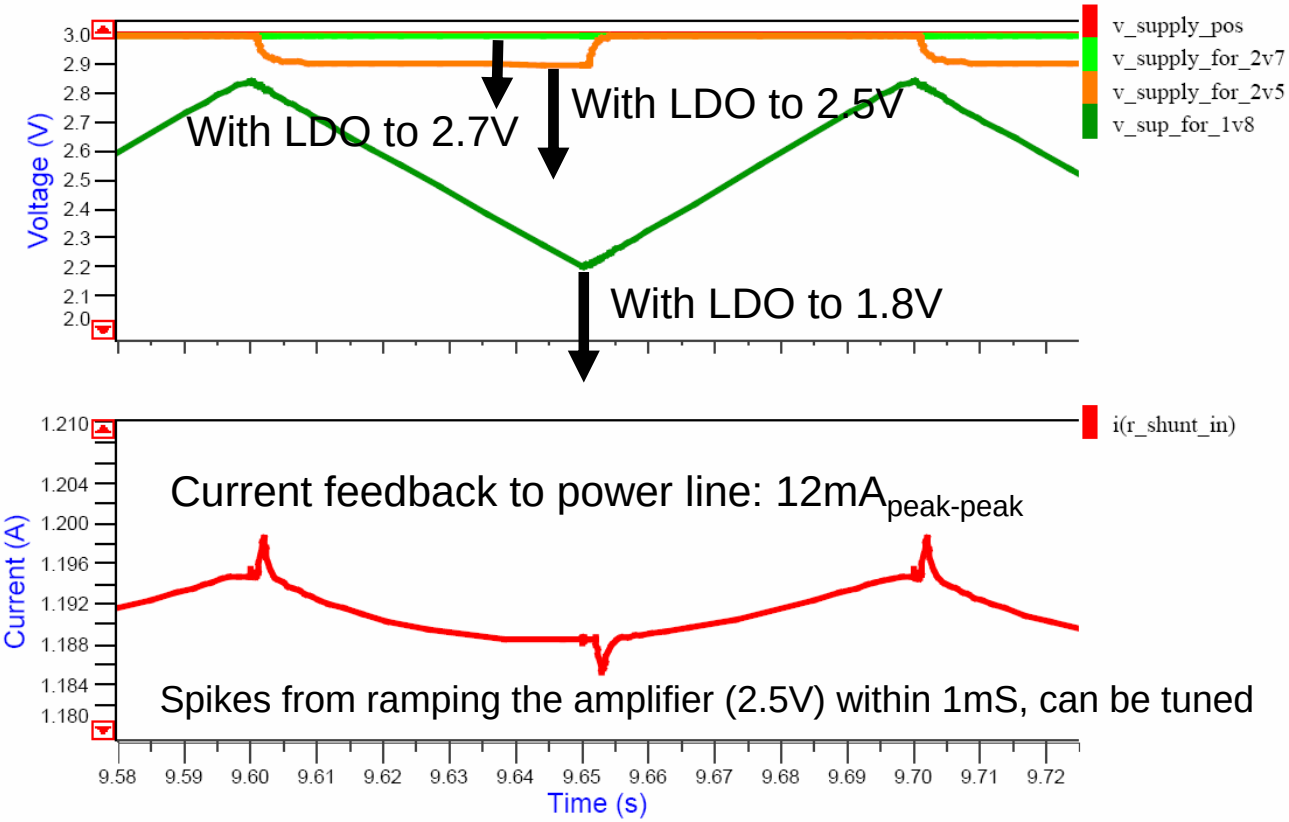
Following LDO-regulators still missing

> Nice and planned: Monitor for minimum/mean/maximum

> Symmetric negative part missing at the moment

Module electronics: analogue part: Power





Worst case simulation

With 50% duty-cycle

400 picture*32*32 pixel

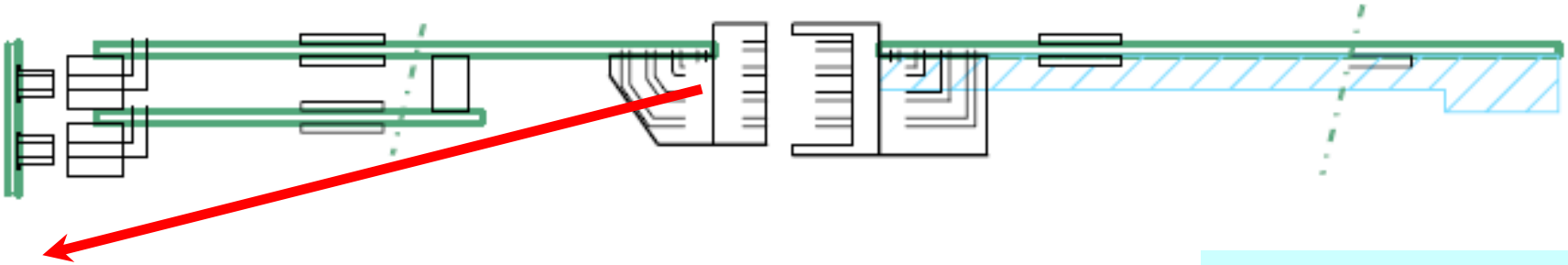
* (sampe+gain)

*20ns/100ms= 16%

Settable operation point via

quadrant-µC ⇒ I2C ⇒ DAC

Module electronics: Connector dig. part



View into the female connector of the analog part

			Impedance controlled								
	connector	row							column		
			shield gh	h	g	shield ef	f	e	shield cd	d	c
PCB-area	1	1	GND_LV	ADC0_data0_p	ADC0_data0_n	GND_LV	ADC0_data1_p	ADC0_data1_n	GND_LV	ADC0_data6_p	ADC0_data6_n
		2	GND_LV	ADC0_data2_p	ADC0_data2_n	GND_LV	ADC0_data3_p	ADC0_data3_n	GND_LV	ADC0_FCO_p	ADC0_FCO_n
		3	GND_LV	ADC0_data4_p	ADC0_data4_n	GND_LV	ADC0_data5_p	ADC0_data5_n	GND_LV	ADC0_DCO_p	ADC0_DCO_n
		4	GND_LV	ADC1_data0_p	ADC1_data0_n	GND_LV	ADC1_data1_p	ADC1_data1_n	GND_LV	ADC1_DCO_p	ADC1_DCO_n
		5	GND_LV	ADC1_data2_p	ADC1_data2_n	GND_LV	ADC1_data3_p	ADC1_data3_n	GND_LV	ADC1_FCO_p	ADC1_FCO_n
		6	GND_LV	ADC1_data4_p	ADC1_data4_n	GND_LV	ADC1_data5_p	ADC1_data5_n	GND_LV	LVDS_spare_0_p	LVDS_spare_0_n
		7	GND_LV	ADC1_data6_p	ADC1_data6_n	GND_LV	ADC1_data7_p	ADC1_data7_n	GND_LV	LVDS_spare_1_p	LVDS_spare_1_n
		8	GND_LV	ADC2_data0_p	ADC2_data0_n	GND_LV	ADC2_data1_p	ADC2_data1_n	GND_LV	LVDS_spare_2_p	LVDS_spare_2_n
		9	GND_LV	ADC2_data2_p	ADC2_data2_n	GND_LV	ADC2_data3_p	ADC2_data3_n	GND_LV	ADC2_FCO_p	ADC2_FCO_n
		10	GND_LV	ADC2_data4_p	ADC2_data4_n	GND_LV	ADC2_data5_p	ADC2_data5_n	GND_LV	ADC2_DCO_p	ADC2_DCO_n
	2	1	GND_LV	ADC2_data6_p	ADC2_data6_n	GND_LV	ADC2_data7_p	ADC2_data7_n	GND_LV	ADC3_DCO_p	ADC3_DCO_n
		2	GND_LV	ADC3_data0_p	ADC3_data0_n	GND_LV	ADC3_data1_p	ADC3_data1_n	GND_LV	ADC3_FCO_p	ADC3_FCO_n
		3	GND_LV	ADC3_data2_p	ADC3_data2_n	GND_LV	ADC3_data3_p	ADC3_data3_n	GND_LV	Fast_data0_quadrant_mod_p	Fast_data0_quadrant_mod_n
		4	GND_LV	ADC3_data4_p	ADC3_data4_n	GND_LV	ADC3_data5_p	ADC3_data5_n	GND_LV	Fast_data1_quadrant_mod_p	Fast_data1_quadrant_mod_n
		5	GND_LV	ADC3_data6_p	ADC3_data6_n	GND_LV	ADC3_data7_p	ADC3_data7_n	GND_LV	fast_clk_coded_p	fast_clk_coded_n
		6	GND_LV	ADC4_data0_p	ADC4_data0_n	GND_LV	ADC4_data1_p	ADC4_data1_n	GND_LV	fast_clk_system_p	fast_clk_system_n
		7	GND_LV	ADC4_data2_p	ADC4_data2_n	GND_LV	ADC4_data3_p	ADC4_data3_n	GND_LV	fast_clk_conv_bunch_p	fast_clk_conv_bunch_n
		8	GND_LV	ADC4_data4_p	ADC4_data4_n	GND_LV	ADC4_data5_p	ADC4_data5_n	GND_LV	ADC_conv_clk_p	ADC_conv_clk_n
		9	GND_LV	ADC4_data6_p	ADC4_data6_n	GND_LV	ADC4_data7_p	ADC4_data7_n	GND_LV	ADC4_FCO_p	ADC4_FCO_n
		10	GND_LV	ADC5_data0_p	ADC5_data0_n	GND_LV	ADC5_data1_p	ADC5_data1_n	GND_LV	ADC4_DCO_p	ADC4_DCO_n
	3	1	GND_LV	ADC5_data2_p	ADC5_data2_n	GND_LV	ADC5_data3_p	ADC5_data3_n	GND_LV	ADC5_DCO_p	ADC5_DCO_n
		2	GND_LV	ADC5_data4_p	ADC5_data4_n	GND_LV	ADC5_data5_p	ADC5_data5_n	GND_LV	ADC5_FCO_p	ADC5_FCO_n
		3	GND_LV	ADC5_data6_p	ADC5_data6_n	GND_LV	ADC5_data7_p	ADC5_data7_n	GND_LV	LVDS_spare_3_p	LVDS_spare_3_n
		4	GND_LV	ADC6_data0_p	ADC6_data0_n	GND_LV	ADC6_data1_p	ADC6_data1_n	GND_LV	LVDS_spare_4_p	LVDS_spare_4_n
		5	GND_LV	ADC6_data2_p	ADC6_data2_n	GND_LV	ADC6_data3_p	ADC6_data3_n	GND_LV	LVDS_spare_5_p	LVDS_spare_5_n
		6	GND_LV	ADC6_data4_p	ADC6_data4_n	GND_LV	ADC6_data5_p	ADC6_data5_n	GND_LV	ADC6_FCO_p	ADC6_FCO_n
		7	GND_LV	ADC6_data6_p	ADC6_data6_n	GND_LV	ADC6_data7_p	ADC6_data7_n	GND_LV	ADC6_DCO_p	ADC6_DCO_n
		8	GND_LV	ADC7_data0_p	ADC7_data0_n	GND_LV	ADC7_data1_p	ADC7_data1_n	GND_LV	ADC7_DCO_p	ADC7_DCO_n
		9	GND_LV	ADC7_data2_p	ADC7_data2_n	GND_LV	ADC7_data3_p	ADC7_data3_n	GND_LV	ADC7_DCO_p	ADC7_FCO_n
		10	GND_LV	ADC7_data4_p	ADC7_data4_n	GND_LV	ADC7_data5_p	ADC7_data5_n	GND_LV	ADC7_data6_p	ADC7_data6_n

LVDS_spare_5_p and ...._n might be used as FAST_data_clk_quadrant, but priority has: operation of ASIC/HDI from module.

	power+	power-	GND
ADC's	3.4A		3.4A
Fast-OP's	2.9A	2.9A	
Slow-control	1.0A		1.0A
Sum:	7.3A	2.9A	4.4A
contacts á 0.7A	12	6	8
shields as spare	6	5	9

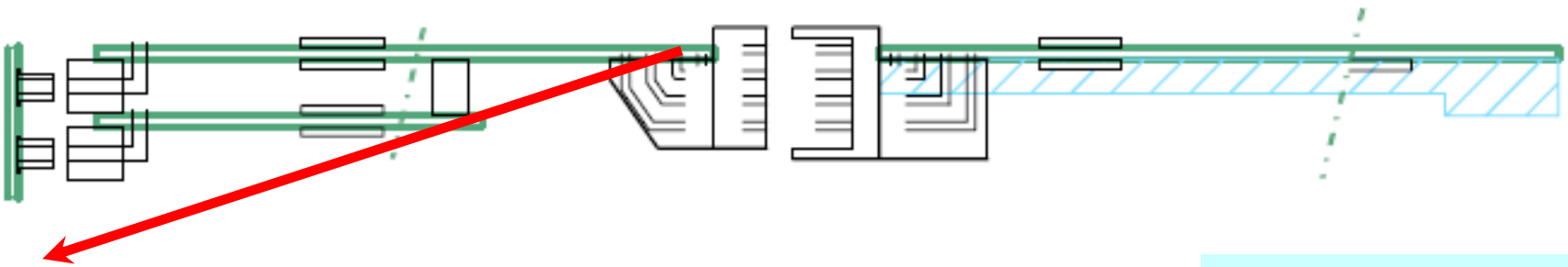
Differential pairs
In 3 layers reachable.

Single ended and

Power squeezed in: eazier mounting

Fan part of quadrant?
… or power needed here
WP: Mechanics

Module electronics: Connector dig. part

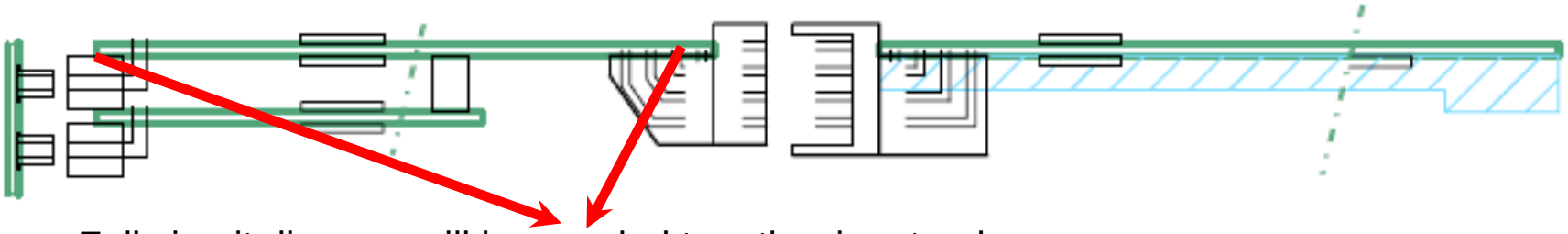


Differential pairs
In 3 layers reachable.

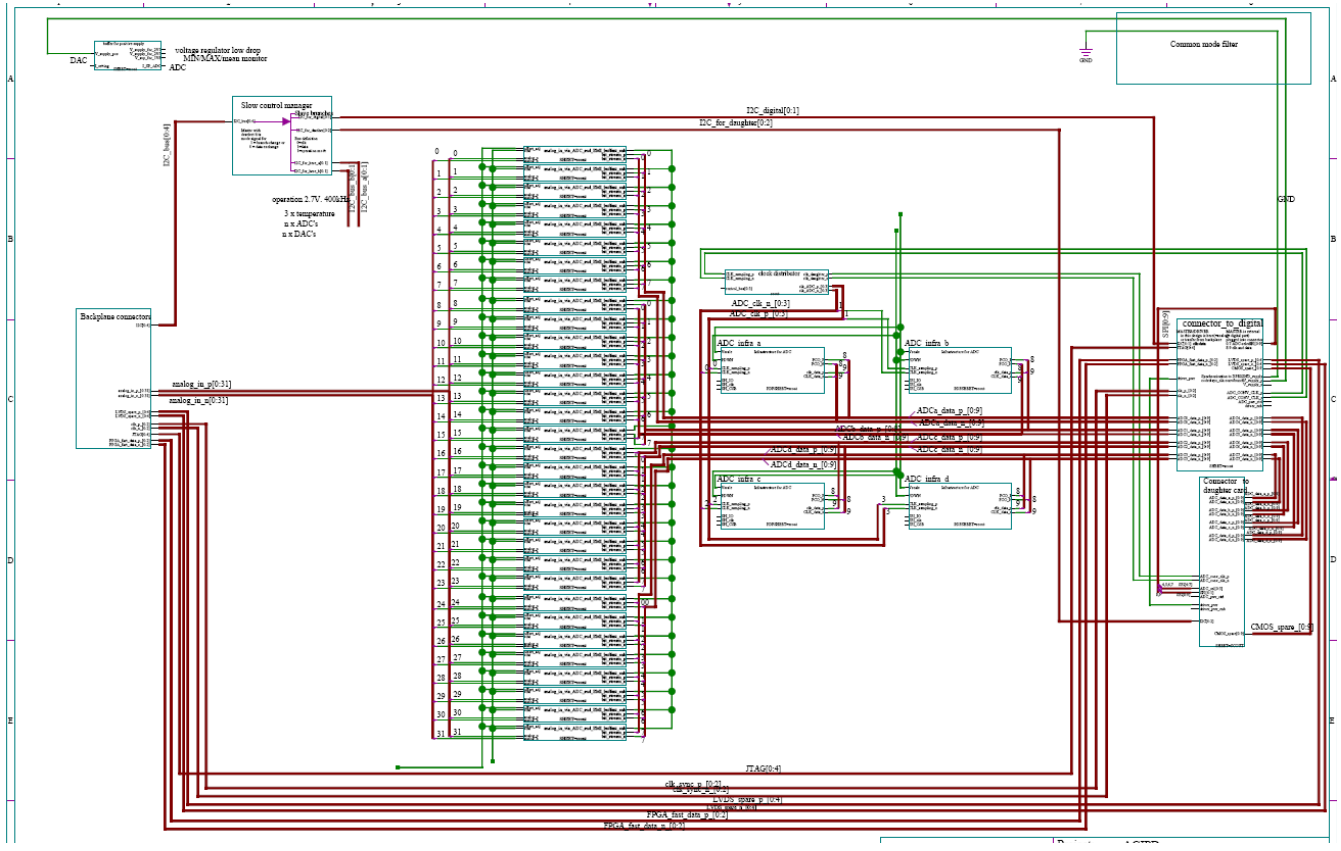
Power-EMI-performance

Easy-layers

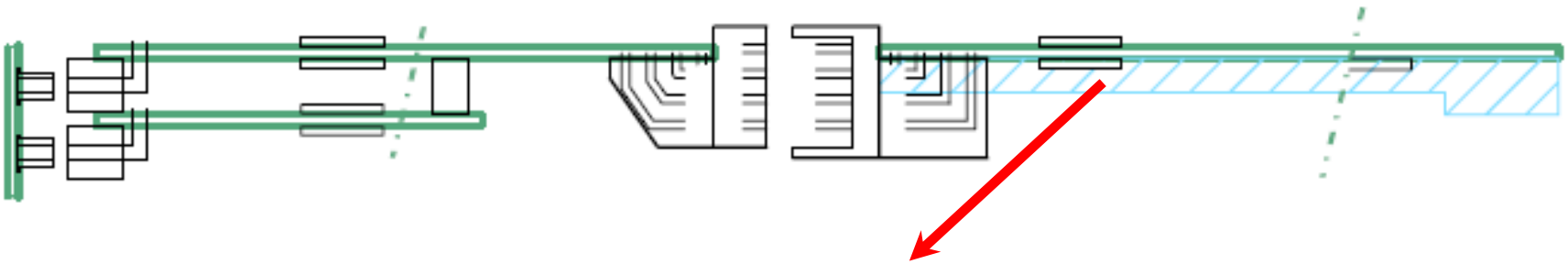
Module electronics: .. Getting analogue part together



Full circuit diagram will be puzzled together in a top-layer:
…. Not now, I add the status to the minutes
…. Still a few blocks missing or not filled.



Module electronics: Digital part



Not so many interference with the other work packages, …. Keep it short:

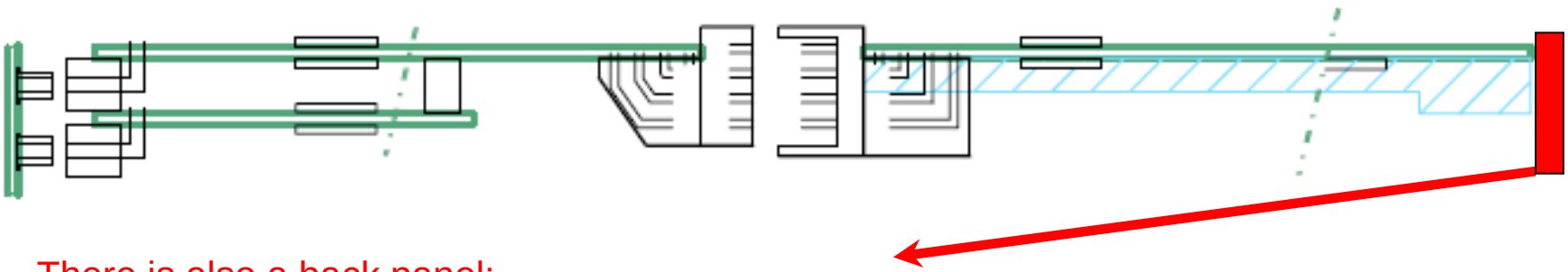
Doing the circuit diagram and layout, based on the studies of last year:

- writing 64 ADC's into memory
- First all amplitudes , afterwards all gains
- Parallel transfer of sorted data to 10GbE
- Controlling the ADC's
- Getting controlled from the quadrant: Firmware boot and parameter setting
- Getting monitored from the quadrant

- Passing power from backpanel to the analog part

- Another heat: 10-20W generated from +12V
  DC/DC converters with reasonable filtering,
  closed current loops (digital quality)

Module electronics: Digital part



There is also a back panel:

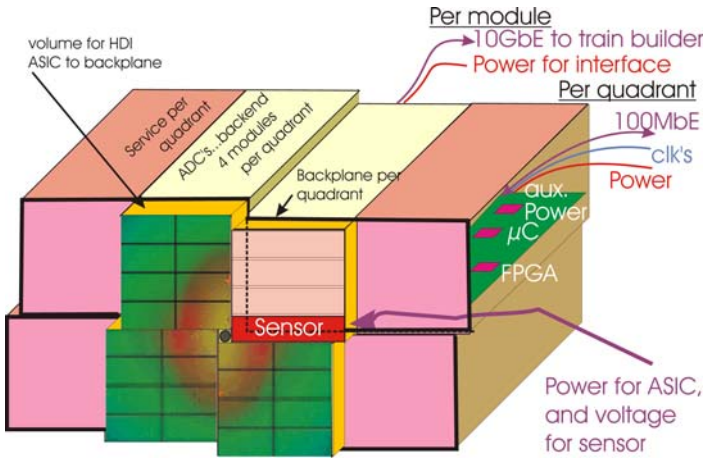
- Power for interface electronics (not HDI/ASIC)
  As $V_{positive}$ $V_{negative}$ and GND_{analog}
  To local GND at analog part
- Power for digital part as one voltage, $GND_{digital}$
  To local GND at digital part
- Fiber for 10GbE – UDP
- If space: expert connections
- air stream? …. Better from the side

One sub-D-combo

Typical:
Wires: 5m: 4mm² FRNC
Current: 6A

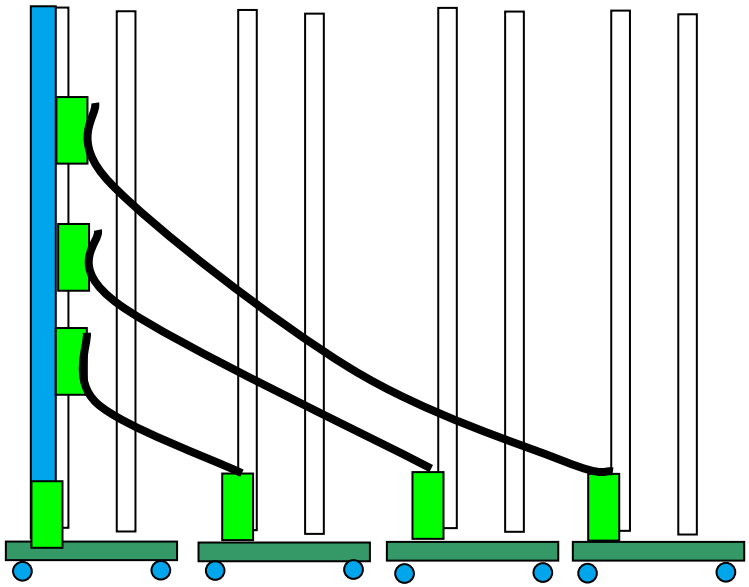
Voltage drop: 0.25V
OK.

Quadrant electronics: Backplanes



Mounting Modules in the new mechanical concept requires or eases the procedure with a backplane per module (two in a row for 4MPixel)

Then interconnect on the quadrant by flat-cable or Flex-rigid PCB's in the quadrant to a common FPGA-µC system.



Power for HDI?
- monitored there?
- at some time need more information, at the moment more priority for the module boards

Fans?

Work for µC, I put into Tomorrows talk

Getting to “16x16” system: Fast, “no definitions”

Text boxes from a year ago
There is was commented,
“ will be done by the ASIC-
test boards from the ASIC
developing groups”

We have

- 10Gbit development
- ADC evaluation

In production

- Interface ADC-evaluation to 10Gbit-development

…….. **That is the basics as specialties**

But no common program

But not:

- analogue signal filter:… Need specifications

  not in beginning?, experience
- pattern generator……. **Buy for PXI** (control system)

  or VHDL on evaluation
- I2C..... No definitions

16 x 16 tests: Interface electronics , Who?

We have, that evaluation boards : ADC, FPGA and our 10GbE
We have the circuit diagram for the final analogue chain.

We do not have the description of the connector to the HDI
We do not have a description for the pattern/sequences to go to the ASIC/HDI
We do not have a description of values delivered back

Who does the board?
When are description available?
Who talks the next time about that item?

Progress only with detailed informations.

Summary

- Module electronics:
  For the final system circuit diagrams and steps towards PCB's are progrssing.
  A bit behind the plans.

- Backplanes: Open the connectivity to the HDI with hardware and connectivity definitions.

- Quadrant: (Tomorrow) : μC basic studies are started.
  new mechanical idea following the changes of front module installation.

- 16 x 16 : Confusion, missing information, urgent