WP 2.5 Control System
but also touched issues in WP2.4

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- XFEL common organization
- issues for fast clocks/signals
- interface electronics internal control
- fast veto possibilities
- slow control

XFEL common organization

- common development for the fast clocks/signals by British consortia: working prototype end 2010

- development for a slow control system on the example of AGIPD at DESY
  In Detector head (quadrant): ARM9/LINUX
  External system : PC and network
  may be example for the others

Organization:

C&C: UniversityCollegeLondon(implementation)
WP76(coordination) Chris Youngman
Common specification,usage,… : AGIPD, LPD,DSSC

SC: PC-µC WP76: New: Dana Wilson
AGIPD: New: Lothar Steffen(DESY-FEB)

HV-device programming testsWP76: S.Esanov

issues for fast clocks/signals

- From XFEL via experimental Clock&Control:

  - get pre-warning (~10ms) of train start

  - get the bunch clock: (<=5MHz) w/o phase jumps

  - getting a continuous running clock
    just below 100MHz (our ADC's!)
    phase stable multiple of bunch clock
    New: Agreed from XFEL-acc.: no phase jumps on bunch-clk.
    that avoids complexity or PLL's , state machines

- At experimental area generated: Fast reject
  Timing/delay issues was discussion on last meeting

-No specifications: needs of ASIC, yesterdays discussion

-Next train builder and Clock&Control Meeting Oct 22nd

fast clocks/signals….. cont.

Consequences for ADC-clock (and bunch CLK of ASIC?):

Resources: System(100MHz)/bunch clocks: continuous:

Goal: To keep the storage time easy defined,

- State machine from begin-train to end-digitize in the FPGA of the quadrant.
- Minimize storage time for used ASIC-capacitors? or fixed time for each ASIC-capacitor? defines VHDL-code and fast signals to ASIC.

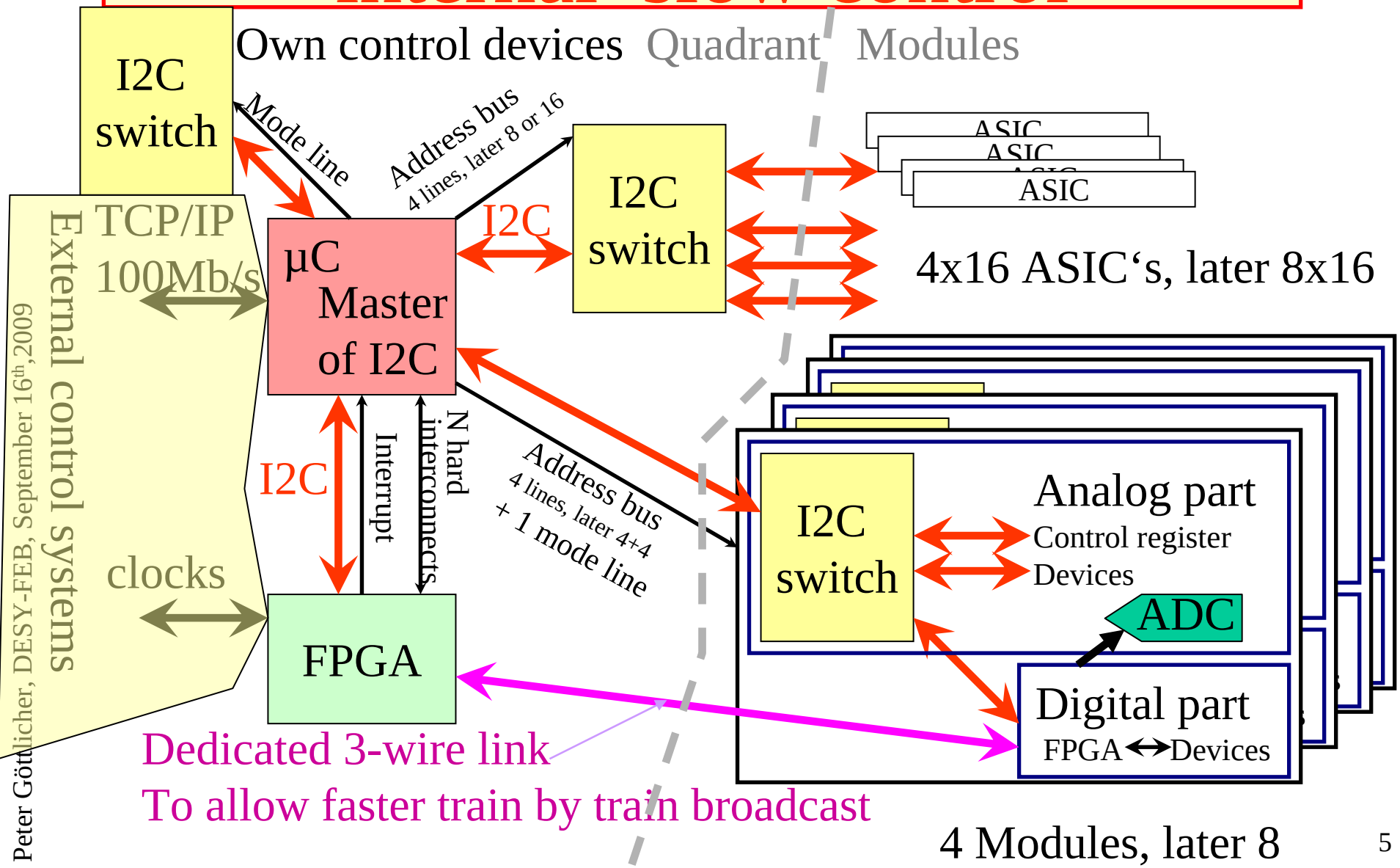
ADC-Clock frequency: How granularity to set?

- Easy clocks: 100MS/s / (2*n): 50, 25. (50% duty -cycle)
- With additional PLL's also 100MS/s * m/(2*n) :

m=1,2 or 3 should be sufficient …. My proposal

Alternative: multiples of the 5MHz-bunch-clock, but that changes more likely with other beamline.

interface electronics
internal slow control



fast veto possibilities

Last XDAC: Can we handle later VETO's?

What can the interface electronics do to support the ASIC:

Major task has to be in the ASIC

BASIC CONCEPTS:

- Veto can be delayed to a fixed bunch number of 200ns.

  ASIC has to organize handling of used cells

  but no additional fast LVDS signals in

  backplane and HDI

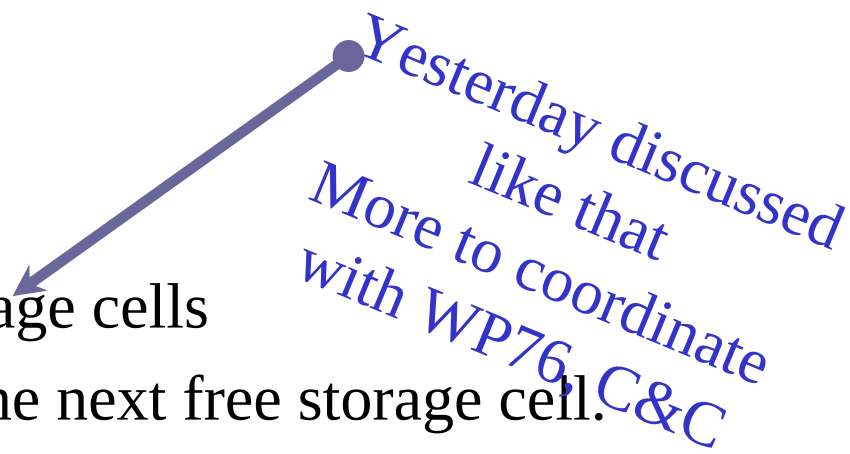
OR

- The quadrant FPGA can do

  the bookkeeping of used storage cells

  and distribute within 200ns the next free storage cell.

  few LVDS line to ASIC's

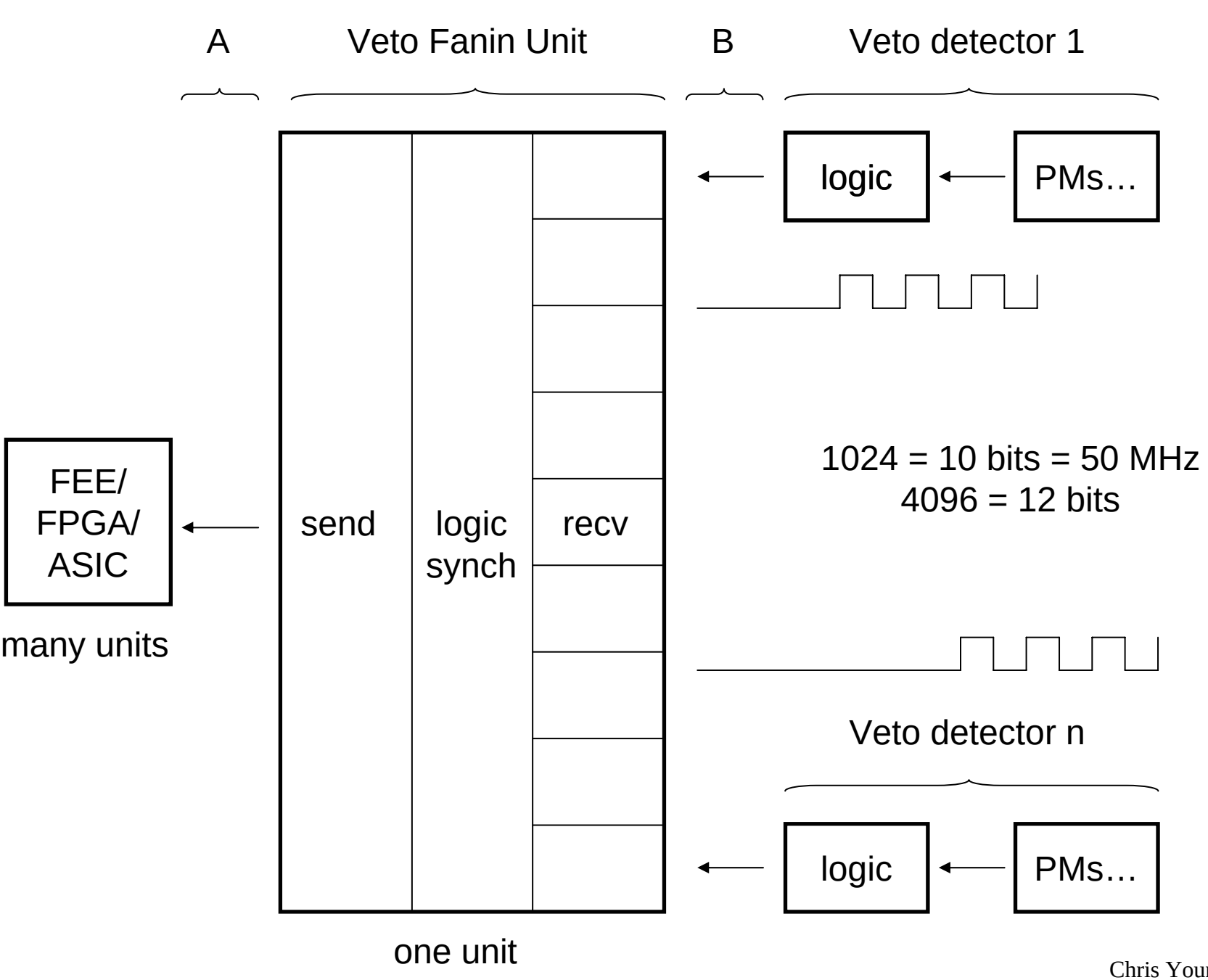


fast veto possibilities… cont.

The next free cell number can be distributed
within 200ns (<= 10bits)

- by few LVDS line 50Mbit/s, needs termination
  digital activity in HDI/ASIC while sampling
- multiple line (4 pairs) without termination.
- technology would depend on HDI signal handling

- To be optimized, may be none optimal usage at train-end
  At end of train might be a period,
  in which all cells are used, but then a cell gets free again!
- Same LDVS lines used for control from quadrant-FPGA to ASIC
- Transfer after train-end from quadrant-FPGA to FPGA in module
  400 picture* 12bit for bunch ID = 4800 bits in 100ms


A
Veto Fanin Unit
B
Veto detector 1
logic
PMs…
FEE/
FPGA/
ASIC
send
logic
synch
recv
1024 = 10 bits = 50 MHz
4096 = 12 bits
many units
Veto detector n
logic
PMs…
one unit

Slow control

Monitoring data: How many, what?

That are questions I get NOW asked by WP76.

Booting:

- Major part needed to boot the ASIC's

  Few bytes per pixel ? Mbytes ?

- Interface electronics:

Power settings :	few bits / module
TCP/IP addresses for output links:	few bytes
Boot parameter of pattern generator:	few (100) byte
bunch patterns	few kBytes

Slow control…. continue

Monitoring:

- ASIC's?

- interface electronics:

Train by train: Busy, ready error state

Data transfer performance (if feedback) few bytes

Slow: currents, voltages, temperatures few 10sensors/module

control link performance bytes/quadrant.

Summary/Outlook

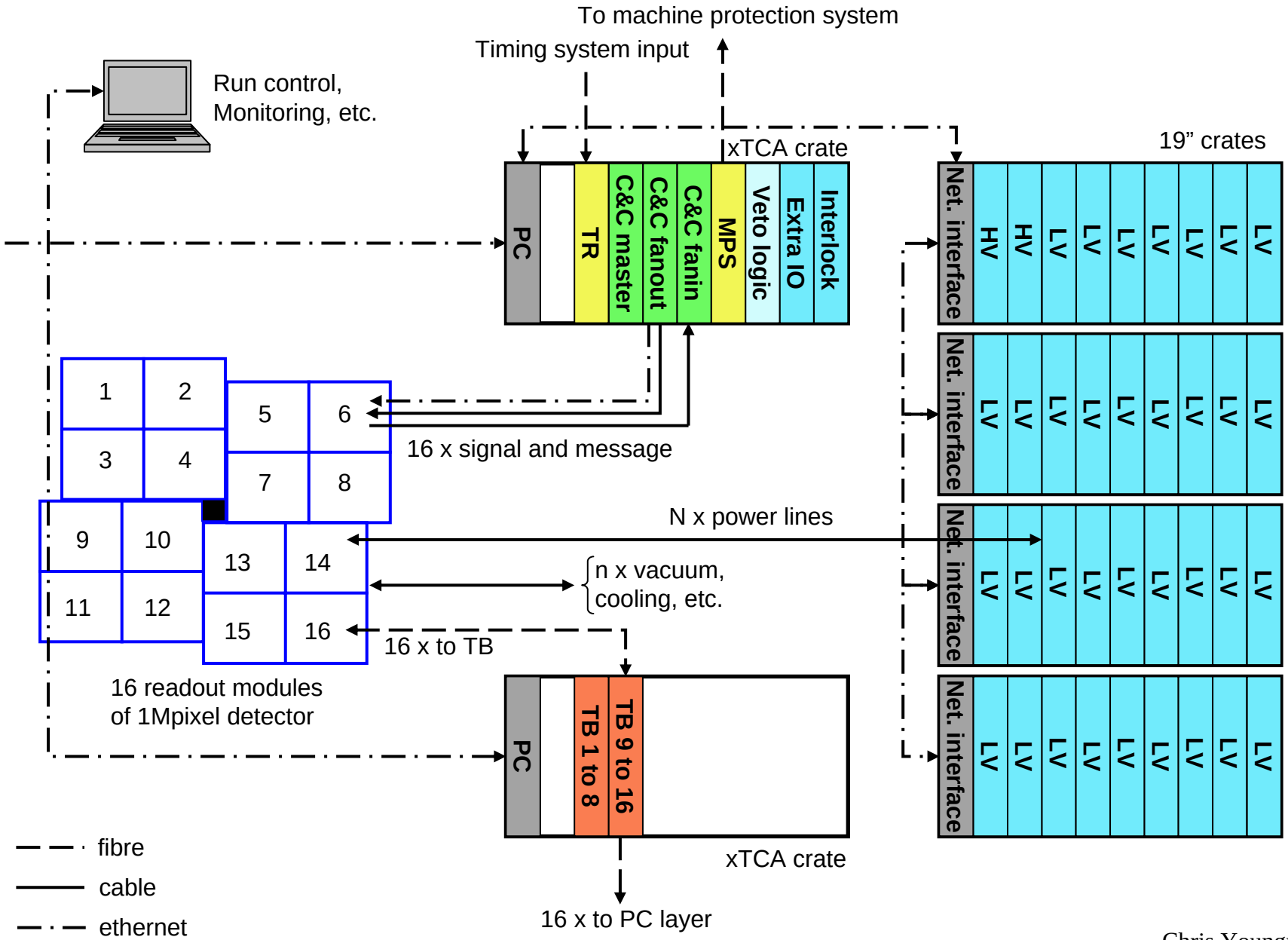
Common WP76 gets active:

- continuous clock, allows continuous operation of state machines.
- also force to us, to specify data volumes and meanings.

My statement, also in proposal:

“Definitions develops with progress in the developments.”

Estimations of data volumes from interface possible,
but not always the majority. ASIC?


To machine protection system
Timing system input
Run control,
Monitoring, etc.
xTCA crate
19” crates
PC
TR
C&C master
C&C fanout
C&C fanin
MPS
Veto logic
Extra IO
Interlock
Net. interface
HV
LV
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
16 x signal and message
N x power lines
n x vacuum,
cooling, etc.
16 x to TB
16 readout modules
of 1Mpixel detector
TB 1 to 8
TB 9 to 16
xTCA crate
16 x to PC layer
fibre
cable
ethernet