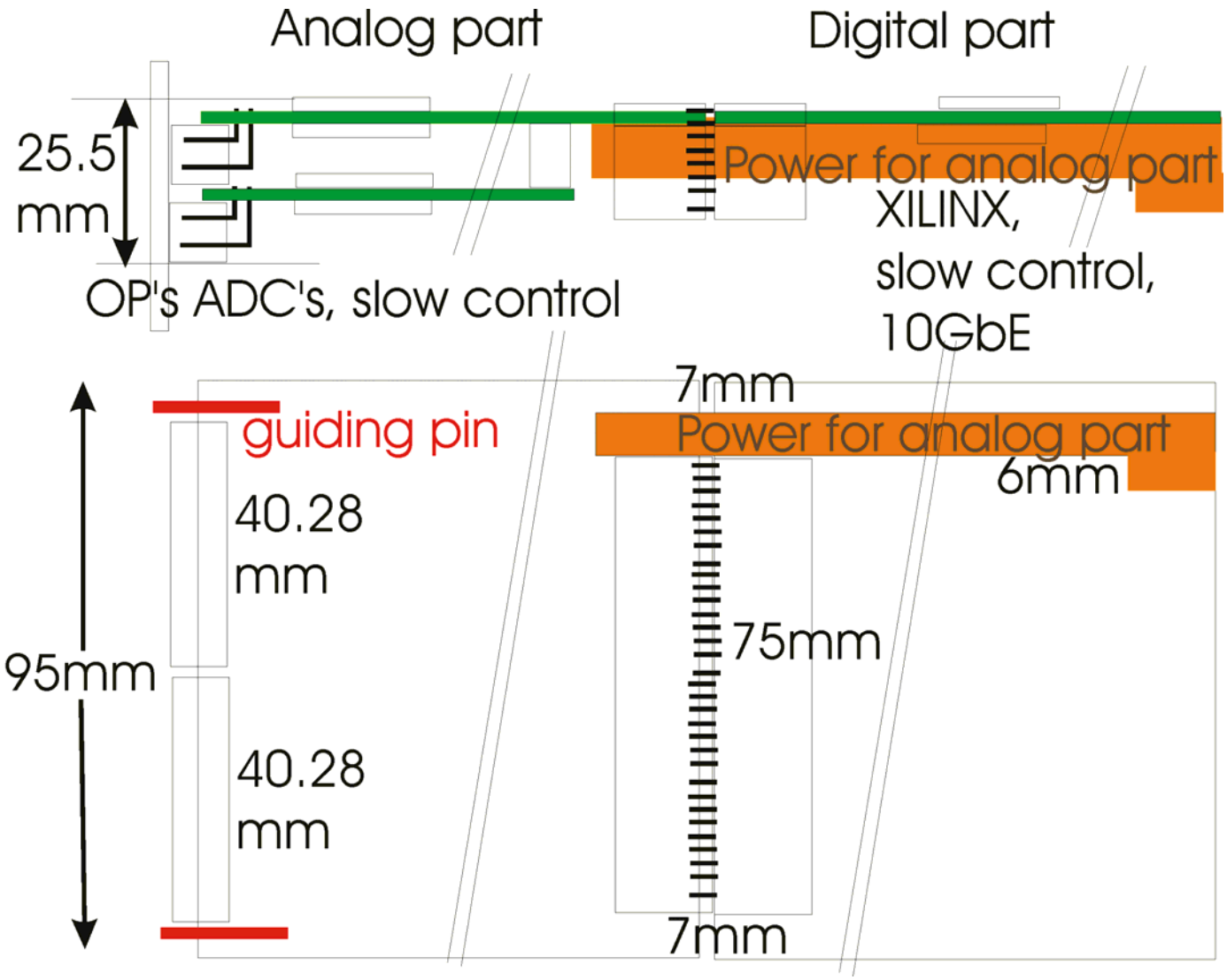
WP 2.4 Interface electronics

Peter Göttlicher, DESY-FEB, September 16th , 2009

- module concept
- technical challenges
- mechanical dimensions
- fully open: specifications for the ASIC's

--- slow/fast control in quadrant
see tomorrow

Module concept



Technical challenges

See talk from Igor Sheviakov

- ADC‘s : 50MS/s, >10 bits above noise OK.

- High data transfer 700Mbits/s through connections OK.

- Access to memory for 50MS/s and 10GbE,
  concept last meeting OK.

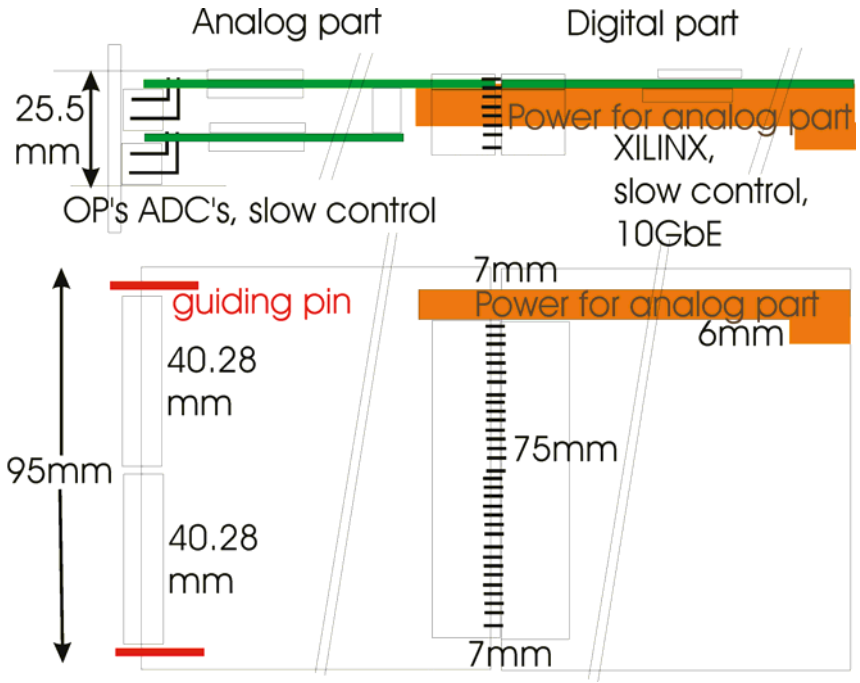
- Own test board with 10GbE OK.

-Connector densities see next slides: concept OK??

ONLY, if ASIC: gain-bits on analogue lines
needs two analogue boards,
gives also more compact detector head.

Discussed today with ASIC

Mechanical dimensions: width to be fixed



Module width of 95mm would allow

- For 2mm of rails each side, 91 mm for components.
- If needed, forced air stream, one side in, other out.
- Some freedom for for mechanical design
- Some shifts of electronics against sensors: More distance to beam.

Connections to quadrant-backplane

Signal count

200 64 analog from ASIC in pattern GND-sig-$\overline{\text{sig}}$-GND

9 3 Fast clocks from quadrant - in GND-sig-$\overline{\text{sig}}$-GND

- system-clk(<~100MHz)
- convert-clk(50MHz), bunch-clk
- coded length for train-start/end for convert-start/-end/pixel-incr.

Slow control:

3 module/extension/mode micro-controller

2 slow control for analog part (I^2C) from µC

3 slow control for digital part (I^2C-like) from FPGA

5 Reserve for remote firmware management

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222 pins: Fits to 4x SAMTEC TML-132-02-S-D-RA-10 = 256

Connections from analog to digital

Signal counts as pairs (" /2" = single line of pair)

80 from ADC's: 700Mbits/s

3 Fast clocks from quadrant

- system-clk(<~100MHz)
- convert-clk, bunch-clk
- coded length for train-start/end for convert_start/end/pixel-incr.

2 power for digital driver

1 ADC-clock from digital to analog

Slow control:

1/2 module select (FPGA-Q)

8/2 ADC-chip-select from FPGA to analog part

3/2 ADC slow control+power-down

3/2 slow control for digital part (I^2C like) from FPGA-Q

2/2 slow control for digital part (I^2C like) from µC

5/2 reserve for remote firmware management

97 pairs: Fits to 3x ERNI: ERmet ZD (female 973032, male 973101) =120

Specification coming from ASIC

?

Discussions ongoing
today and tomorrow

If not settled, the concurrent engineering will fail!
But: That is basics of time schedule!

Risk of developing wrong boards!
too high or too low complexity!

Examples:
Gain bits on analog: strongly defines the whole concept of mechanics and electronics
Speed of analog and gain-bits: defines circuits and space

Slow control :

Not covered today:

- slow control, is in close contact with central Work packages.

- It will tell also AGIPD control inside detector head in talk about WP2.5: control system