AGIPD Interface Electronic Prototyping

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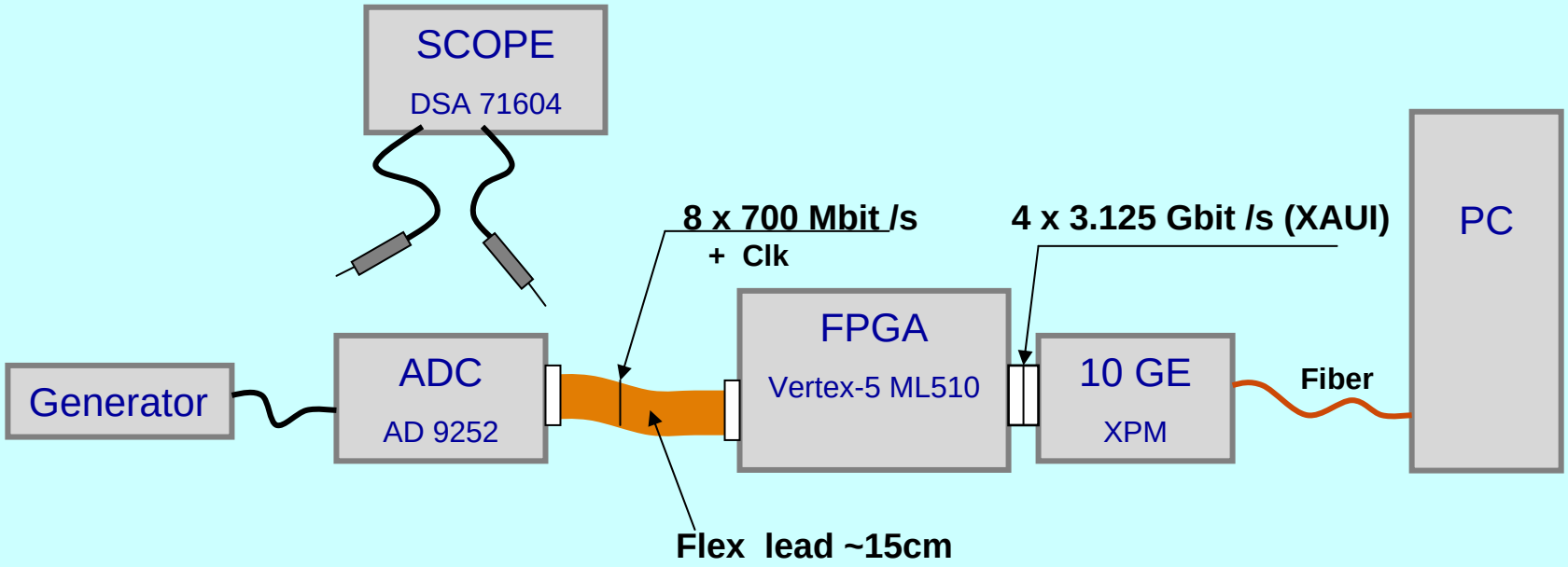
- **Hardware Setup, Measurements**
- **ADC (AD9252** 14bit x 8ch x 50msps **) readout**
- **Custom 10G Ethernet performance**
- **Conclusions**

HELMHOLTZ GEMEINSCHAFT

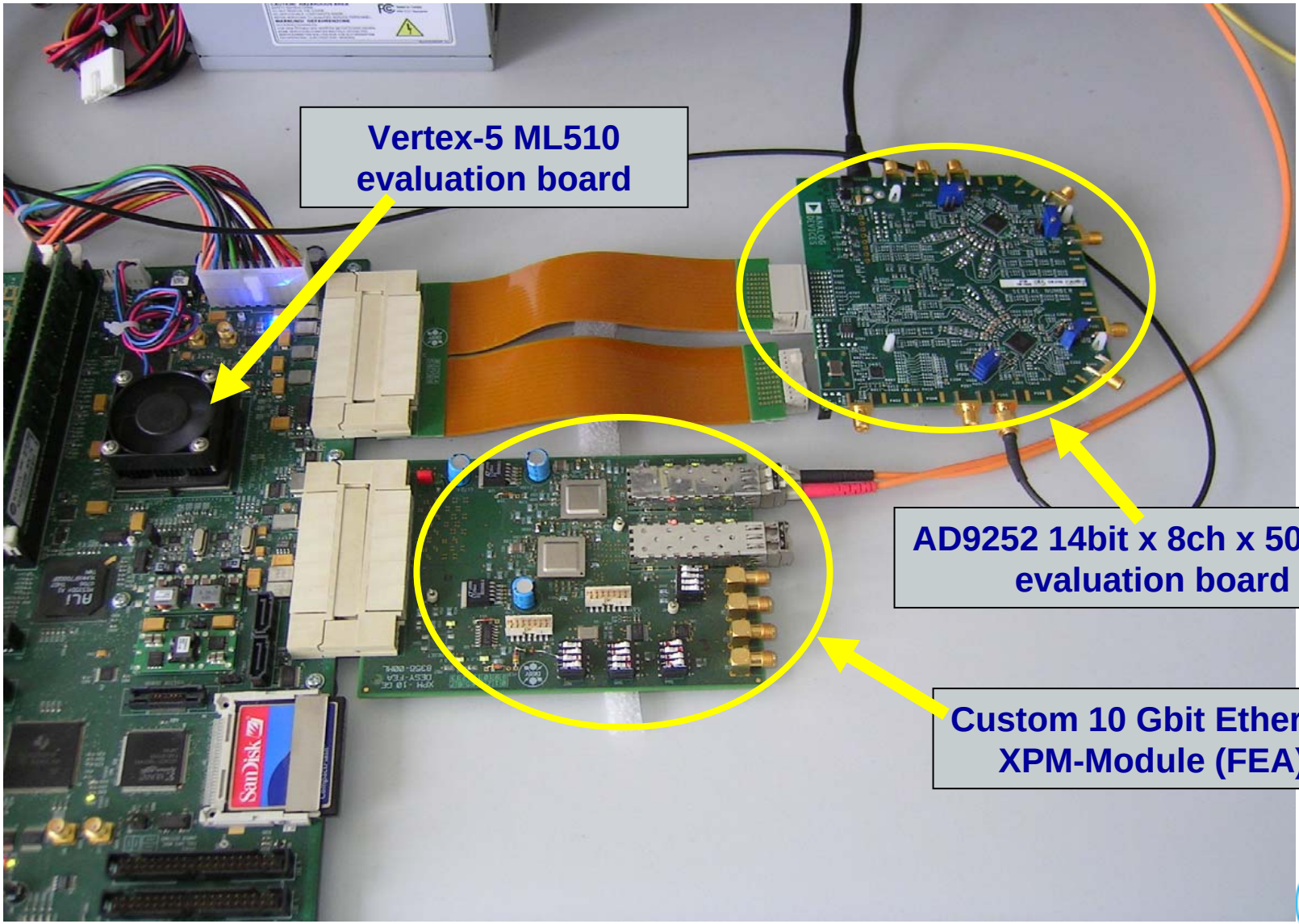
DESY

Test Bench Setup

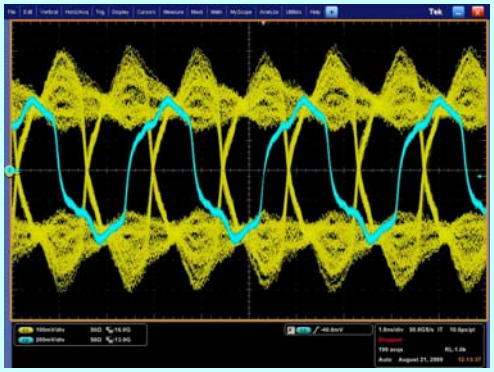


ADC - AD9252 14bit x 8ch x 50msps evaluation board
FPGA - Vertex-5 ML510 evaluation board with XPM connectors
10 GE - Custom 10 Gbit Ethernet XPM-Module developed by FEA **(DESY)**
PC - LINUX-PC (Dual Xeon with 4-core CPU and 10G Ethernet Card
SCOPE – DSA 71604 Digital Serial Analyzer, 16 GHz, 50 GS /s

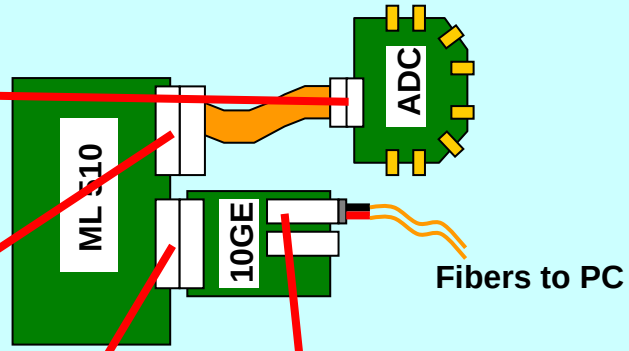
Test Bench Photo



Digital signaling quality in ADC -> FPGA ->10 GE chain



700 Mbit/s (ADC)
Clock + **Data**

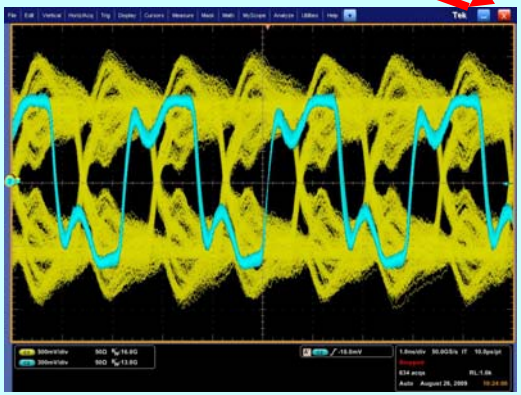


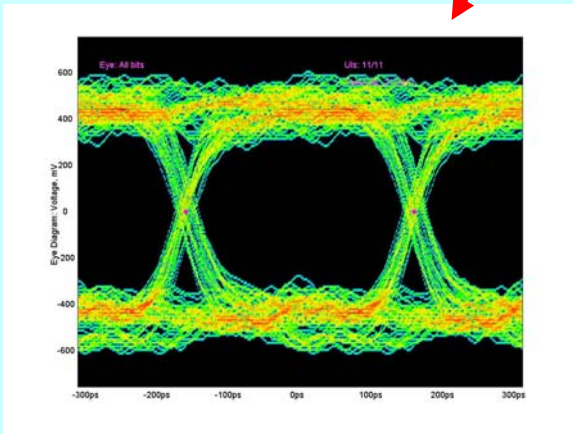
The not optimized chain of ADC board - flex lead -FPGA board without 100 Ohm shows still open eye diagrams.

Concept of separated analogue and digital boards with connector will be O.K.

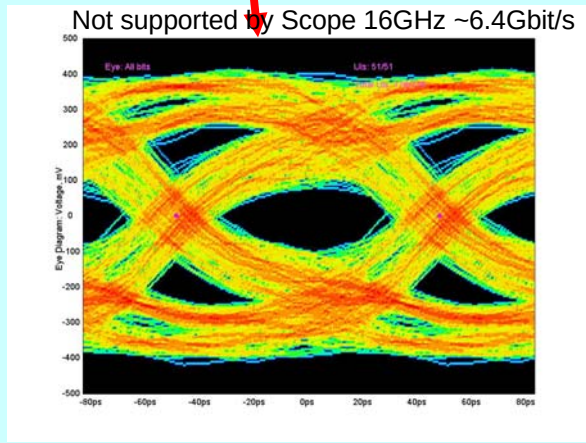
3.125 Gbit/s (XAUI)

10 Gbit/s (XFI)

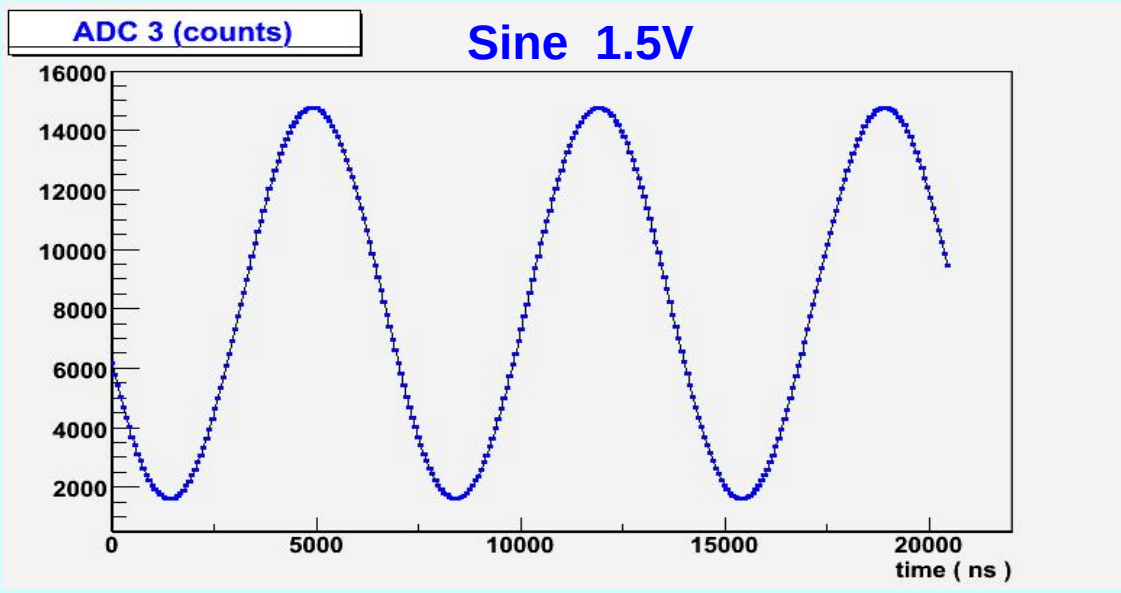


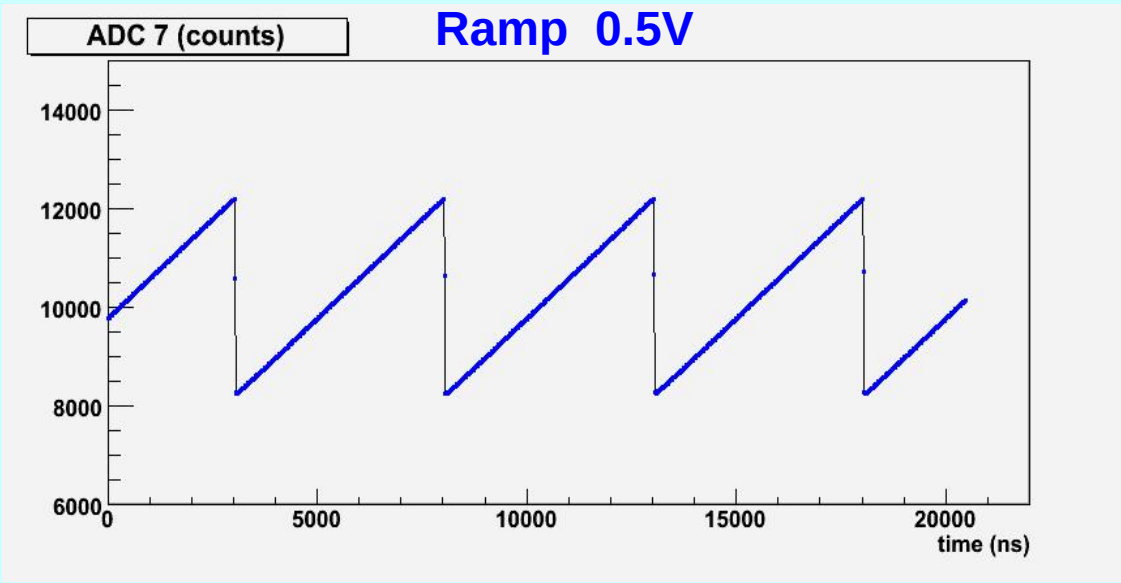


Not supported by Scope 16GHz ~6.4Gbit/s

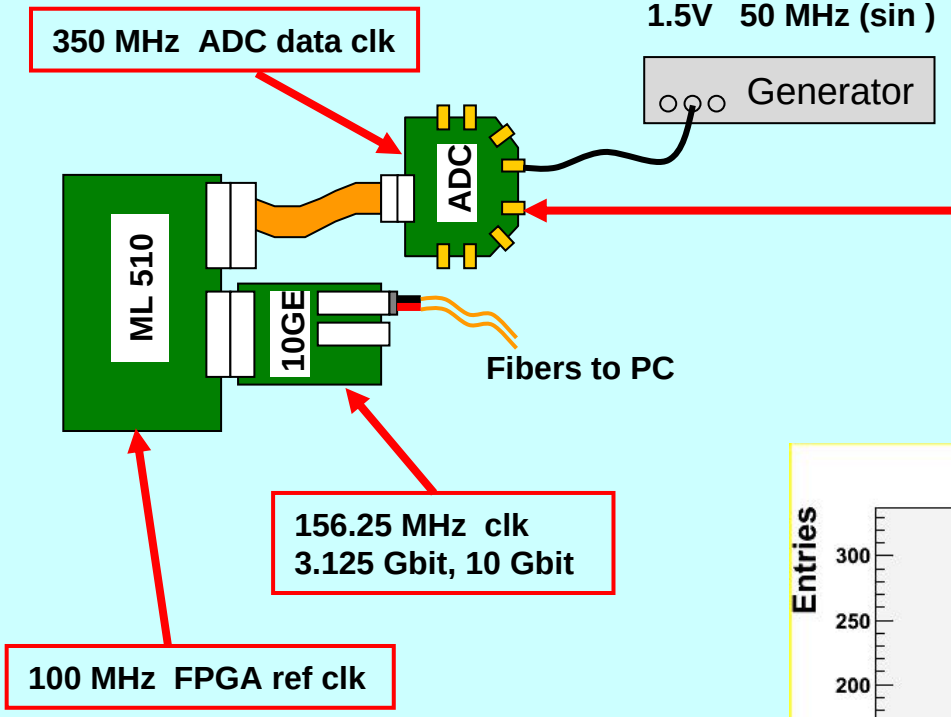


ADC Read-Out tests (through whole chain ADC -> FPGA -> 10GE -> PC)





Noise / Crosstalk Measurements

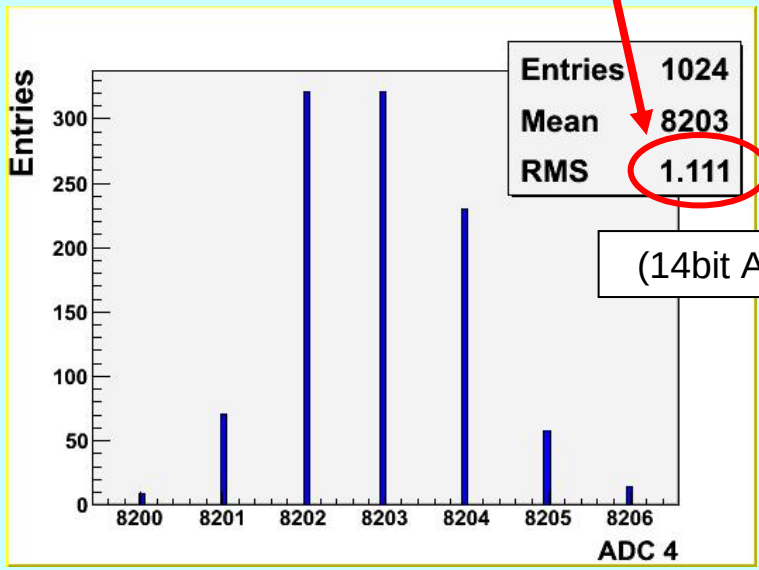


Noise spectrum from an ADC channel with open Input.

Conditions: 1.5V 50 MHz (sin) on the neighbor channel asynchronous with ADC clk ,

10GE stuff : 156.25 MHz mgt ref clk, 3.125 Gbit, 10 Gbit, 100 MHz FPGA ref clk, 250 MHz DDR2

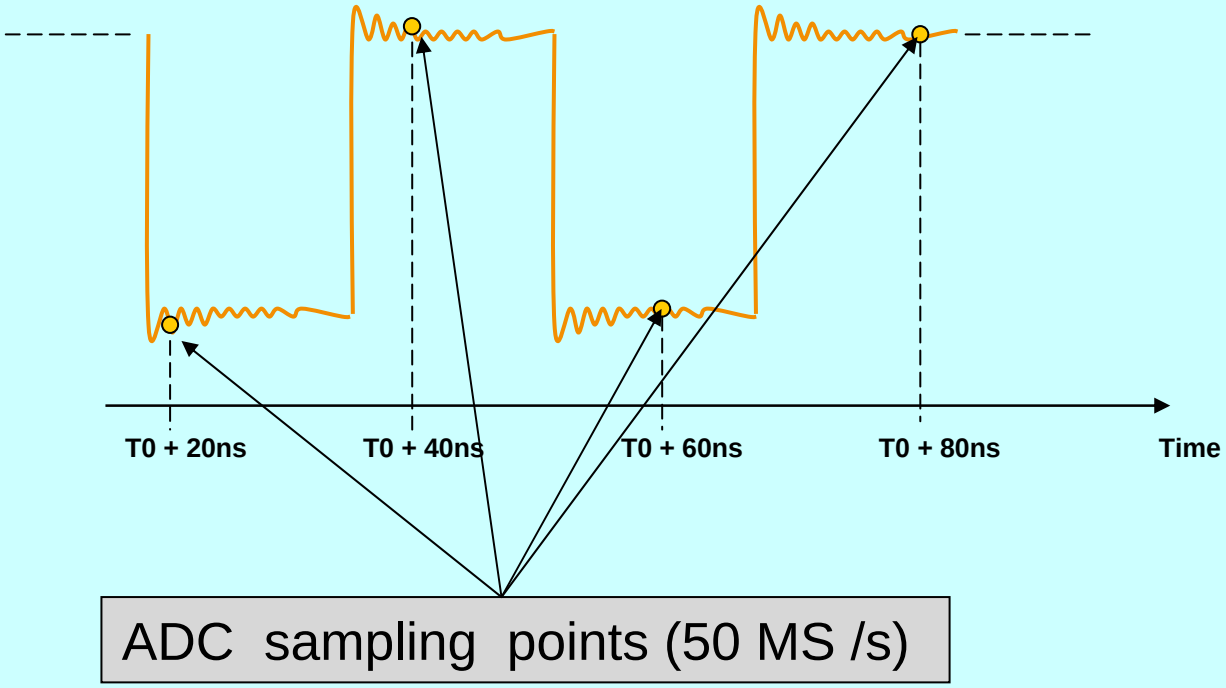
All clocks are asynchronous with ADC



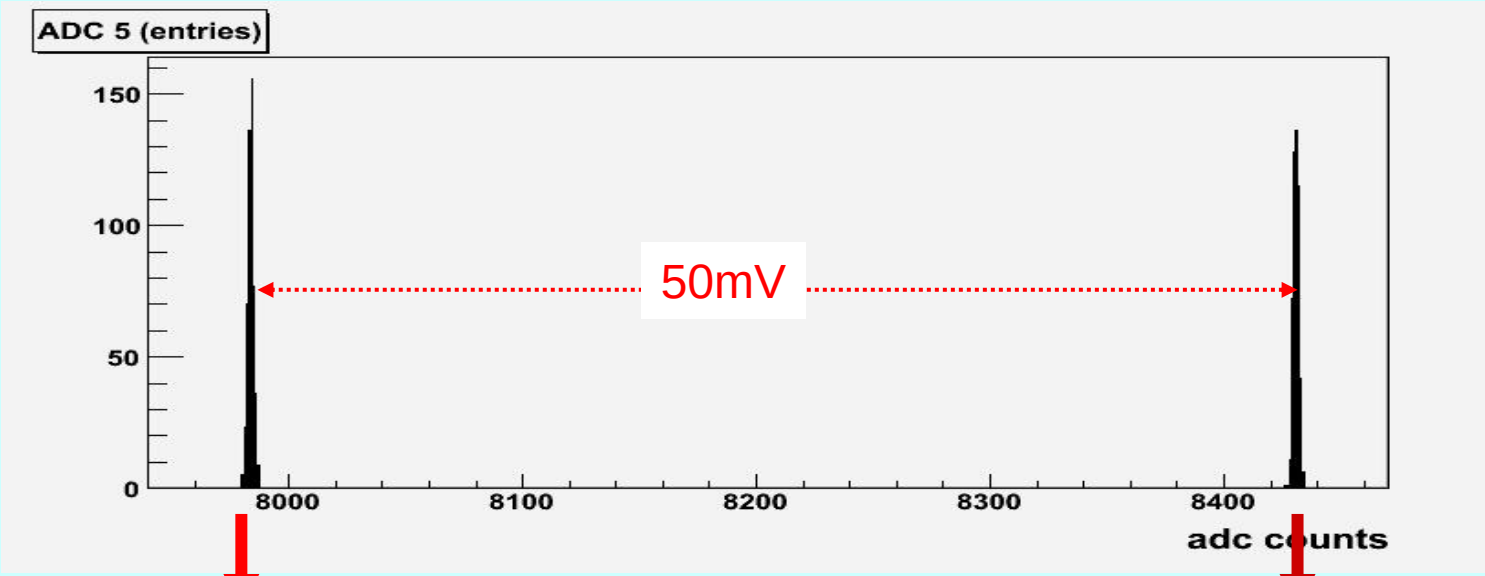
(14bit ADC)

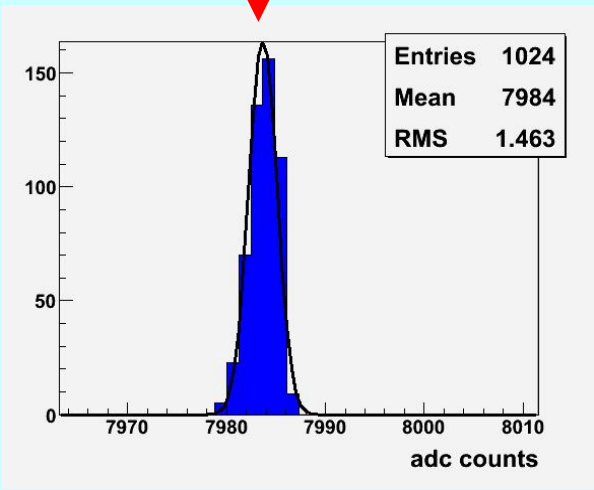
Front End Signal: Step function response

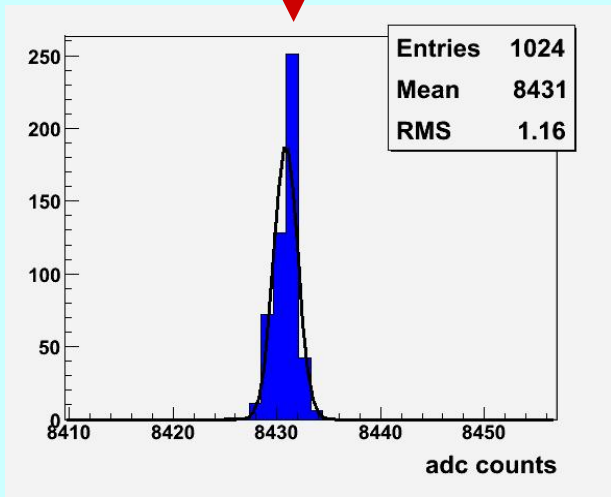
ADC Input: 25 MHz Square, asynchronous with adc_clk



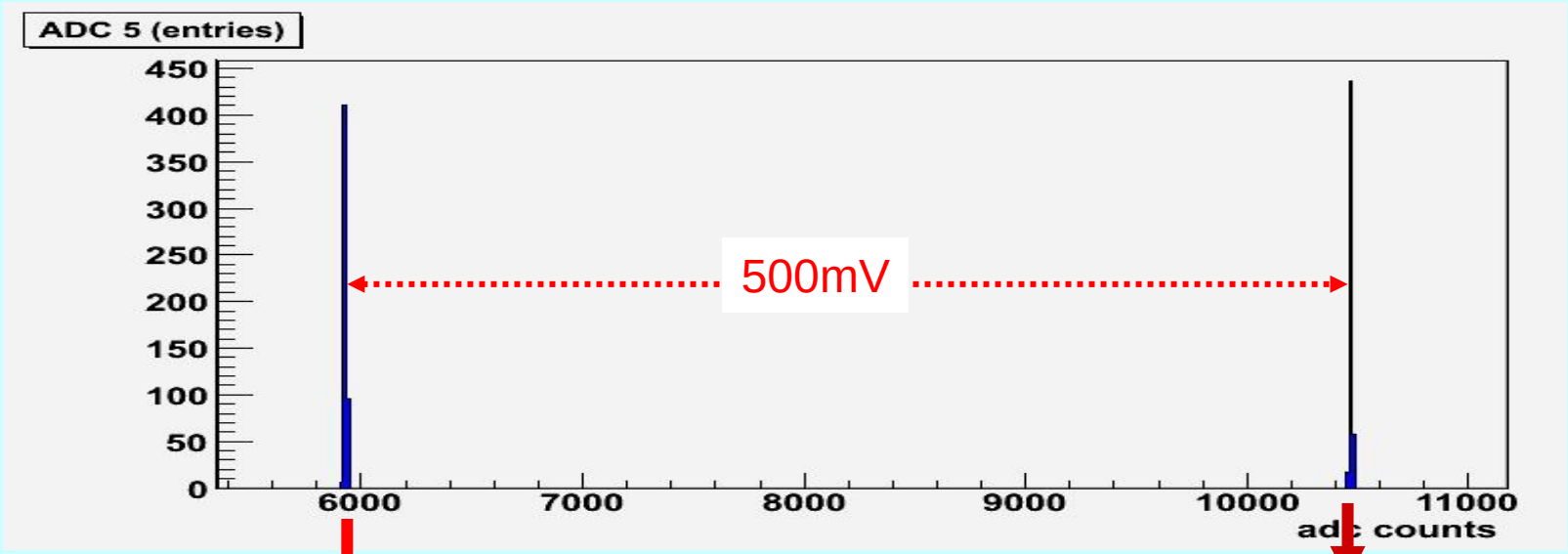
Front End Signal: Step function response

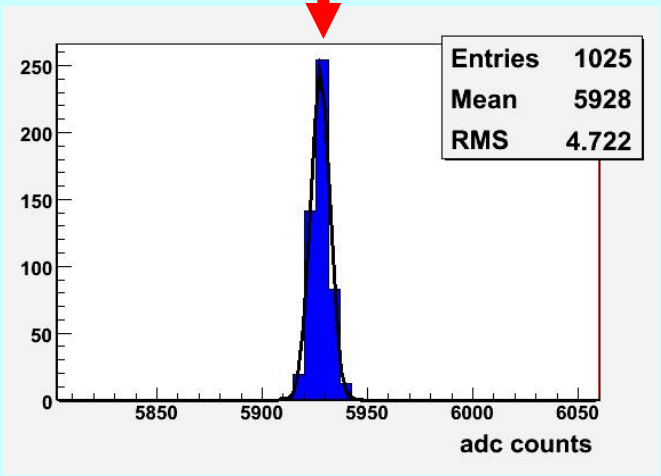


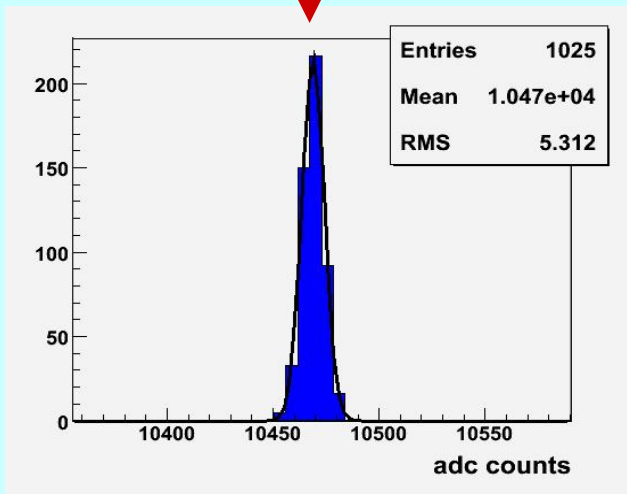




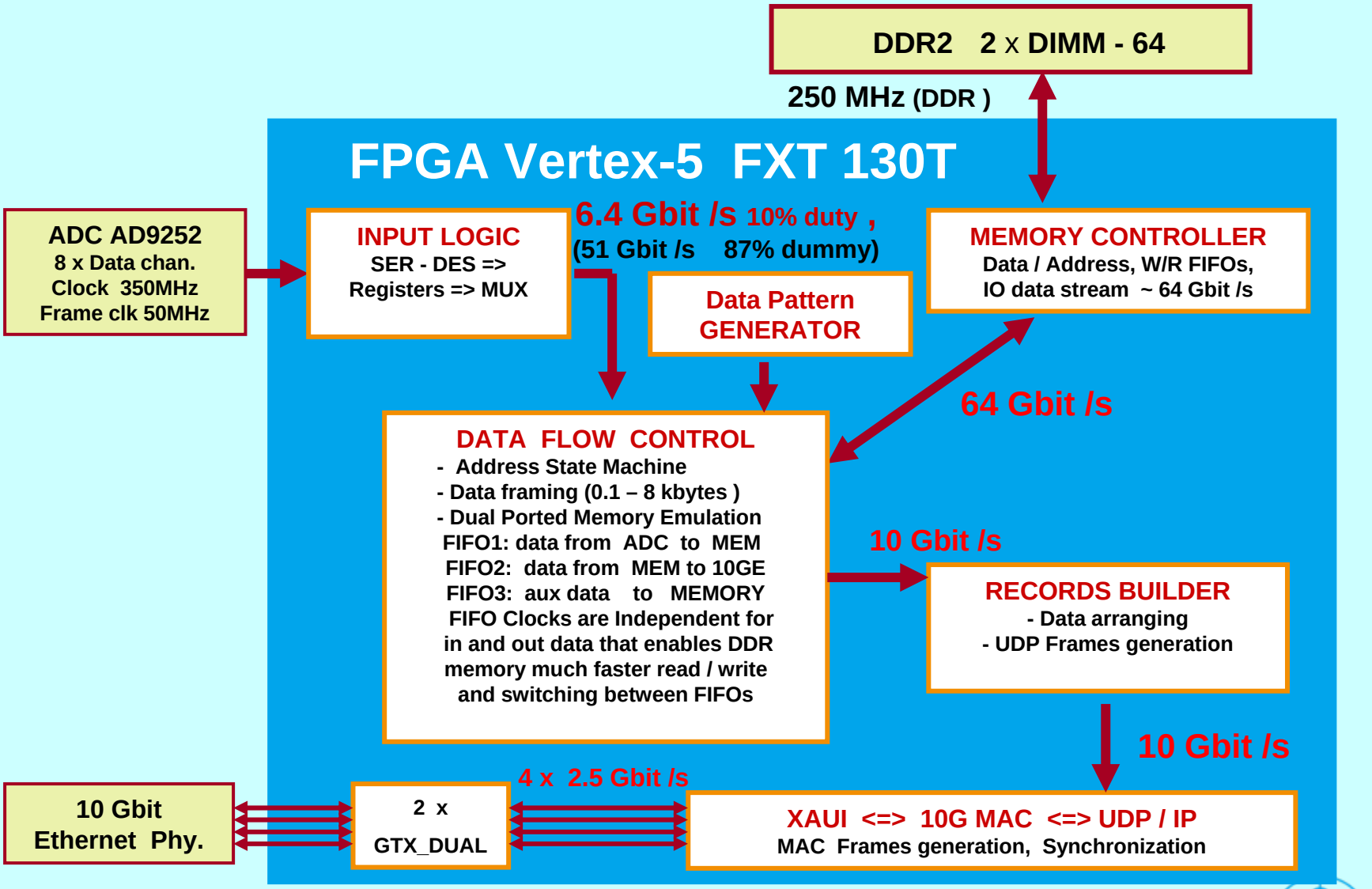
Front End Signal: Step function response







Block Diagram of FPGA (ML510) Program



10 Gigabit Performance Tests : Standalone and with Linux PC

Standalone Loop:

ML510 => 10-GE XPM => SFP+ => Optic => SFP+ => 10-GE XPM => ML510

10 GE Link with Linux PC:

Full duplex (The IEEE 802.3 protocol)

PC <=> Optic <=> SFP+ <=> 10-GE XPM <=> ML510

Tools / Methods

Transmit Engine: wire-speed MAC frame generation with **IPv4, UDP** and selectable data pattern, **ARP** sequence.
Receive Engine: Valid Frame Filter, CRC Error and Pattern Sequence Check

Data flow control - via varying pause fraction (pause length / frame length) for throughput measurements

LINUX-PC: Standard network tools: ethtool, ifconfig, arping, JAVA application, …

10GE XPM Performance Table

Test setup / Measurement	Stand alone data transmission via optical loop	Communication with PC equipped by 10G Ethernet card, UDP IP packets
Data Throughput	98 - 99% is reached	70% (7.1 Gbit/sec) without UDP frame loss
Varied frames, gaps, patterns with full data throughput	Bit / Frame Error < 1.0E-15	BFE < 1.0E-15 (below 7.0 Gbit/sec)
Temperature impact for measured range 20 - 70 C	BFE < 1.0E-15 for all transmission conditions	
Layout impact with two differently routed 10-GE channels	BFE < 1.0E-15 for both channels	

Conclusions

- It was designed and tested fully functional signal chain containing all critical items.

- Performance is acceptable for AGIPD project digital and analog parameters.

- This design and experience is supposed to be used for building the final Interface Electronics .