First Results from the HPAD 0.1 Chip

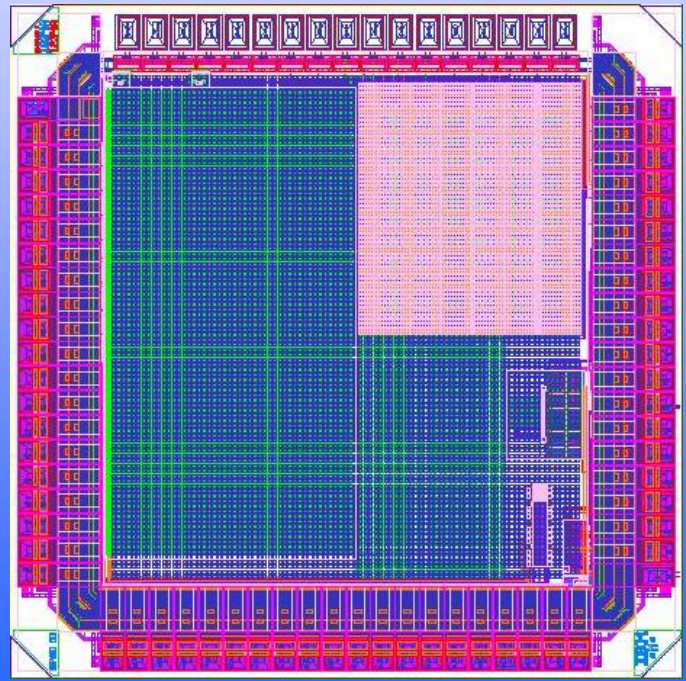
U. Trunk
DESY

The "hpad 0.1" chip

- 2mm x 2mm, submitted via MOSIS at 26.03.2008
- Only test structures:
  - Capacitors
  - Switches (FETs)
  - 16-cell analogue storage array
  - OP-Amp & buffer amplifiers
  - Minimum protection pad

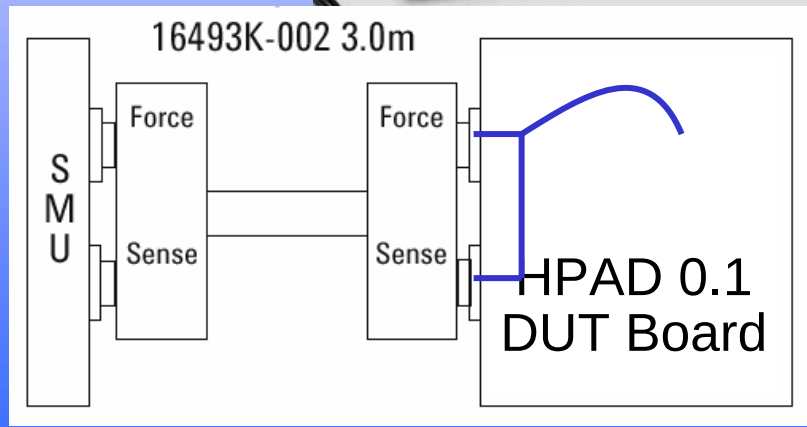
All results are…

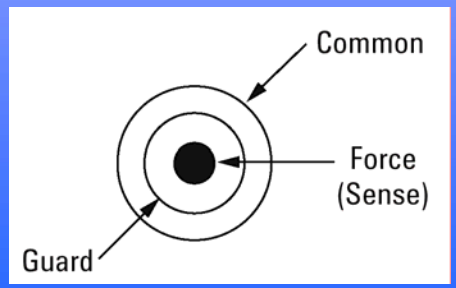
- preliminary!
- per device (unless denoted else)



Measurement Setup

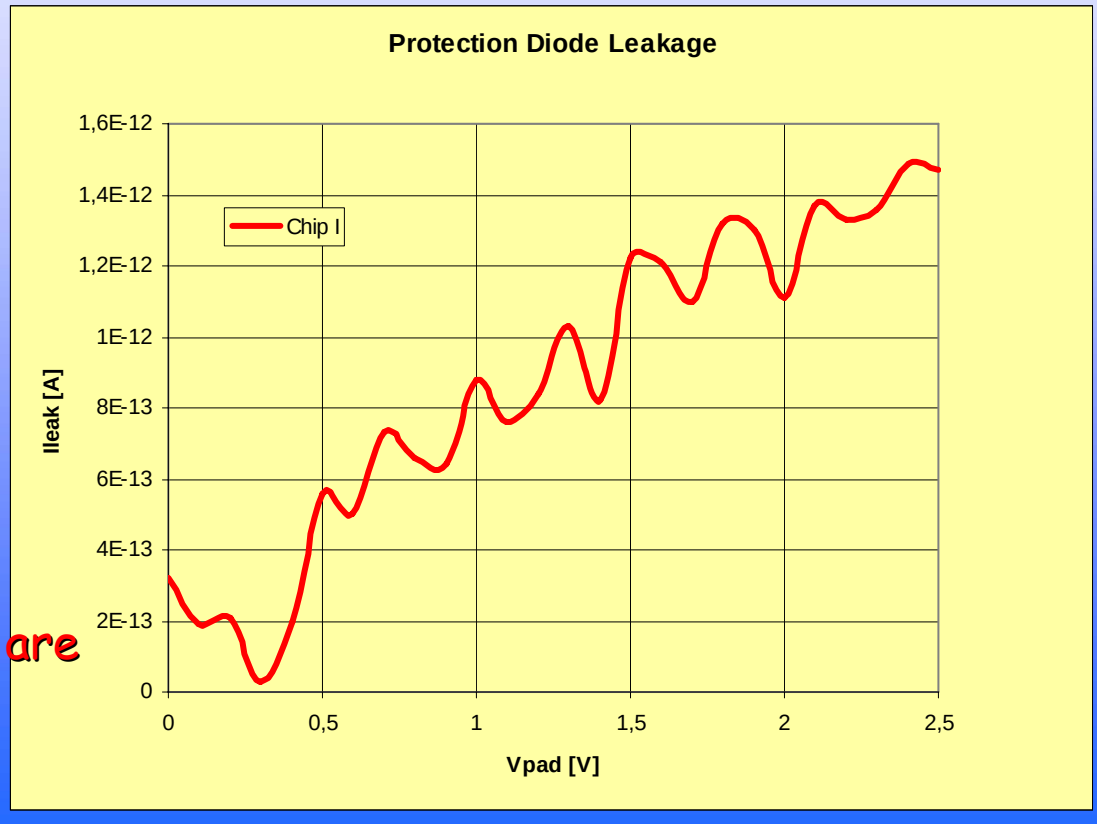
- HP 4156A high-precision semiconductor parameter tester
  - 4 HRSMUs (1fA res, 20fA accuracy)
  - 4-wire Celvin connections via Triax cables
- Custom made HPAD 0.1 DUT board
  - Flying leads & pin headers to connect to analyzer
  - CLCC 84 carrier & test socket
  - >5mm wire spacing when possible
  - Special cleaning procedure





Protection Diode Leakage

- Input of 'Buffer25'
  - ARM pad w. protection structures
  - Single ZVTDGNMOS gate
  - Defines basic accurancy, for which the following results are not corrected

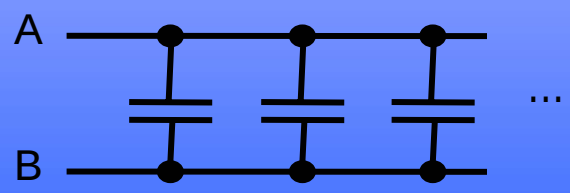


Capacitors on "hpad 0.1"

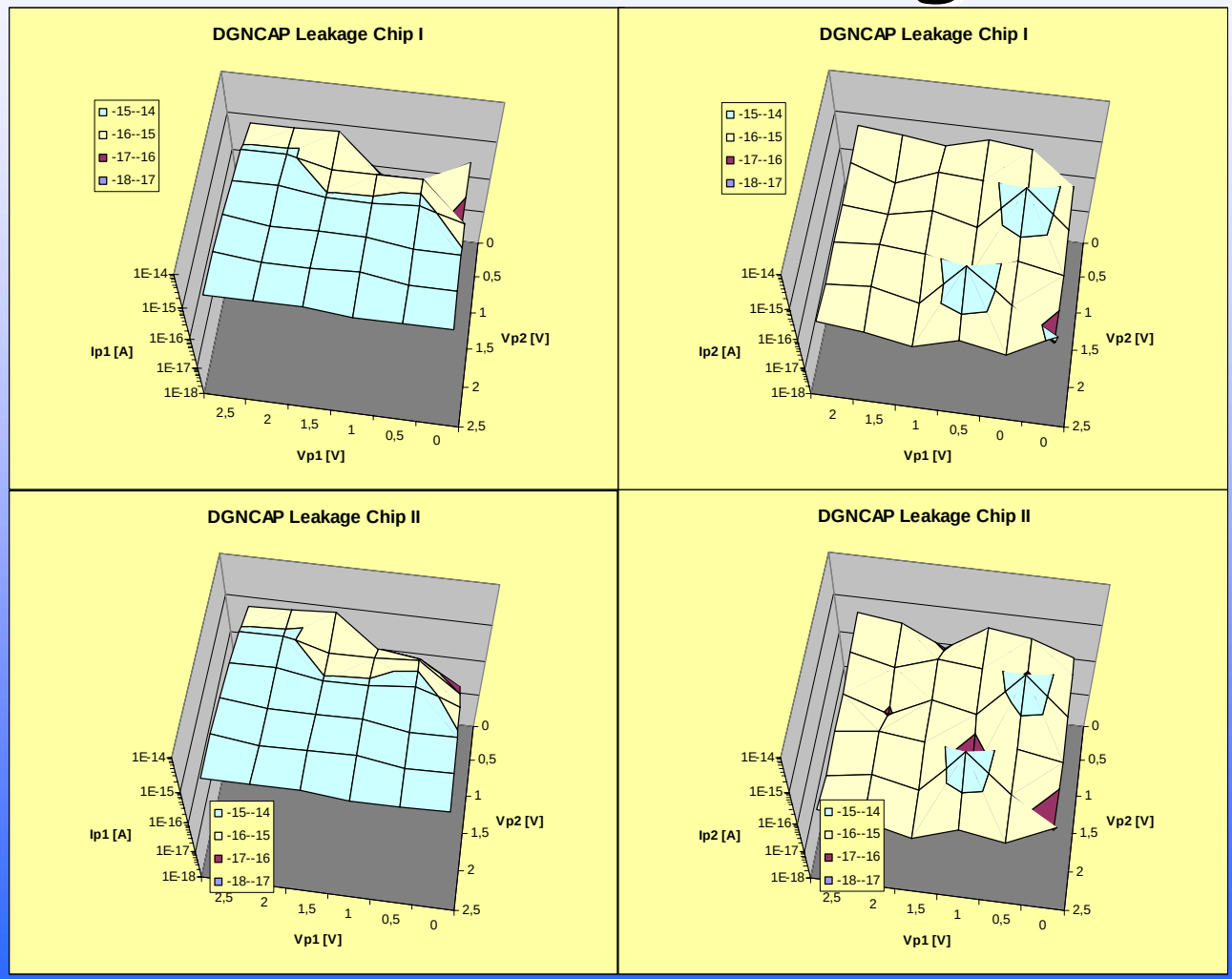
- DGNCAP (thick-oxide NMOS) array
  - 5.0µm ·5.0µm
  - 51.1...145.7fF
  - 8880 cells
- MIM cap array
  - 5.24µm ·5.24µm
  - 59.57fF
  - 8400 cells
- Dual MIM cap array
  - 8.5µm ·8.5µm
  - 680.17fF
  - 876 cells

$$\Delta U = \frac{t_{\text{store}} \cdot I_{\text{leak}}}{C_{\text{store}}}$$

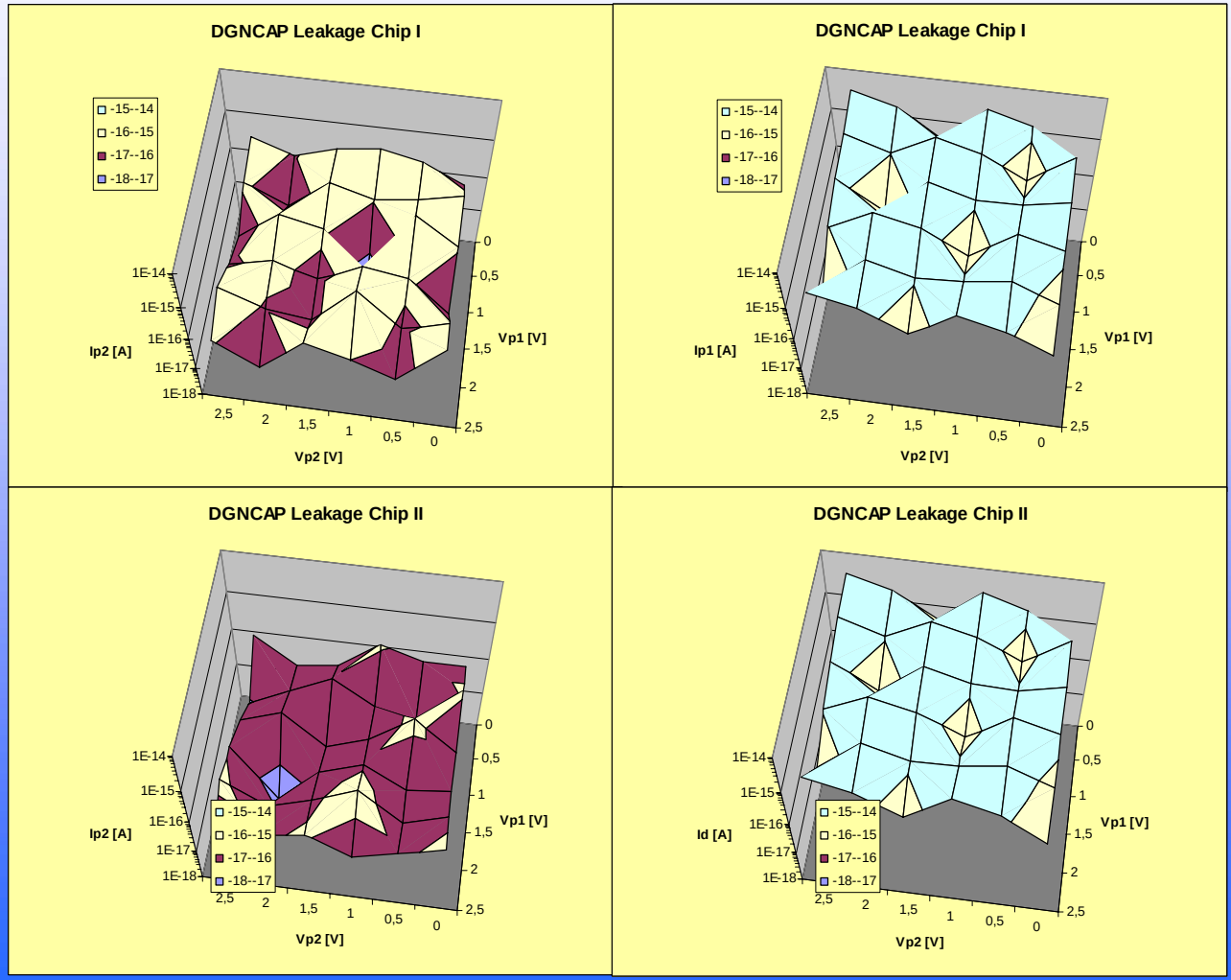
$$\left.\begin{aligned} C_{\text{store}} &= 100\text{fF} \\ t_{\text{store}} &= 100\text{ms} \\ \Delta U &\le 1\text{mV}\ (1\%\ @\ 1\text{V}) \end{aligned}\right\} I_{\text{leak}} \le 1\text{fA}$$



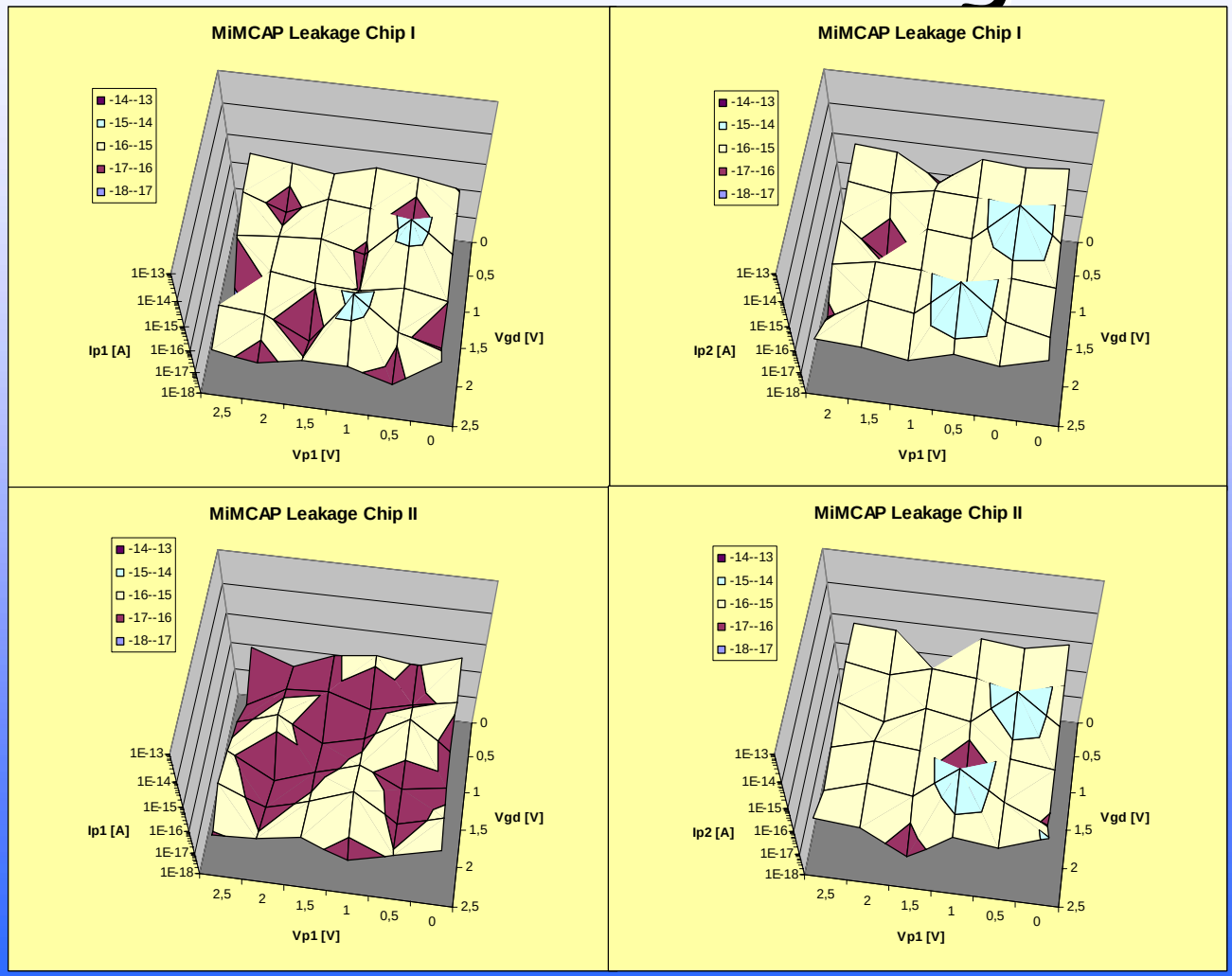
DGNCAP Leakage



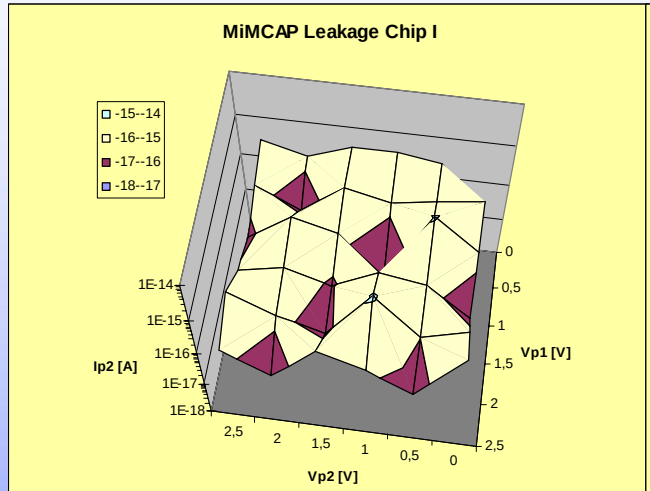
DGNCAP Leakage

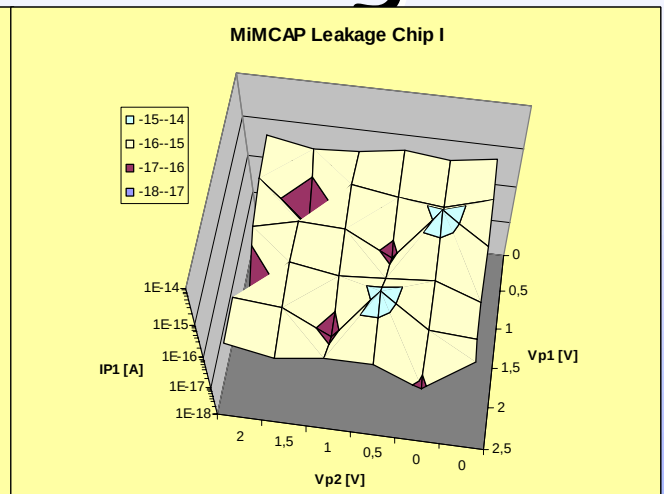


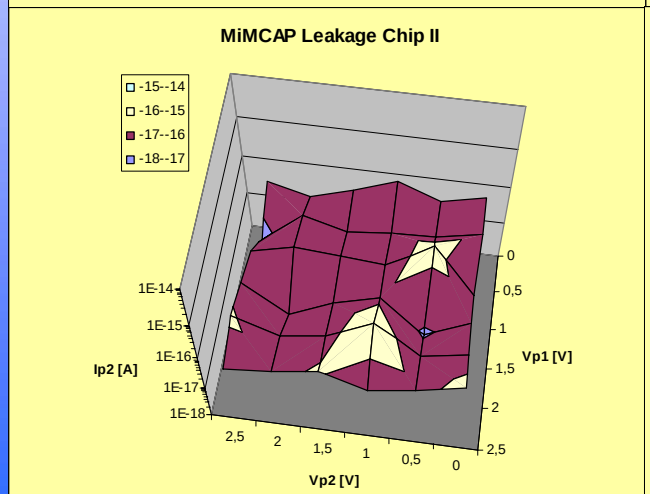
MiMCAP Leakage

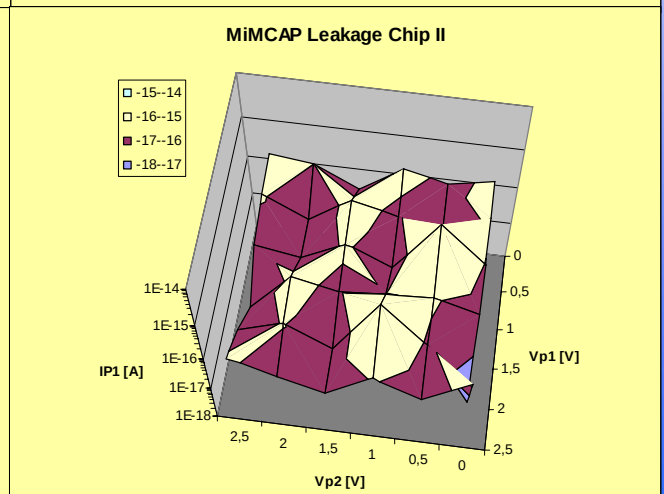


MiMCAP Leakage

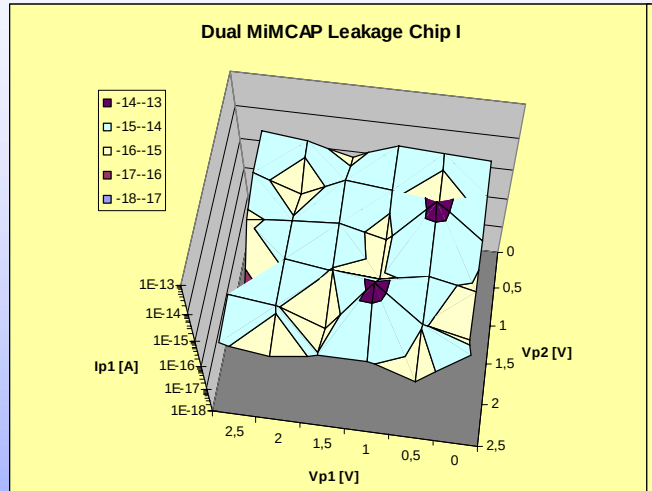


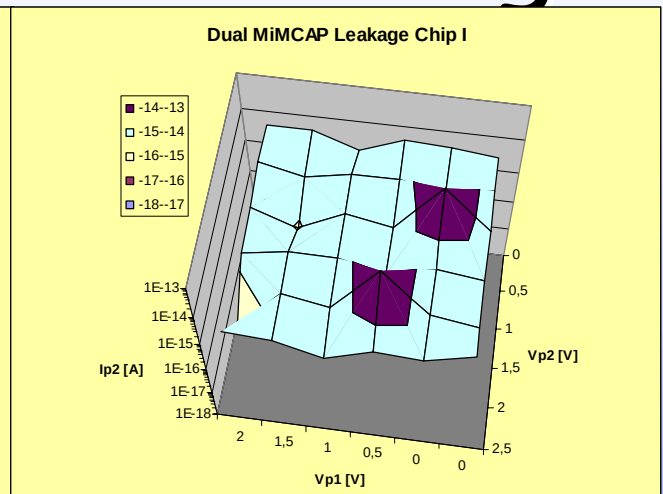


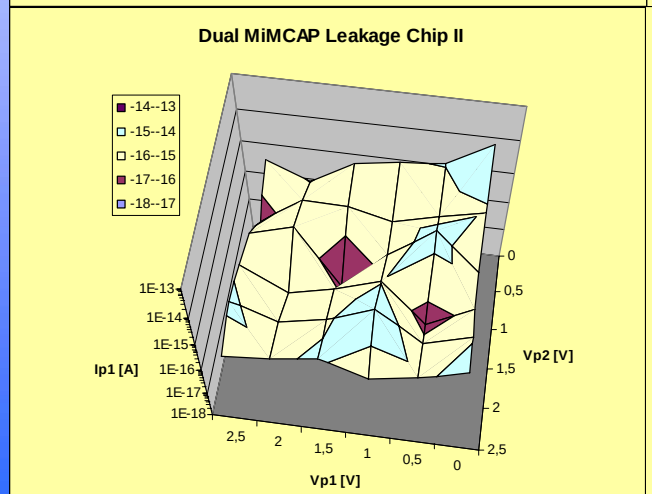


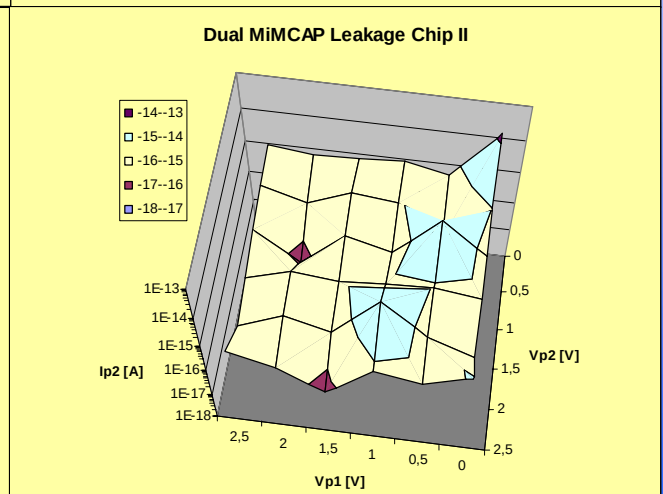


Dual MiMCAP Leakage

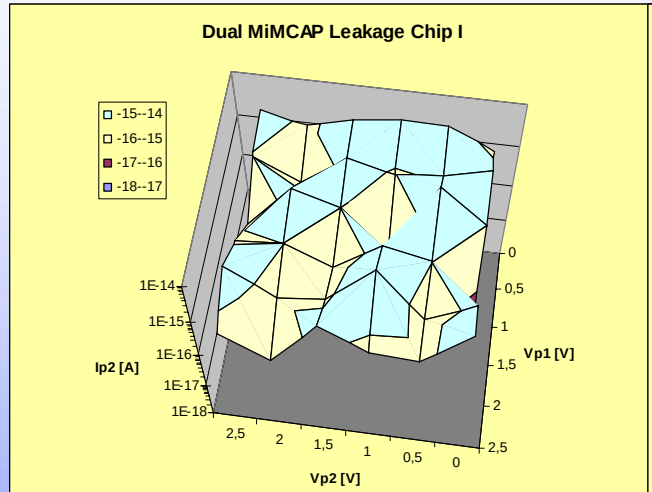


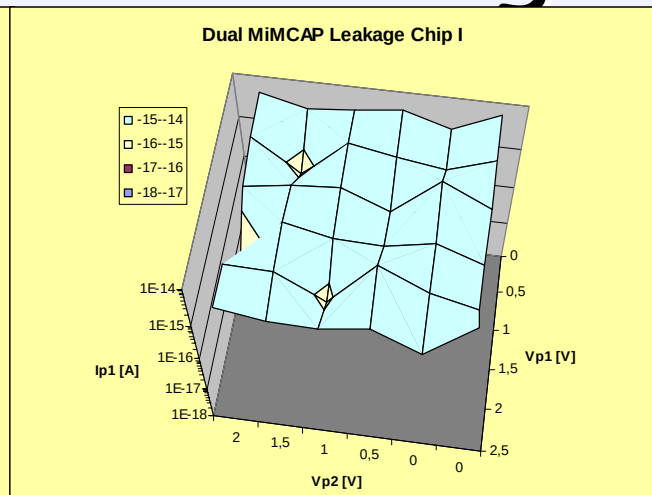


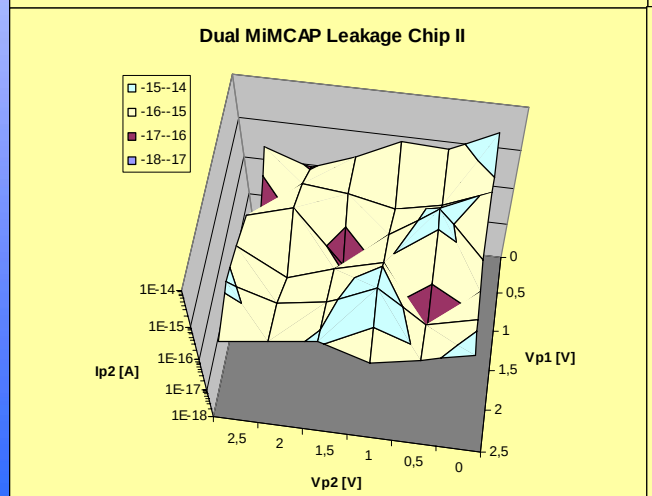


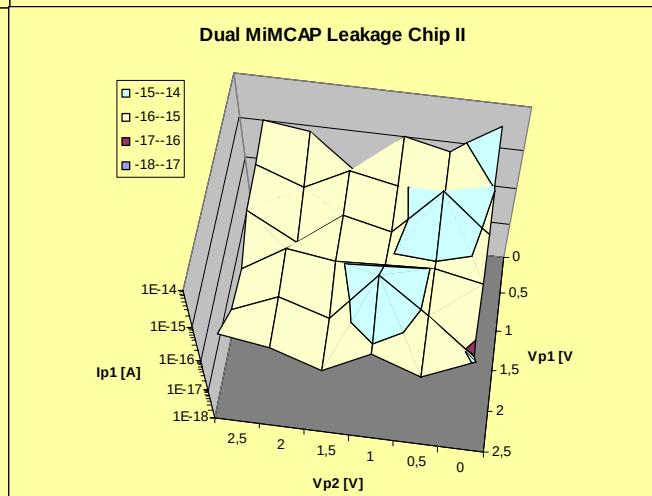


Dual MiMCAP Leakage



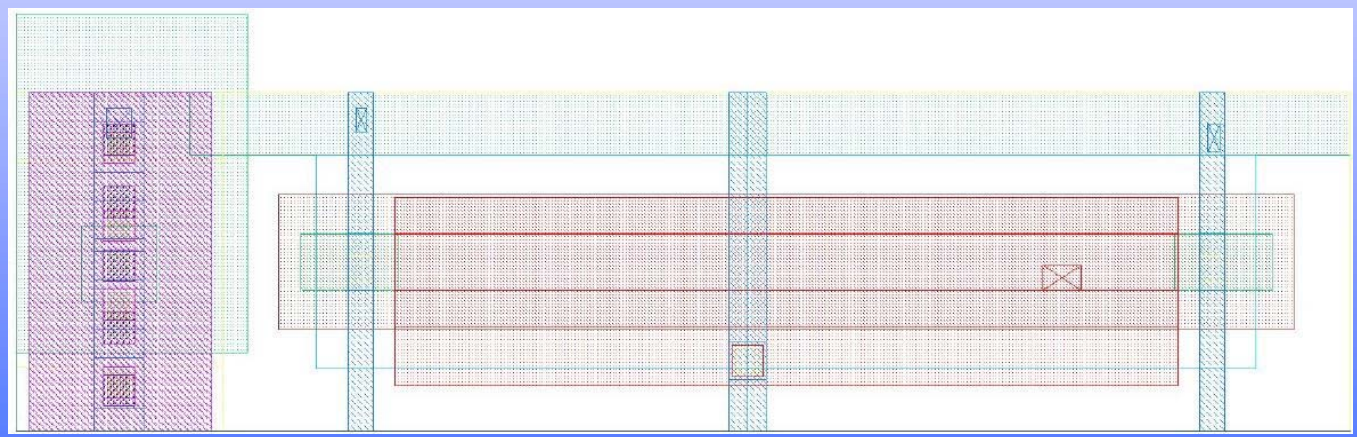




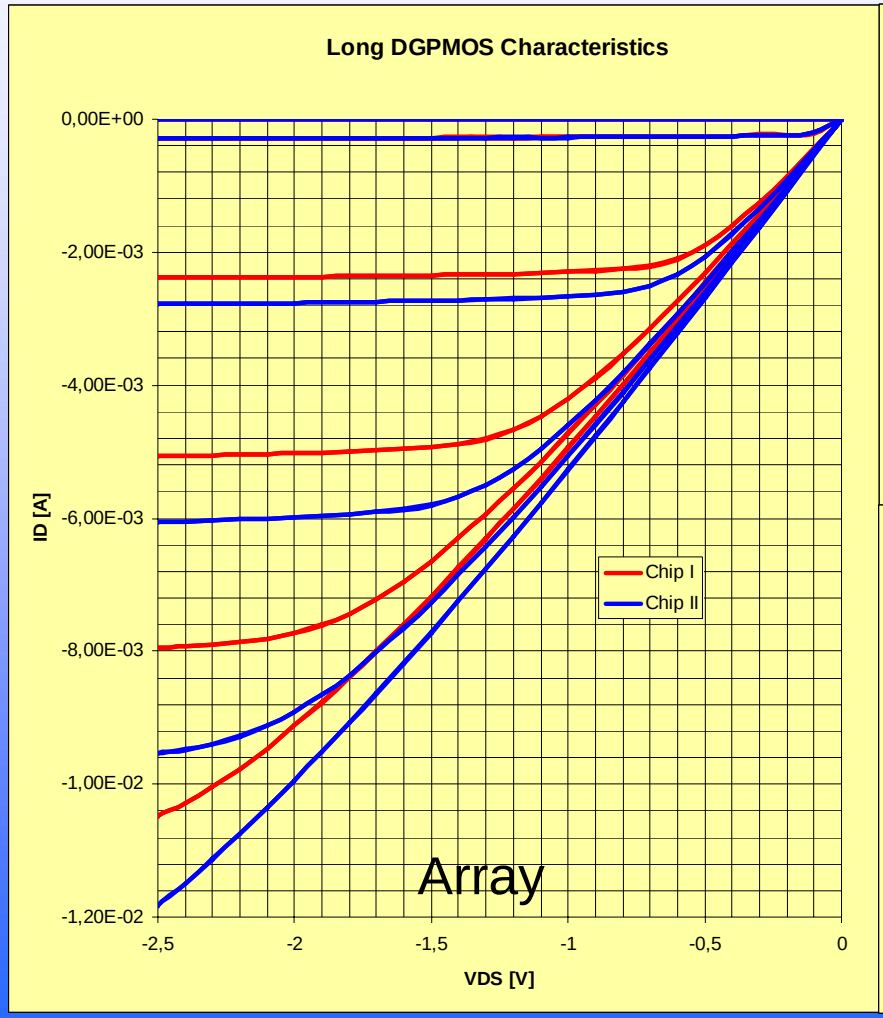


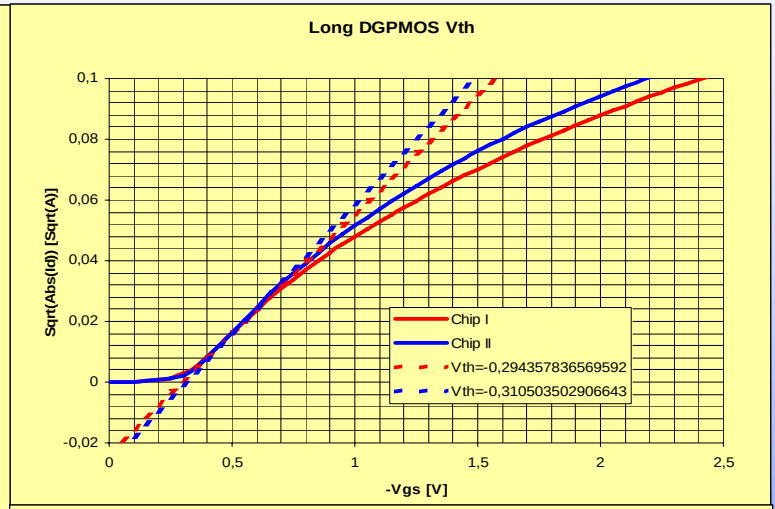
Linear FET switches on "hpad 0.1"

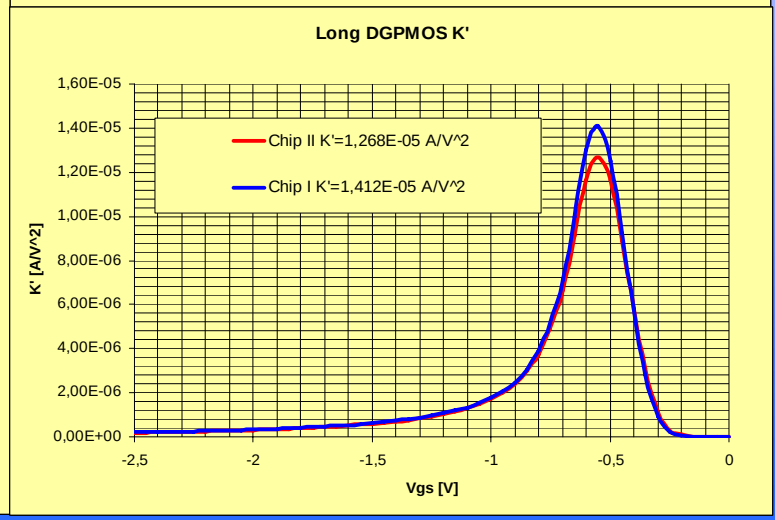
- Long DGPMOS (thick-oxide PMOS) switch array
  - W/L = 0.36µm / 5.0µm
  - 27142 cells



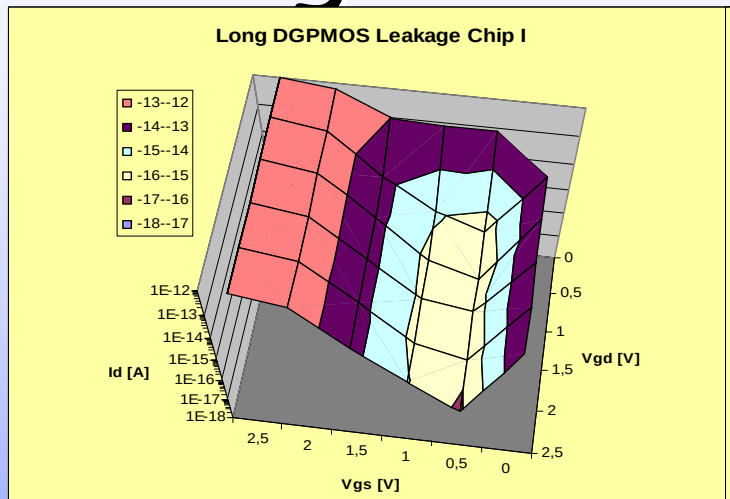
Long DGPMOS Characteristics

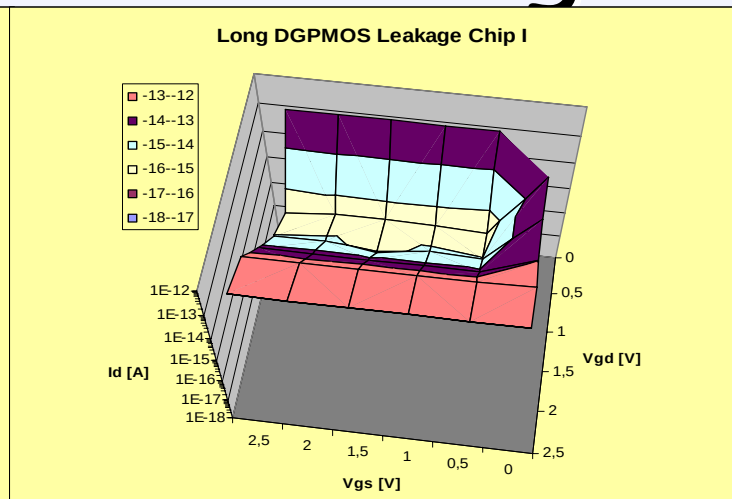


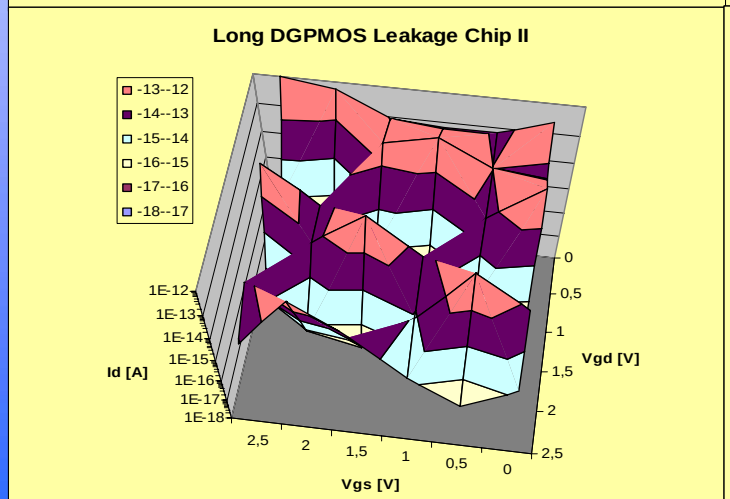


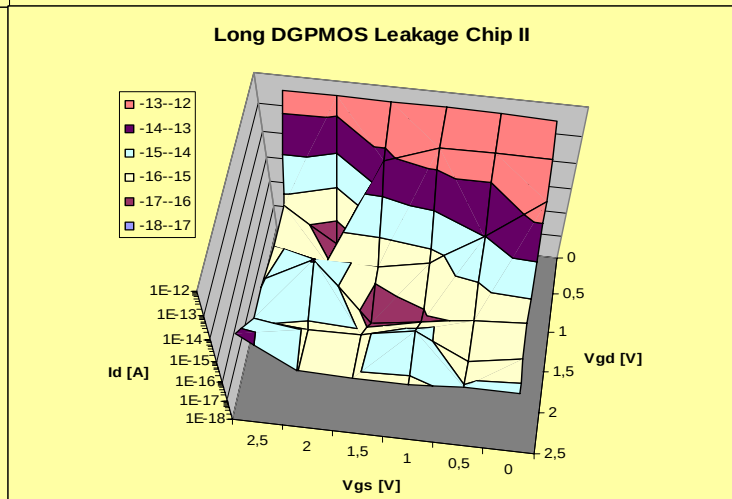


Long DGPMOS Leakage

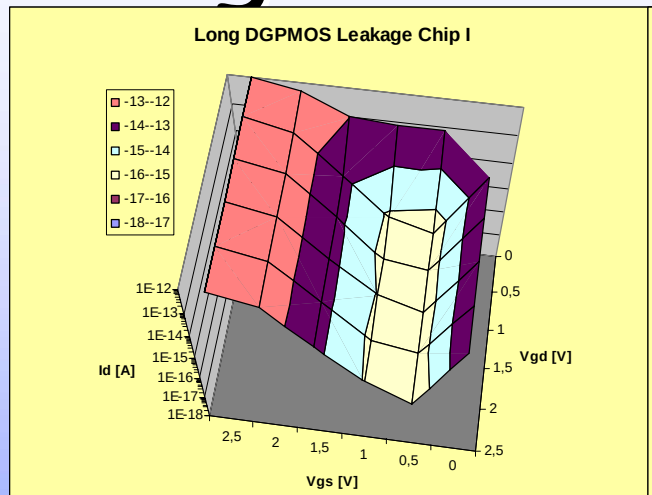


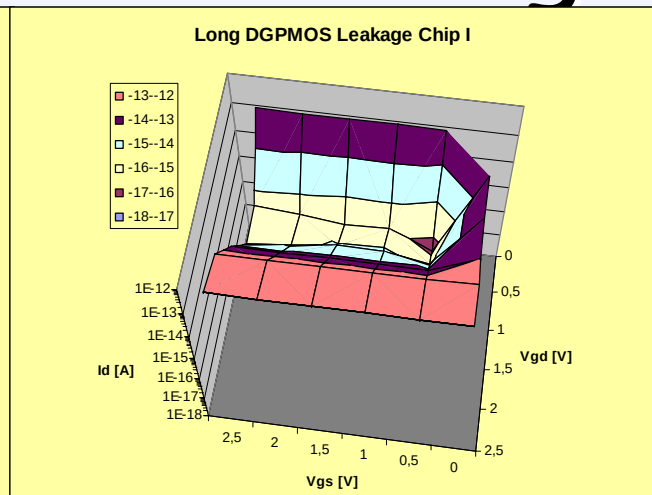


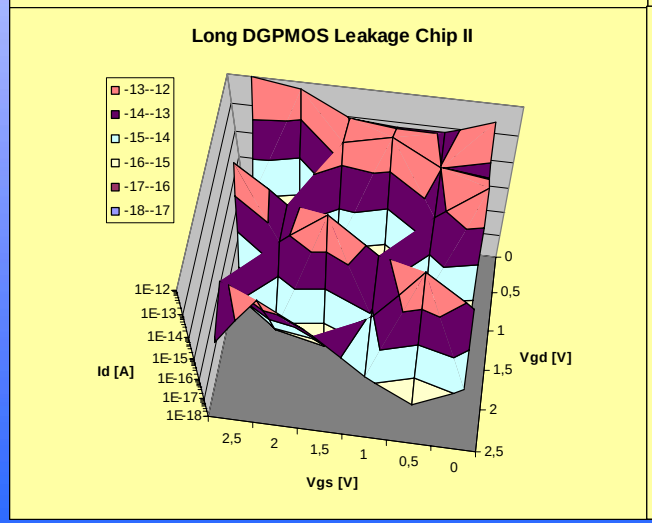


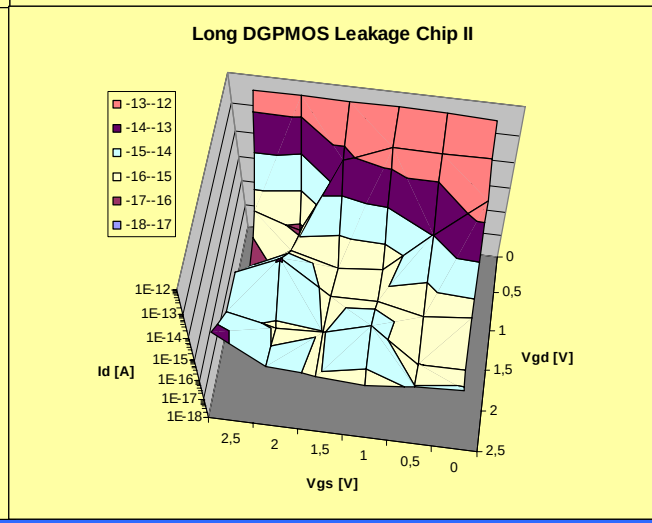


Long DGPMOS Leakage



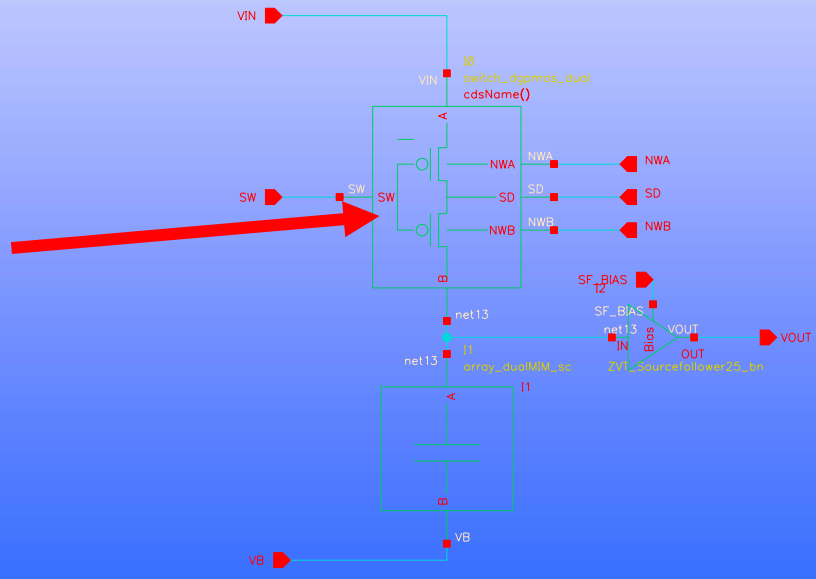




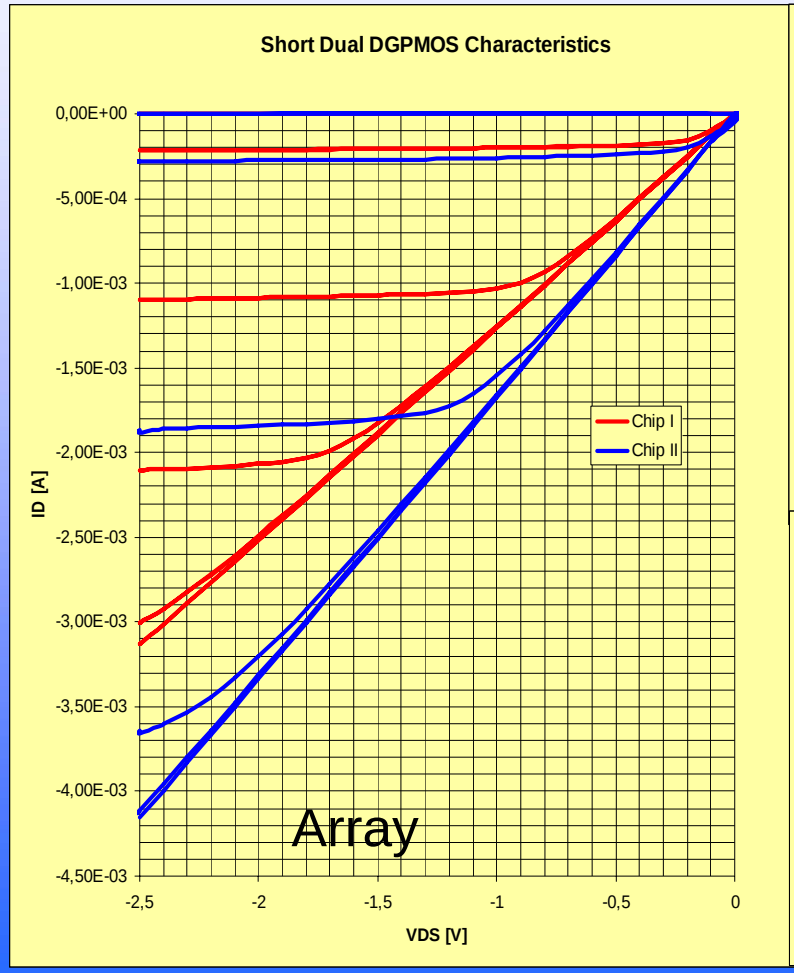


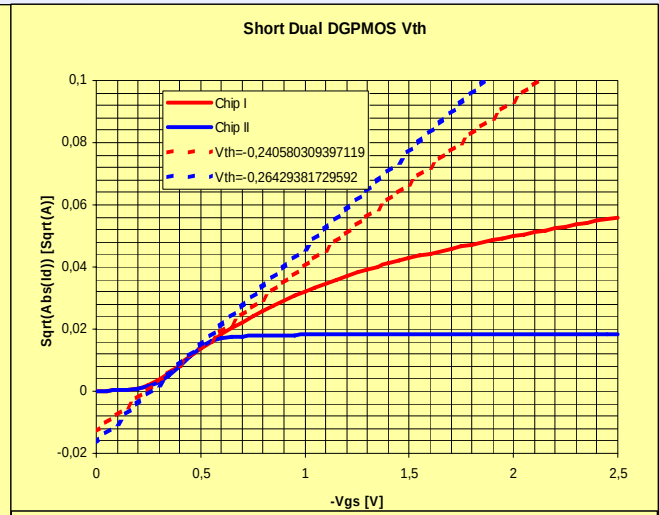
Dual PMOS switches on "hpad 0.1"

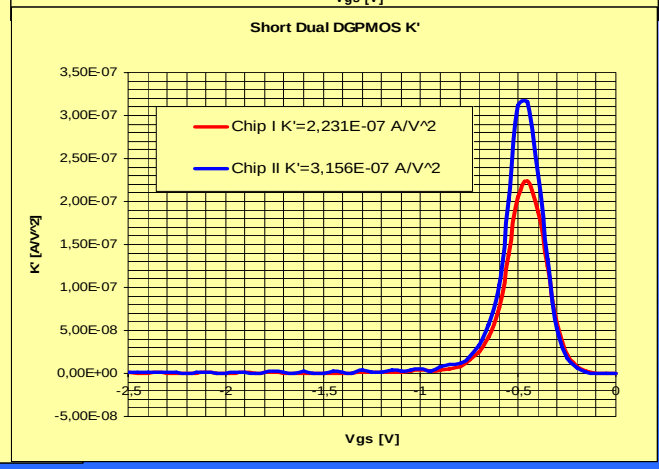
- Array of dual DGPMOS switches
  - W/L 0.36µm/2µm and 0.36µm/0.24µm



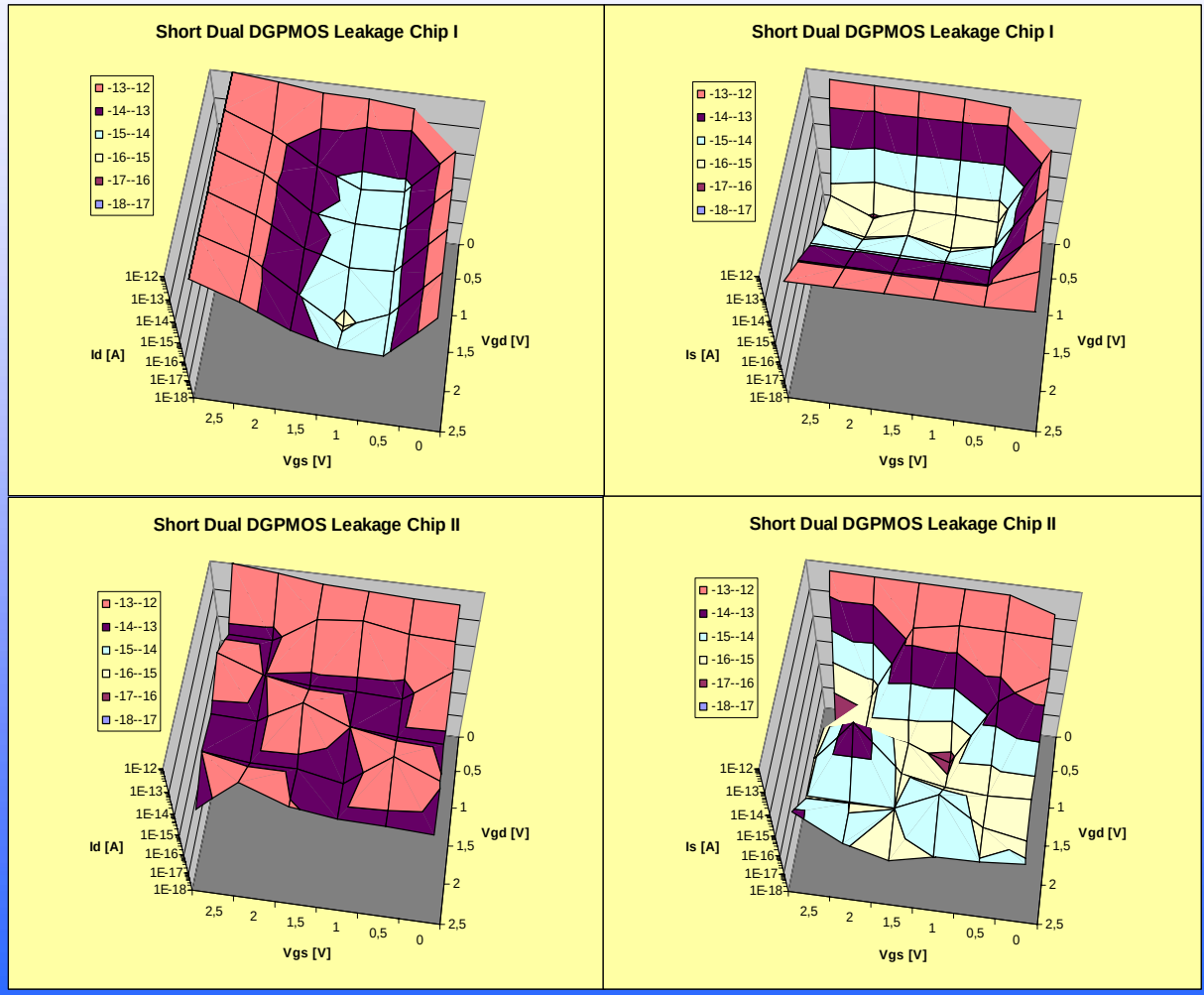
Short Dual PMOS Characteristics



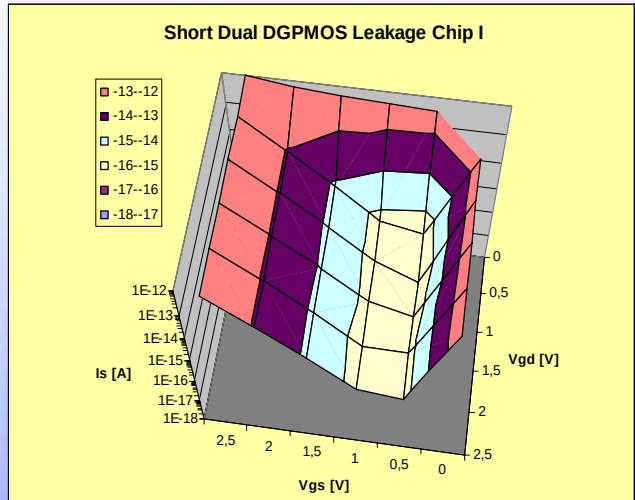


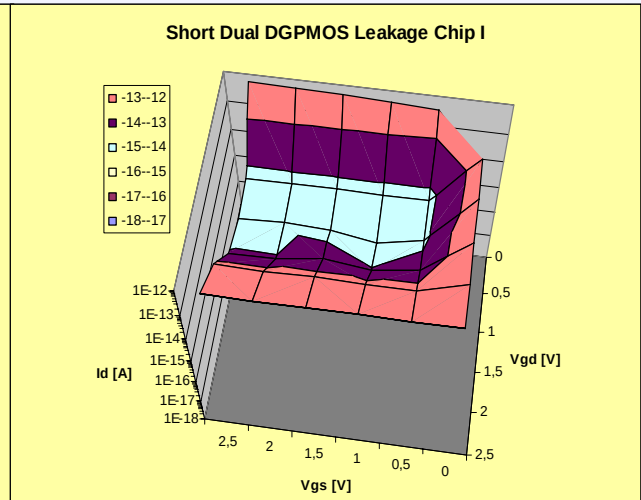


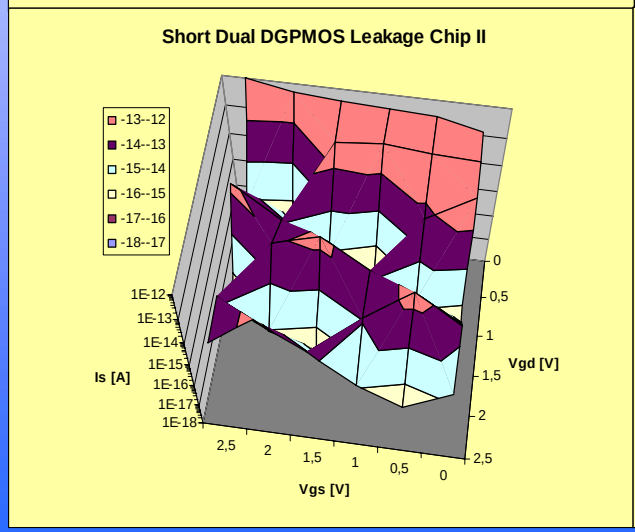
Short Dual PMOS Leakage

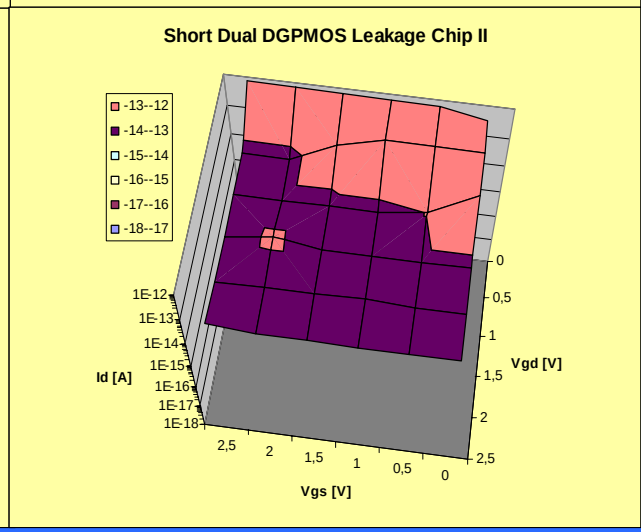


Short Dual PMOS Leakage

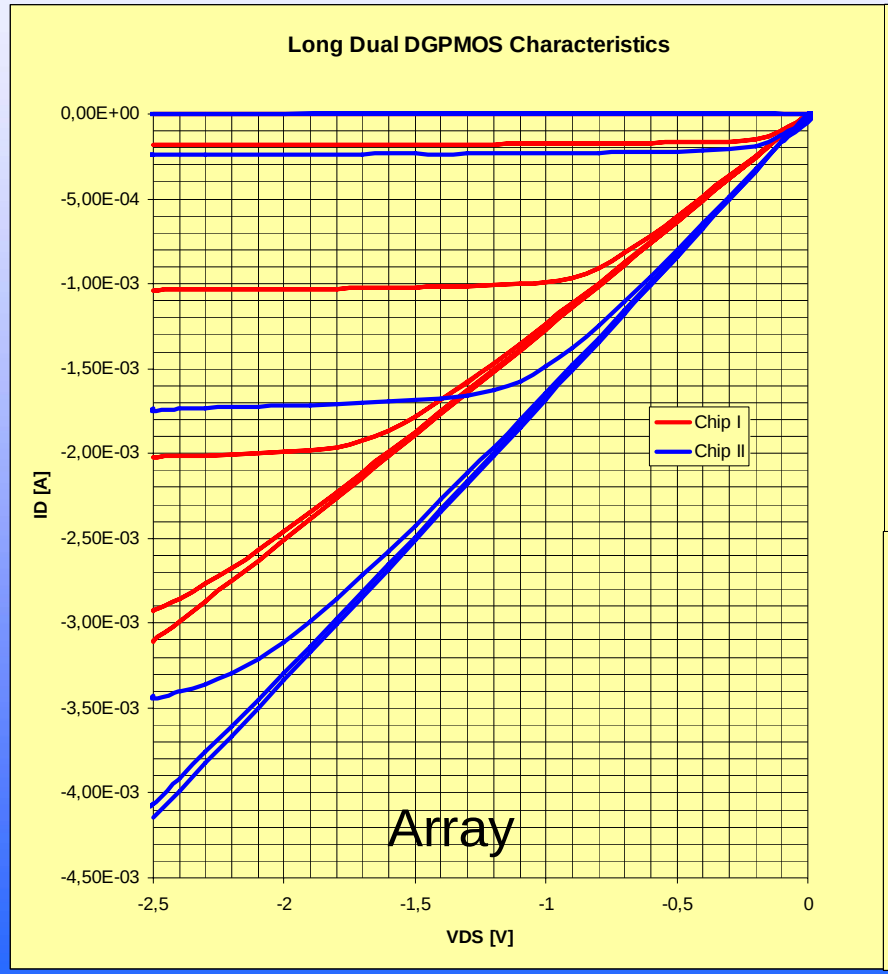


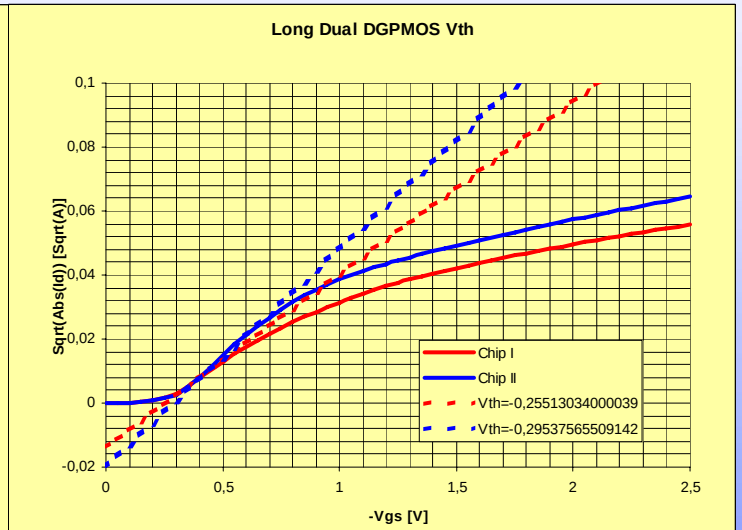


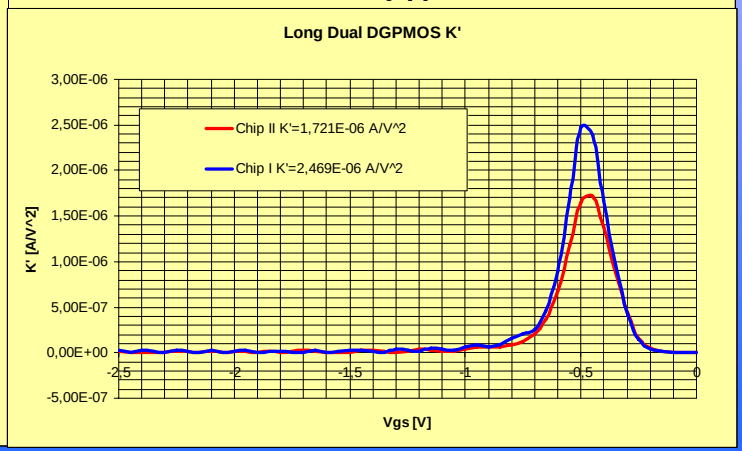




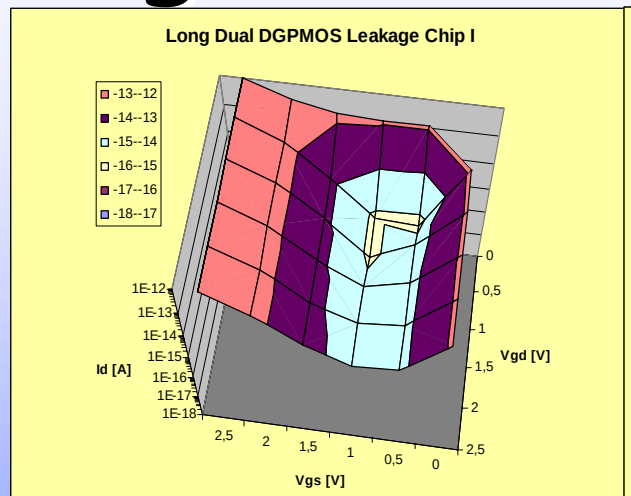
Long Dual PMOS Characteristics

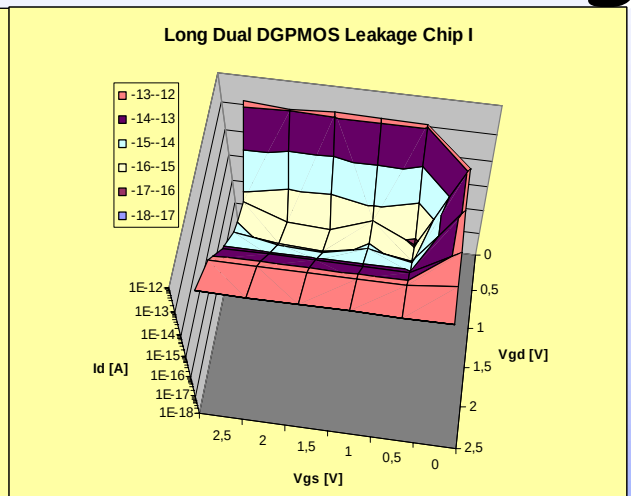


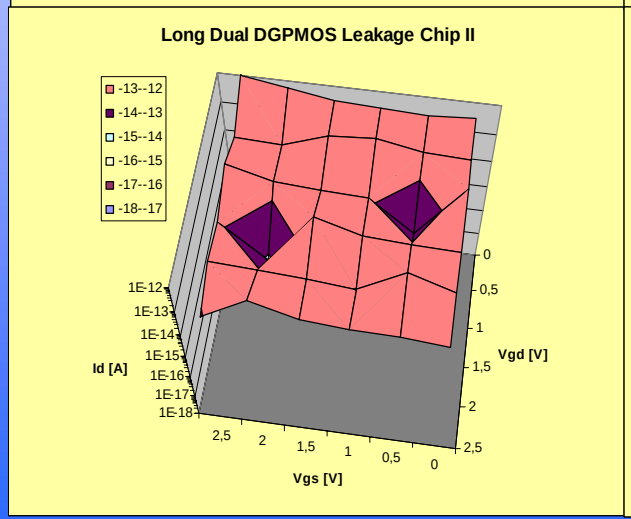


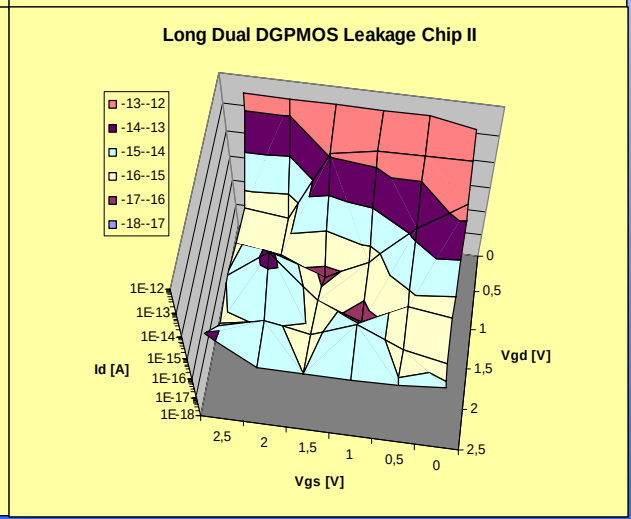


Long Dual PMOS Leakage

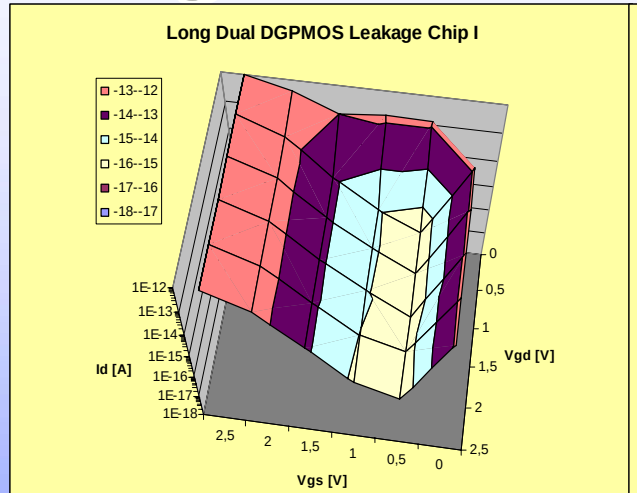


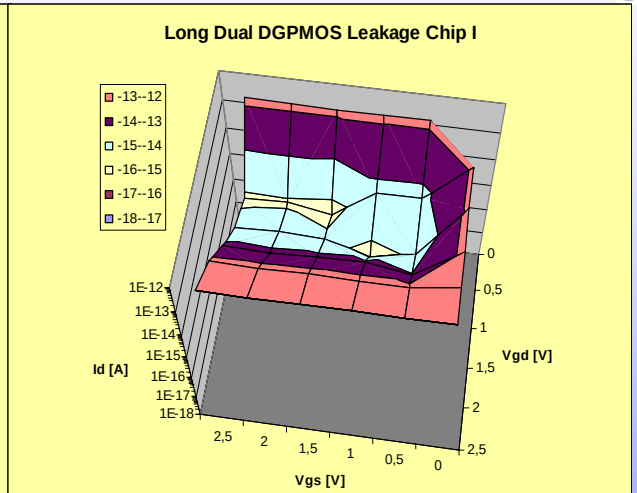


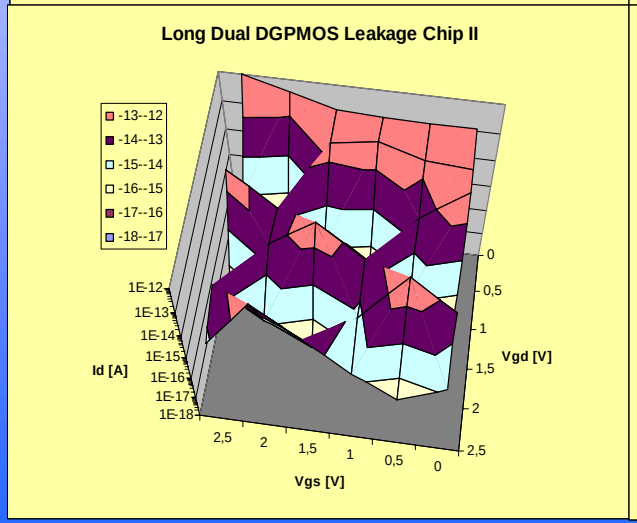


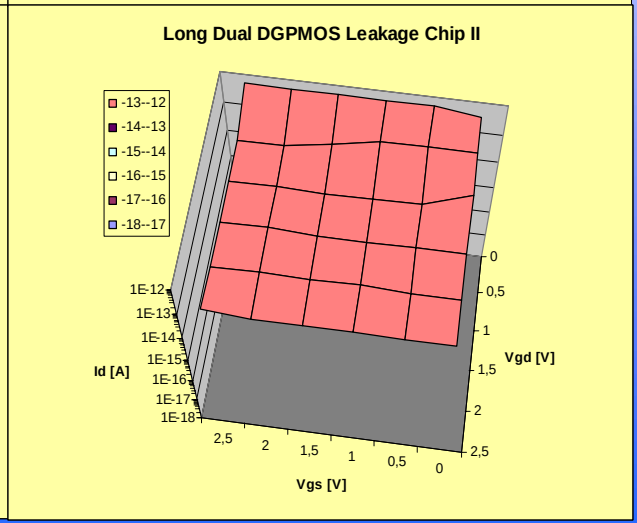


Long Dual PMOS Leakage



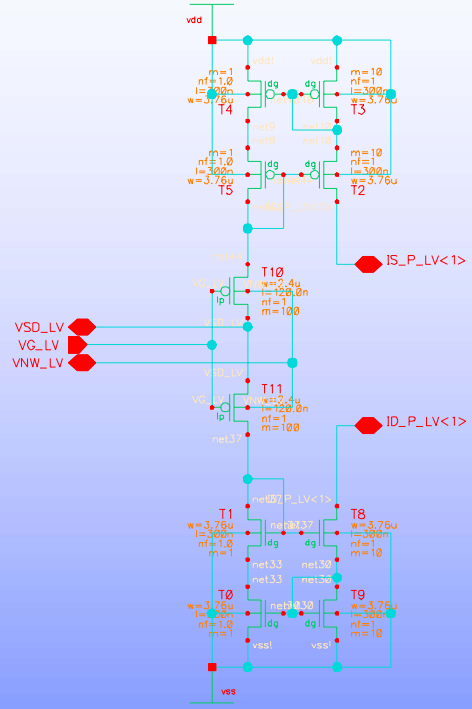


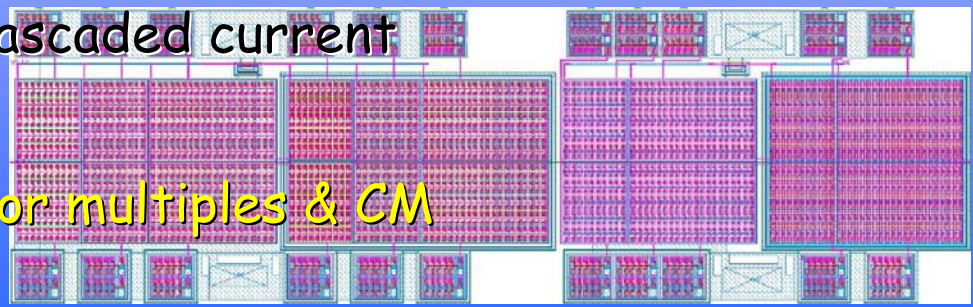




Enclosed FET switches on "hpad 0.1"

- LPPMOS (thin-oxide high-Vt PMOS)
- LPNMOS (thin-oxide high-Vt NMOS)
- DGPMOS (thick-oxide PMOS)
- DGNMOS (thick-oxide NMOS)
- 100 or 200 transistors
- Different W/L
- S & D readout via x10 cascaded current mirrors
- Results not corrected for multiples & CM ratio!

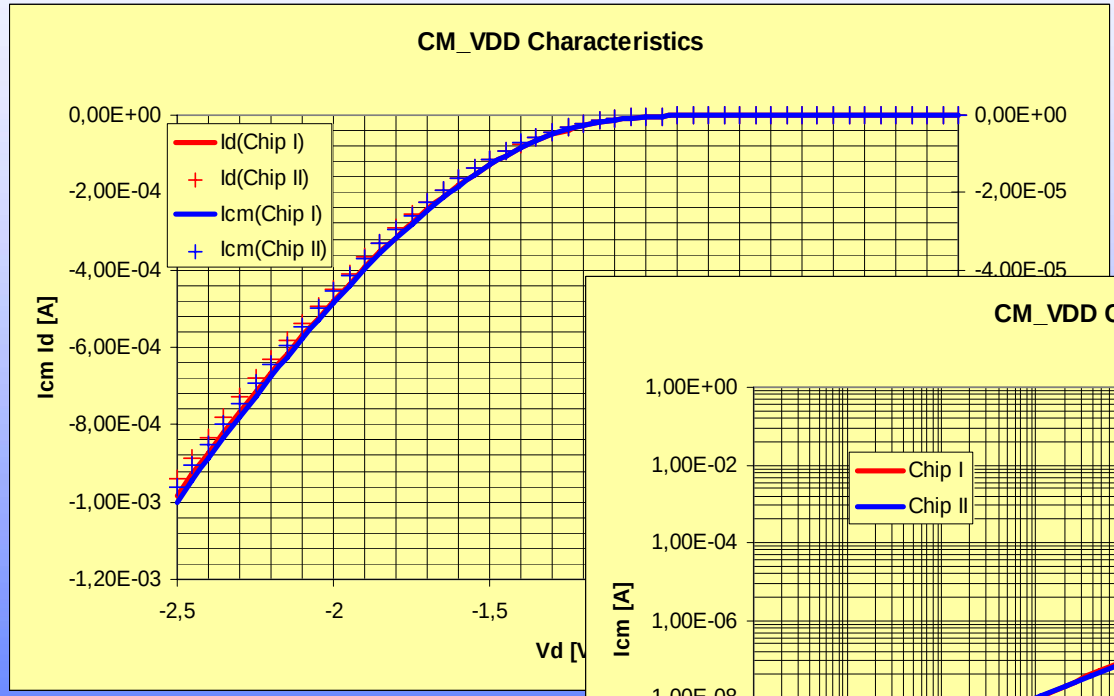


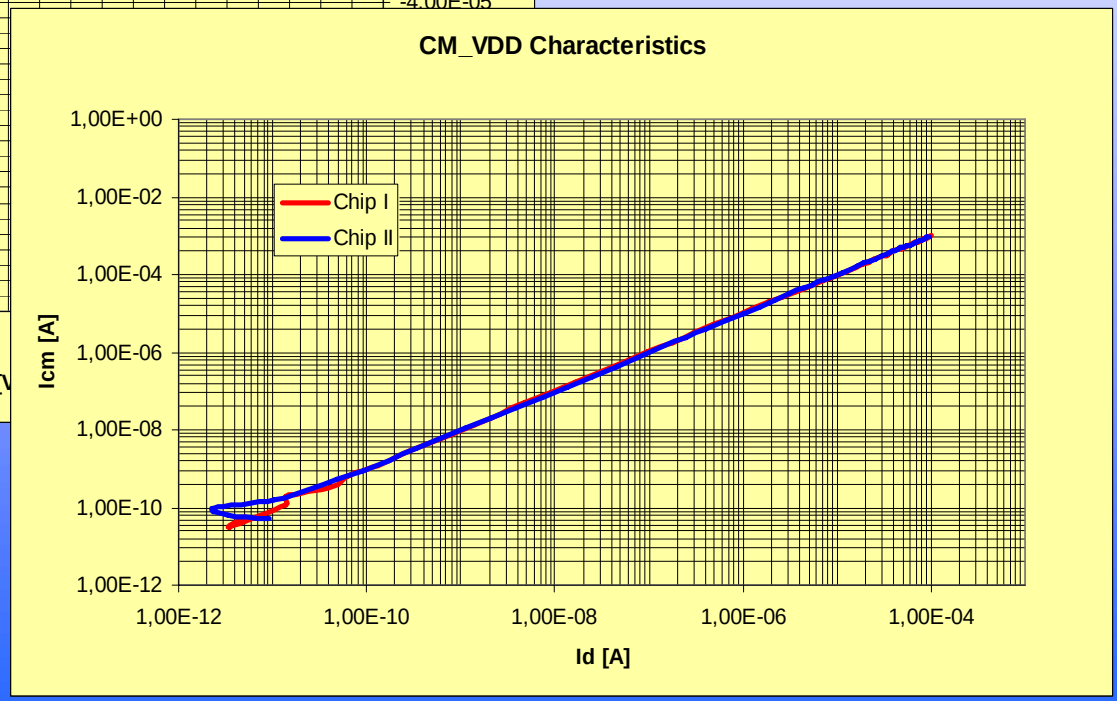


Enclosed FET switches on "hpad 0.1"

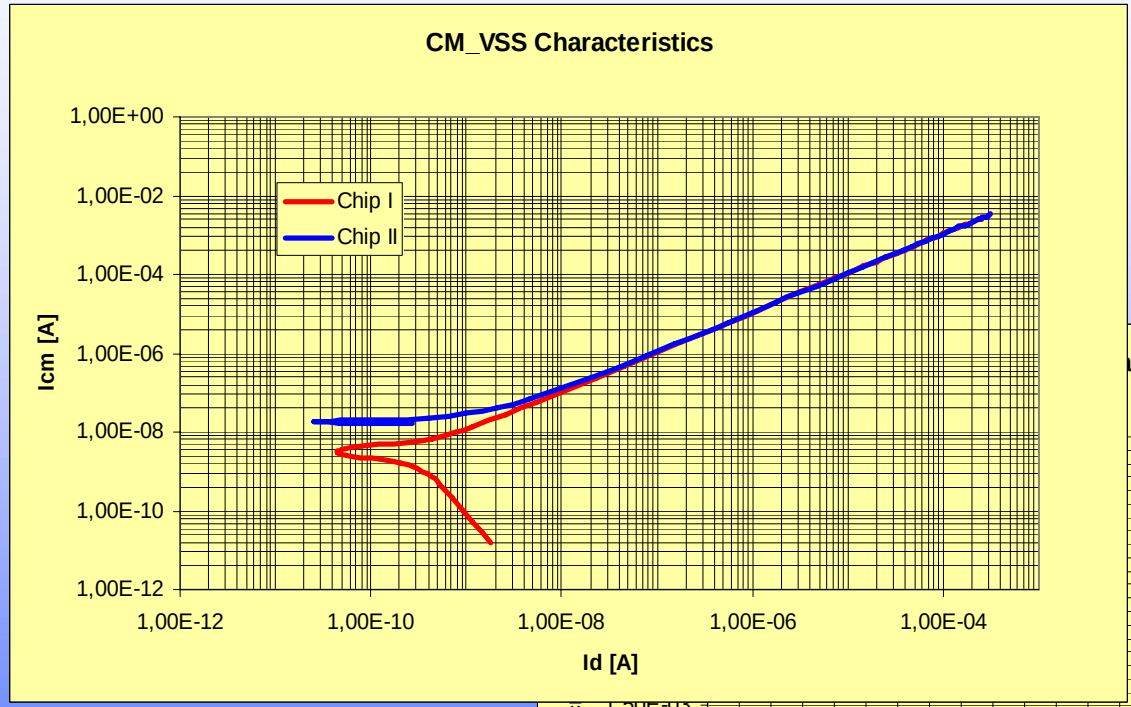
Nr.	Transistor Type [1]	W [µm]	L [µm]	Multi-plier	Source Node	Drain Node
1	LPNMOS	3.040.12100	IS N	LV< 1 >	ID N	LV< 1 >
2	LPNMOS	3.040.24100	IS N	LV< 2 >	ID N	LV< 2 >
3	LPNMOS	3.040.24200	IS N	LV< 3 >	ID N	LV< 3 >
4	LPPMOS	3.040.12100	IS P	LV< 1 >	ID P	LV< 1 >
5	LPPMOS	3.040.24100	IS P	LV< 2 >	ID P	LV< 2 >
6	LPPMOS	3.040.24200	IS P	LV< 3 >	ID P	LV< 3 >
7	DGNMOS	3.040.24100	IS N	DG< 1 >	ID N	DG< 1 >
8	DGNMOS	3.040.24200	IS N	DG< 2 >	ID N	DG< 2 >
9	DGPMOS	3.040.24100	IS P	DG< 1 >	ID P	DG< 1 >
10	DGPMOS	3.040.24200	IS P	DG< 2 >	ID P	DG< 2 >

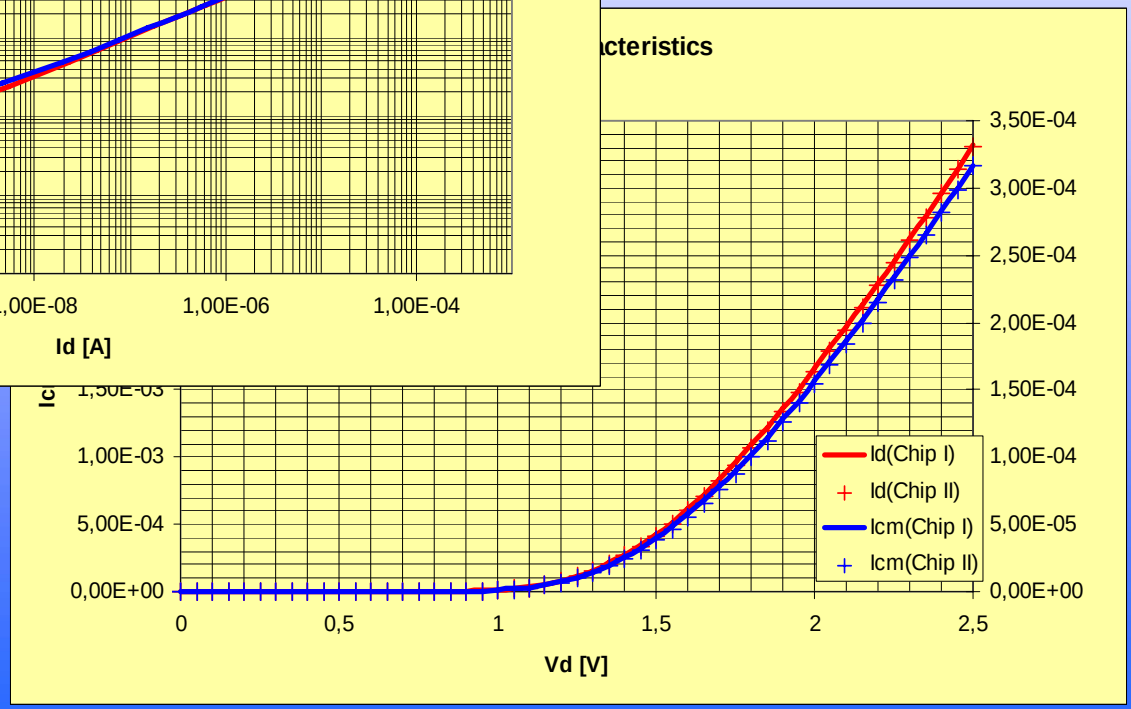
VDD Current Mirror



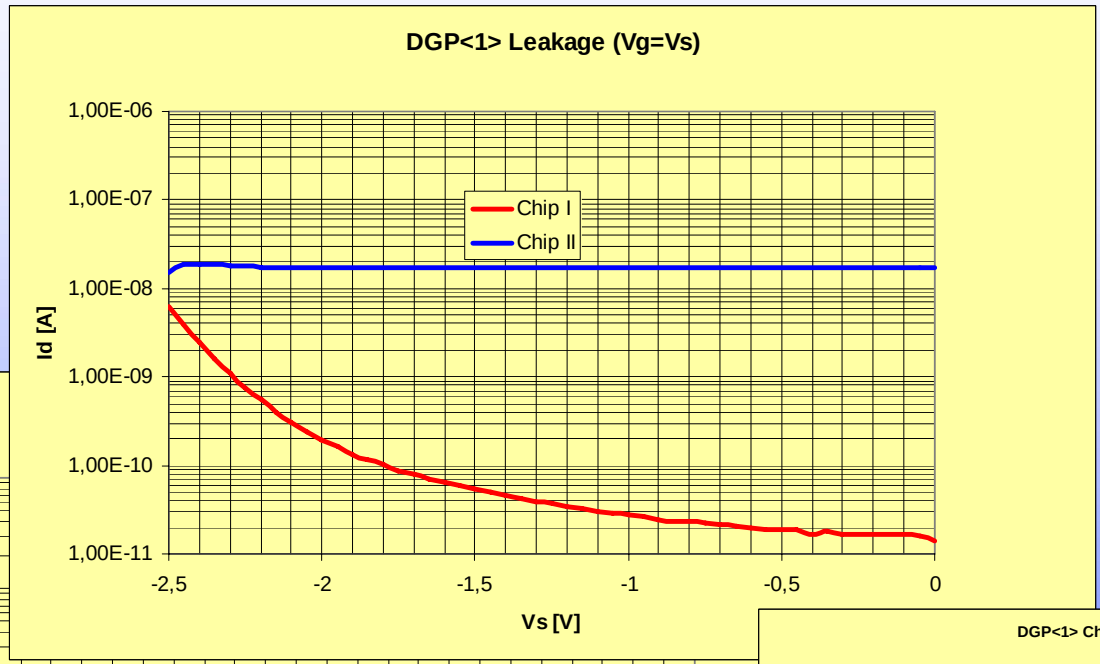


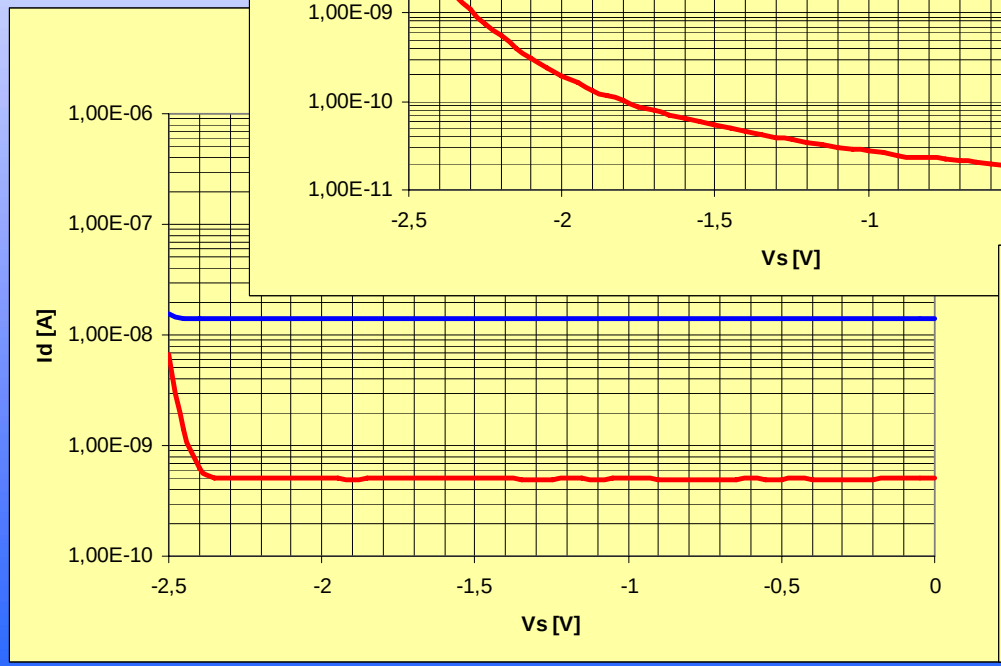
VSS Current Mirror

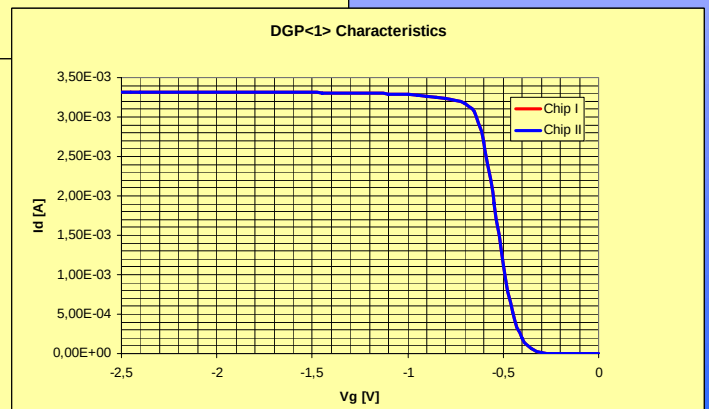




DGPMOS<1>

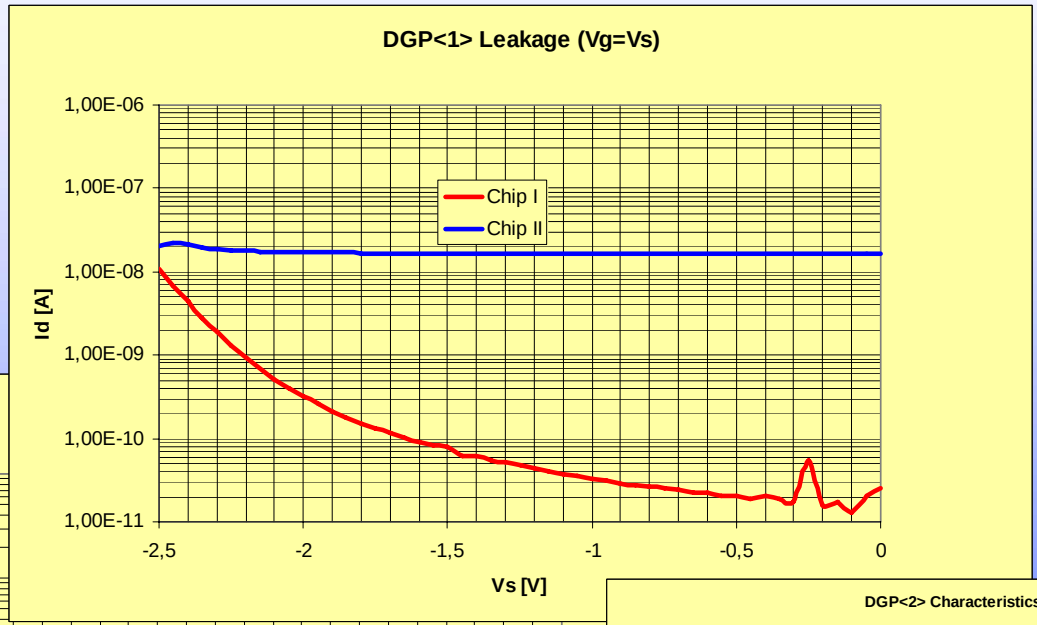


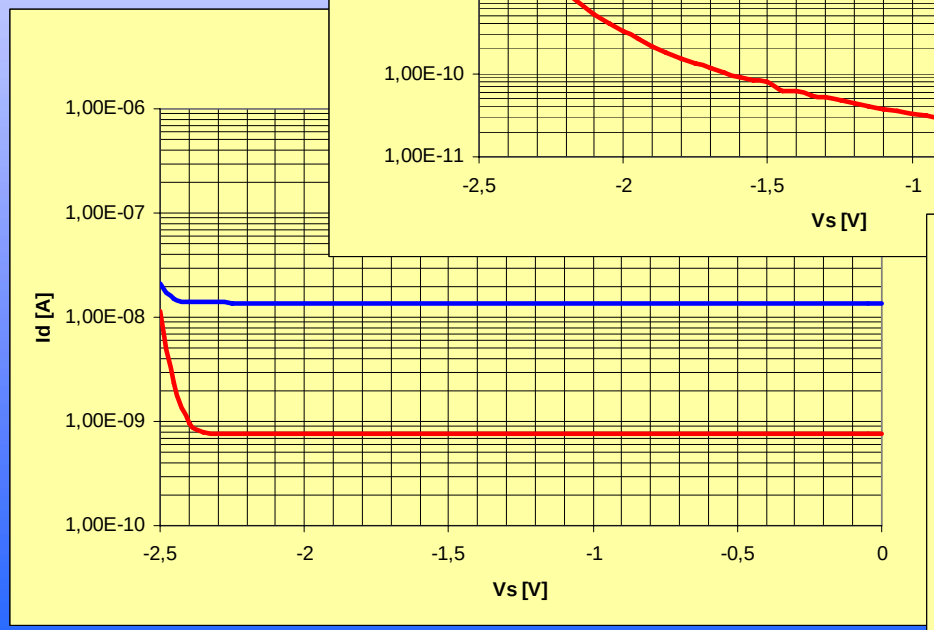


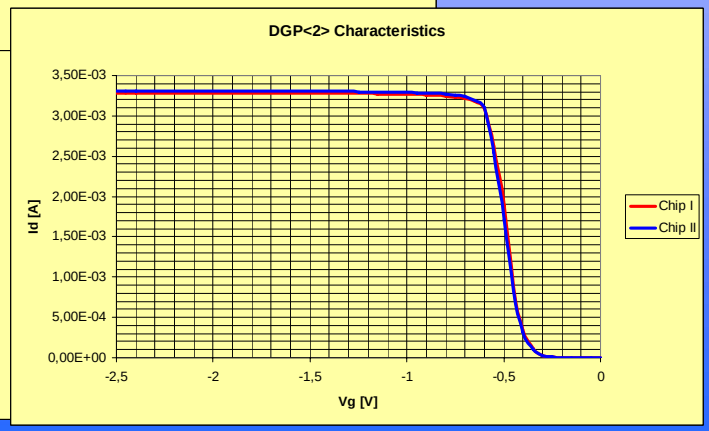


W=3.04um
L= 0.24um
N= 100

DGPMOS<2>

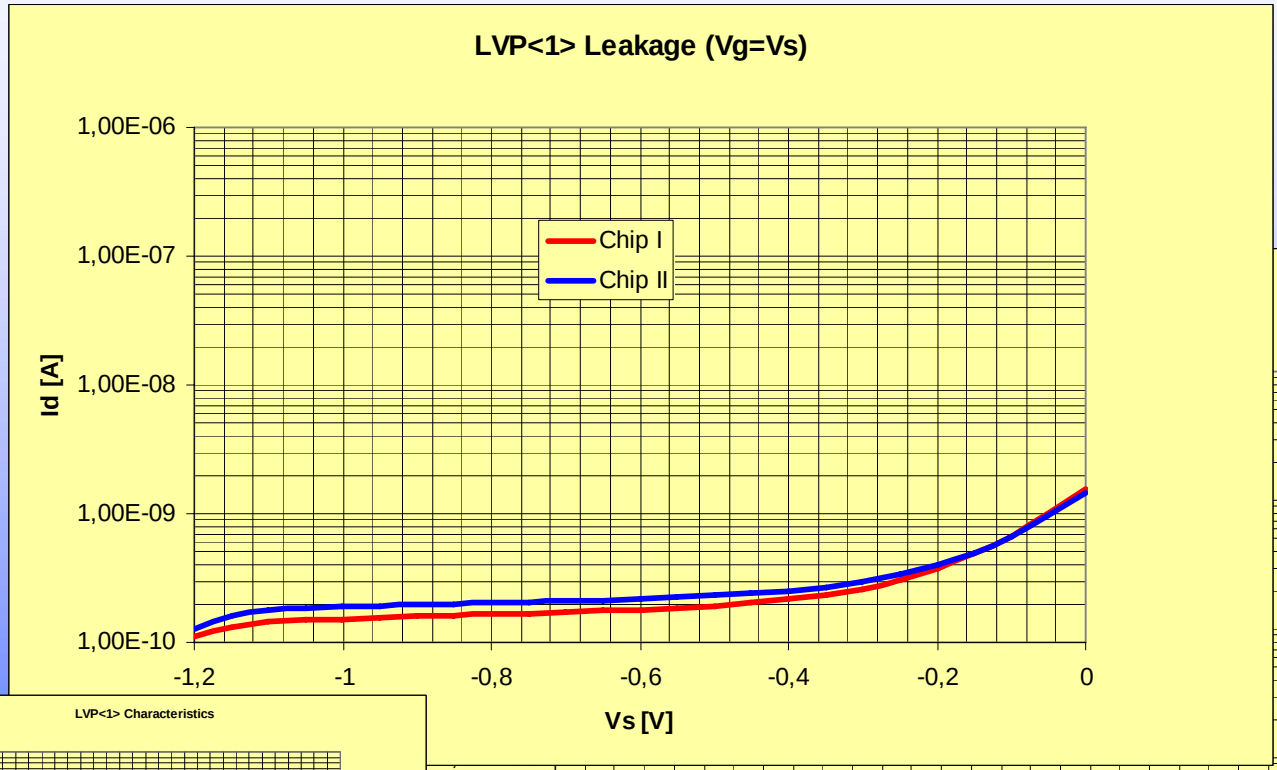




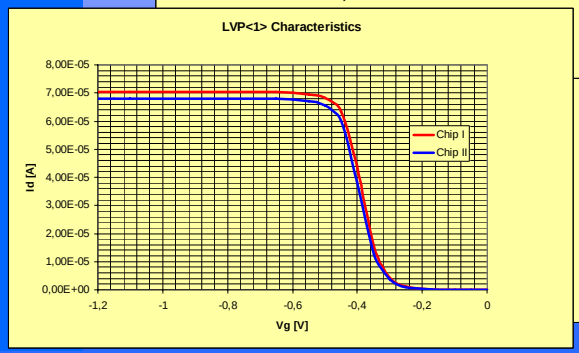


W=3.04um
L= 0.24um
N= 200

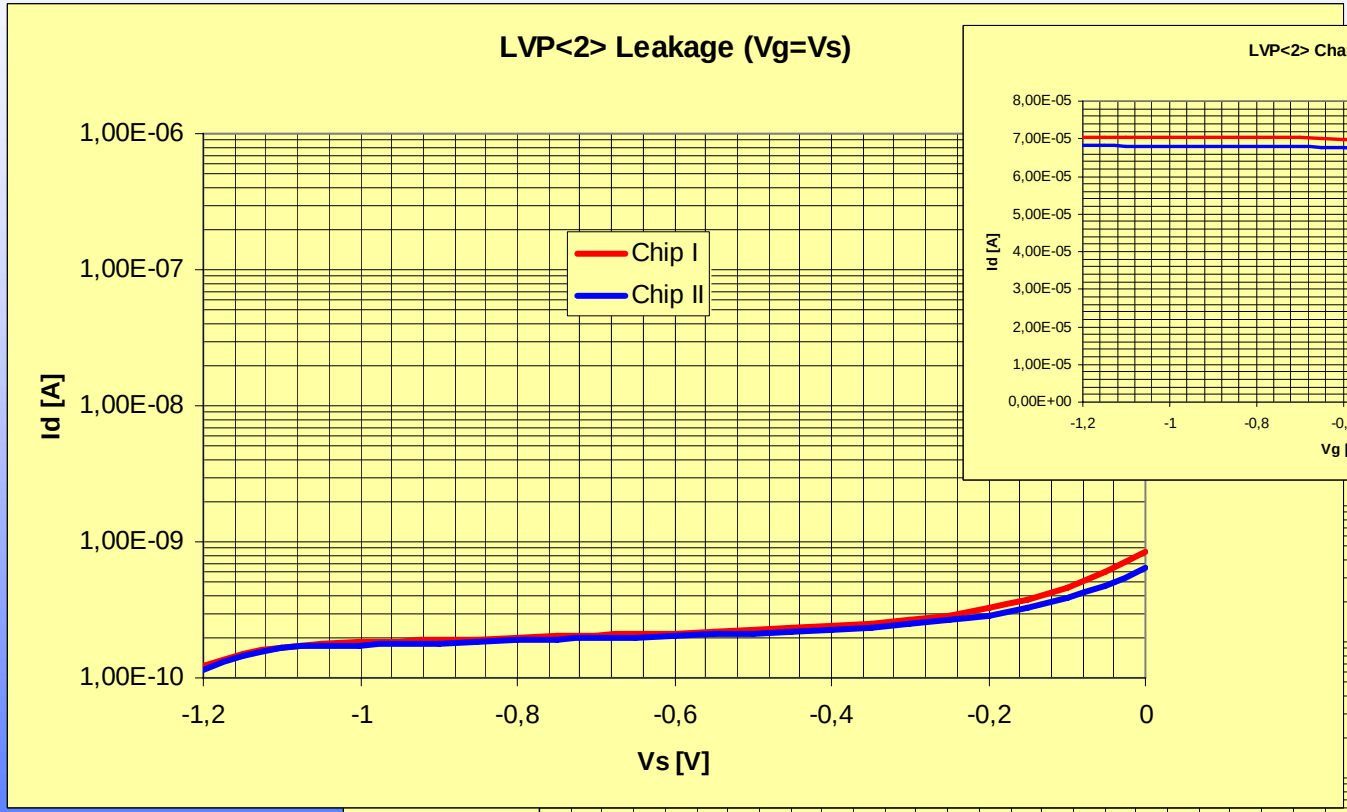
LPPMOS<1>



W=3.04um
L= 0.12um
N= 100

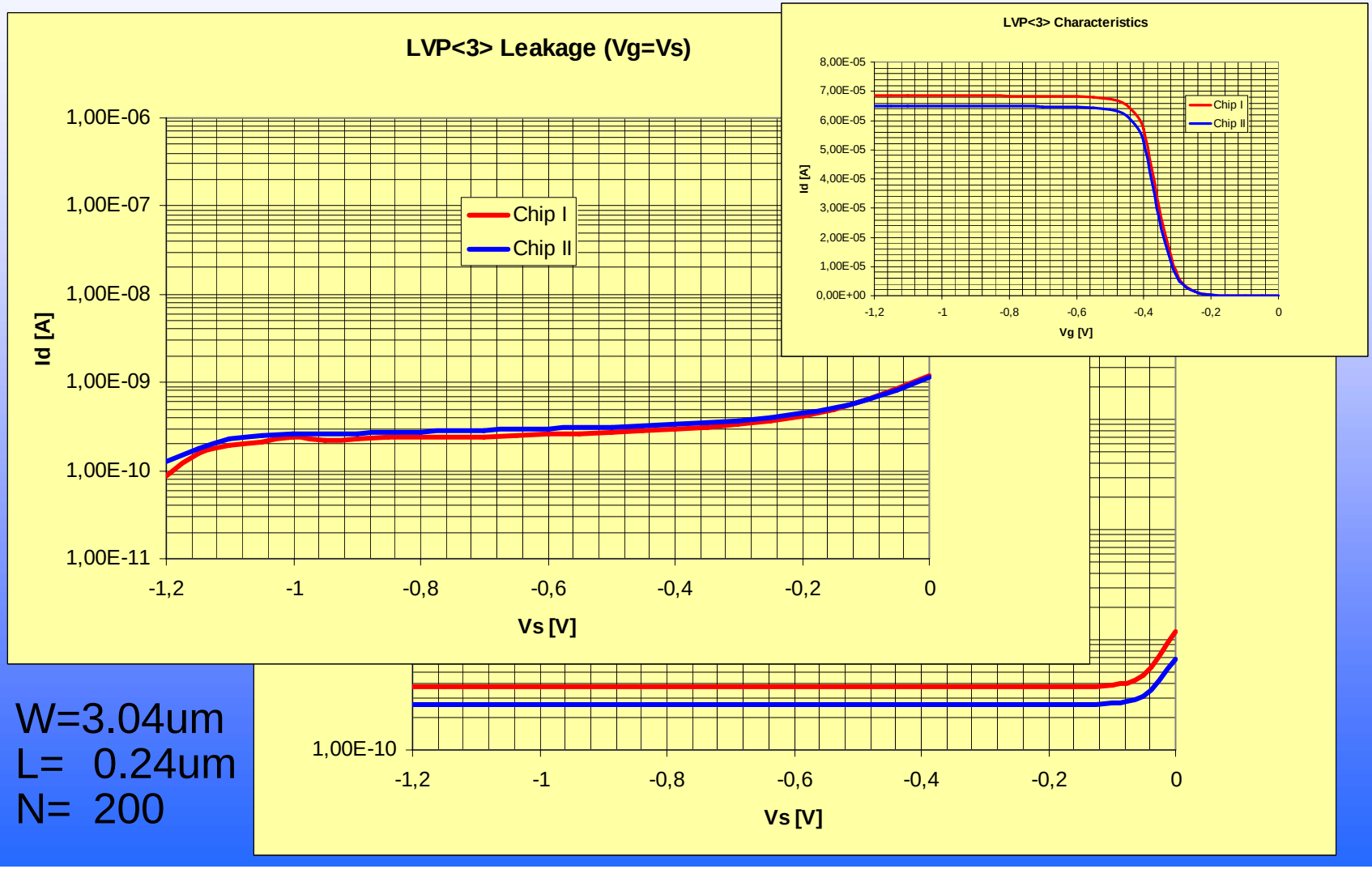


LPPMOS<2>



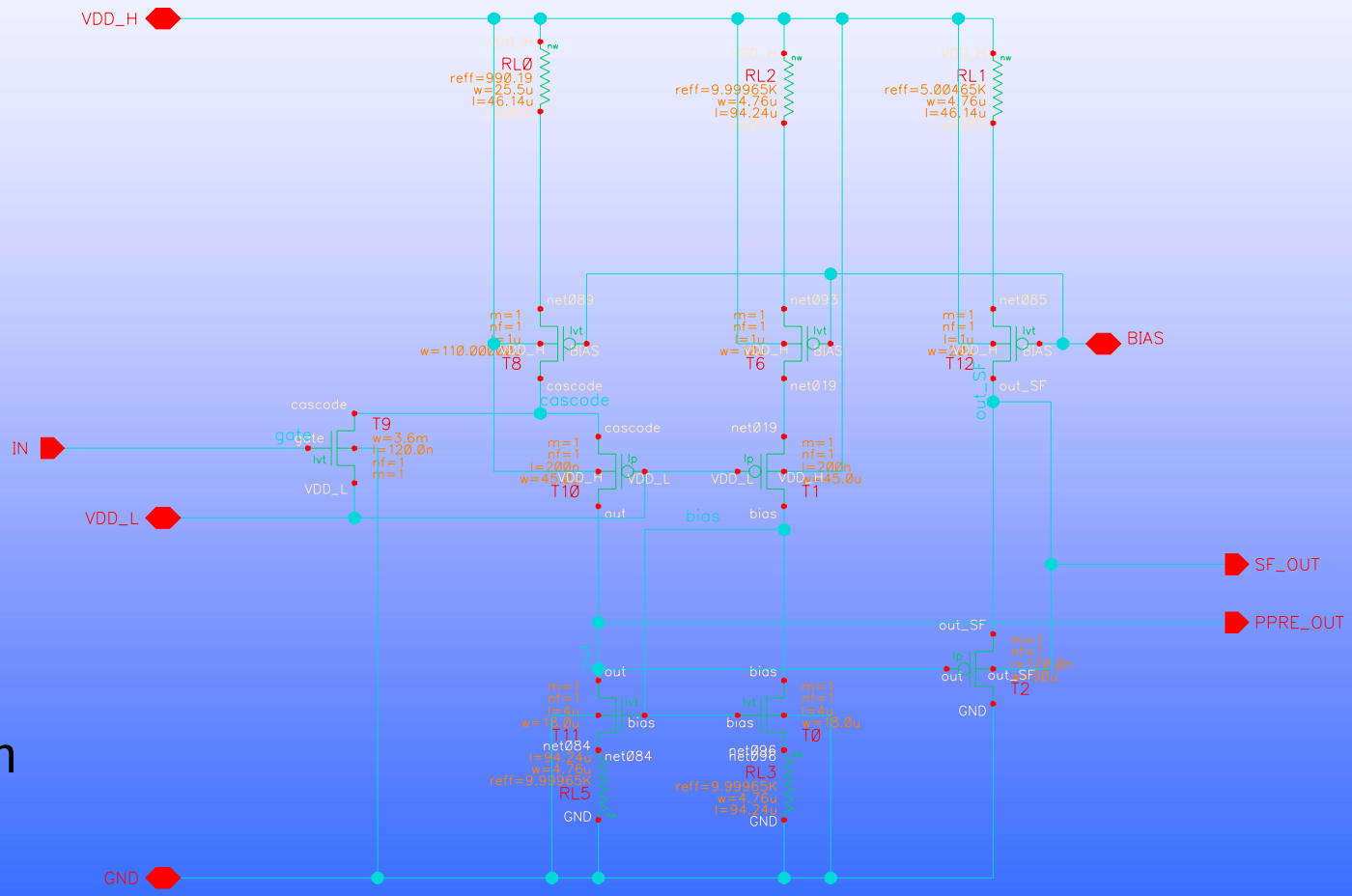
W=3.04um
L= 0.24um
N= 100

LPPMOS<3>



W=3.04um
L= 0.24um
N= 200

Folded Cascode Preamp



W= 3600um
L= 0.12um
NMOS
I= 50uA

Folded Cascode Preamp +Shaper?

Pulse processing		Noise $(\overline{ENC^2})$	
Sampling	Filter	parallel	series
single	none	$\frac{i_{\mathrm{np}}^2}{2} \cdot 0.535\, T_{\mathrm{meas}}$	∞
single	$CR-RC$	$\frac{i_{\mathrm{np}}^2}{2} \cdot 0.475\, T_{\mathrm{meas}}$	$\frac{e_{\mathrm{ns}}^2}{2} C_{\mathrm{p}} \cdot 7.18/T_{meas}$
double	none	$\frac{i_{\mathrm{np}}^2}{2} \cdot 0.750\, T_{\mathrm{meas}}$	$\frac{e_{\mathrm{ns}}^2}{2} C_{\mathrm{p}} \cdot 2.54/T_{meas}$
double	$CR-RC$	$\frac{i_{\mathrm{np}}^2}{2} \cdot 0.238\, T_{\mathrm{meas}}$	$\frac{e_{\mathrm{ns}}^2}{2} C_{\mathrm{p}} \cdot 15.2/T_{\mathrm{meas}}$
quad	none	$\frac{i_{\mathrm{np}}^2}{2} \cdot 0.731\, T_{\mathrm{meas}}$	$\frac{e_{\mathrm{ns}}^2}{2} C_{\mathrm{p}} \cdot 2.68/T_{\mathrm{meas}}$
deconvolution		$\frac{i_{\mathrm{np}}^2}{2} \cdot 0.786\, T_{\mathrm{meas}}$	$\frac{e_{\mathrm{ns}}^2}{2} C_{\mathrm{p}} \cdot 1.80/T_{\mathrm{meas}}$

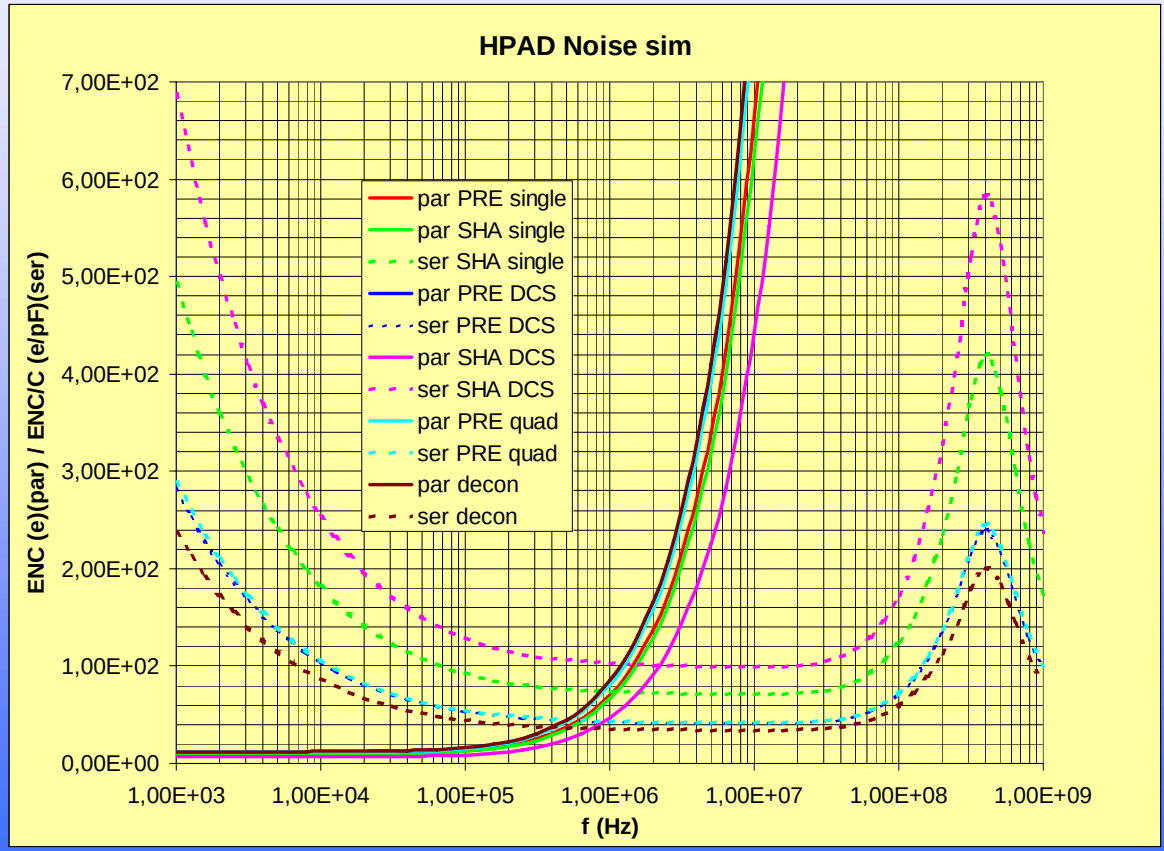
W. Fallot-Burghardt: *A CMOS Mixed-Signal Readout Chip for the Microstrip Detectors of HERA-B*

DCS+CR-RC:

- Shaper will suppress transients from gain switching
- Shaped pulse after the peak (2nd sample) is not evaluated

-> Reset of shaper?

Folded Cascode Preamp +Shaper?



Conclusions

Measurements on "HPAD 0.1"

- Surprises, but
- No conclusions so far, since
  - Results are not (yet) consistent
  - No irradiation data

Work in Progress!

Preamplifier

- Simulations look promising, but
  - No Shaper design yet
  - Ideas for implementation of gain switching exist
  - No simulation of preamp, shaper & gainswitching yet