

# Feedback from the cmrf8sf ASIC Designers Fest

DESY  
June 9<sup>th</sup>-10<sup>th</sup> 2008

# Aims & Goals

Avoid redundant efforts

“REPITA NON PLACENT” or

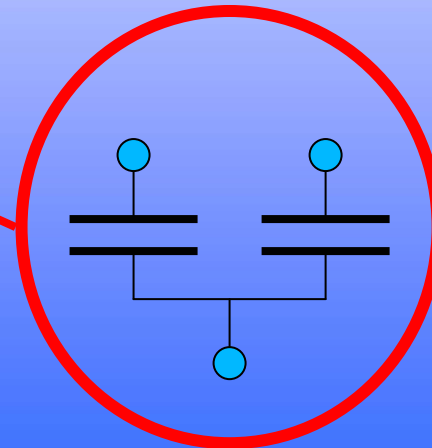
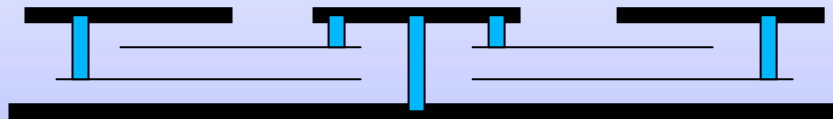
“Don't re-invent the wheel”

- By sharing the results of distributed drudgework
  - Library development
  - LVS deck generation
  - Checking procedures
- By efficient communication of
  - bugs and problems and the related
  - workarounds and fixes

# Bug in Calibre LVS

- (Dual-)MIMCAPS with a common LY electrode are not extracted

E1  
Qy  
Hy  
Ly



# Bug in DIVA & Assura LVS

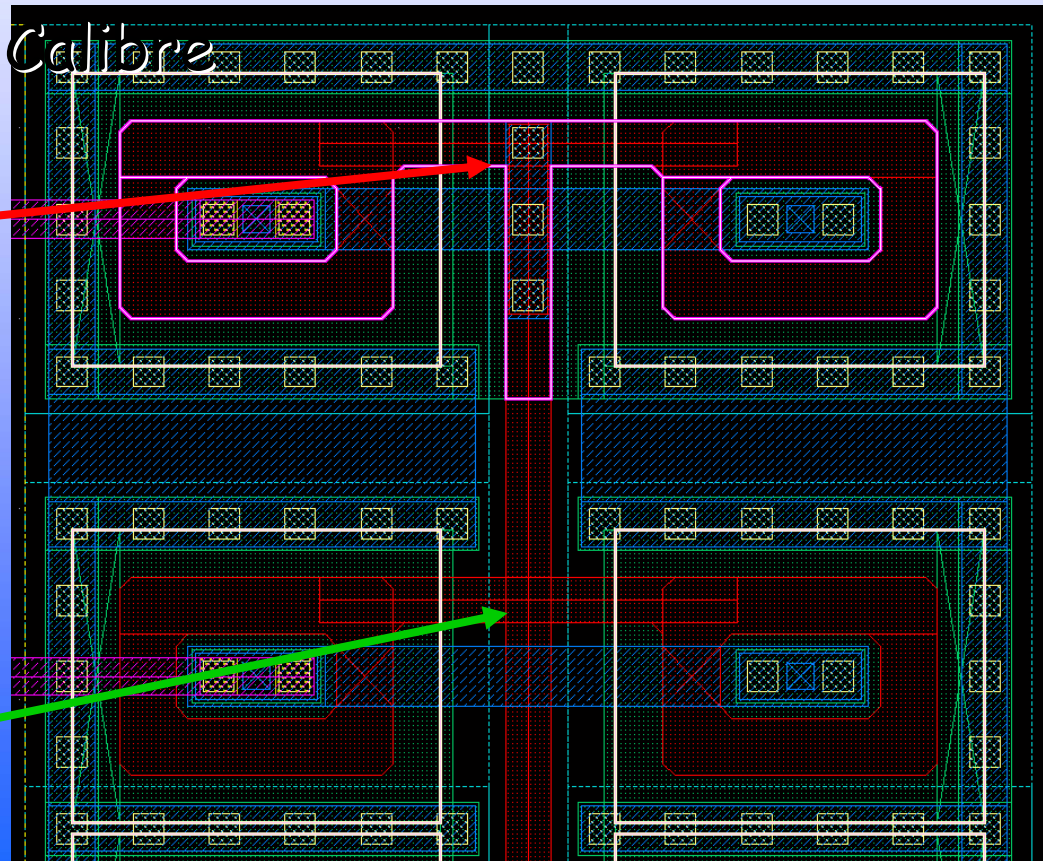
- ELTs connected by PC over RX are not recognized
- Not checked with Calibre



if filled with RX



if not filled with RX



# Rules & Libraries

- Extraction rules for enclosed transistors
- Enclosed transistor library
- Pads & I/Os
- Digital std. Cells
- Other common cells

# Extraction & LVS of enclosed transistors

- DIVA ELT extraction rules from RAL/CERN exist for IBM cmos6sf
  - Relied on additional layers
- Assura ELT LVS rules exist in HD/MA (Group of P. Fischer) for UMC 180nm technology
  - Further information on that required
- Calibre ELT LVS rules exist for IBM cmos6sf
- **Currently no rules available for CMRF8SF**

# Enclosed transistor library

- Includes all basic FETs:
  - lvtmfet
  - nfet
  - lpmfet
  - dgmfet
  - zvtmfet
  - zvtmgmfet
  - lvtpfet
  - pfet
  - lppfet
  - dgpfet

Exists, but

Optional contacts desirable

# ELT pcell example

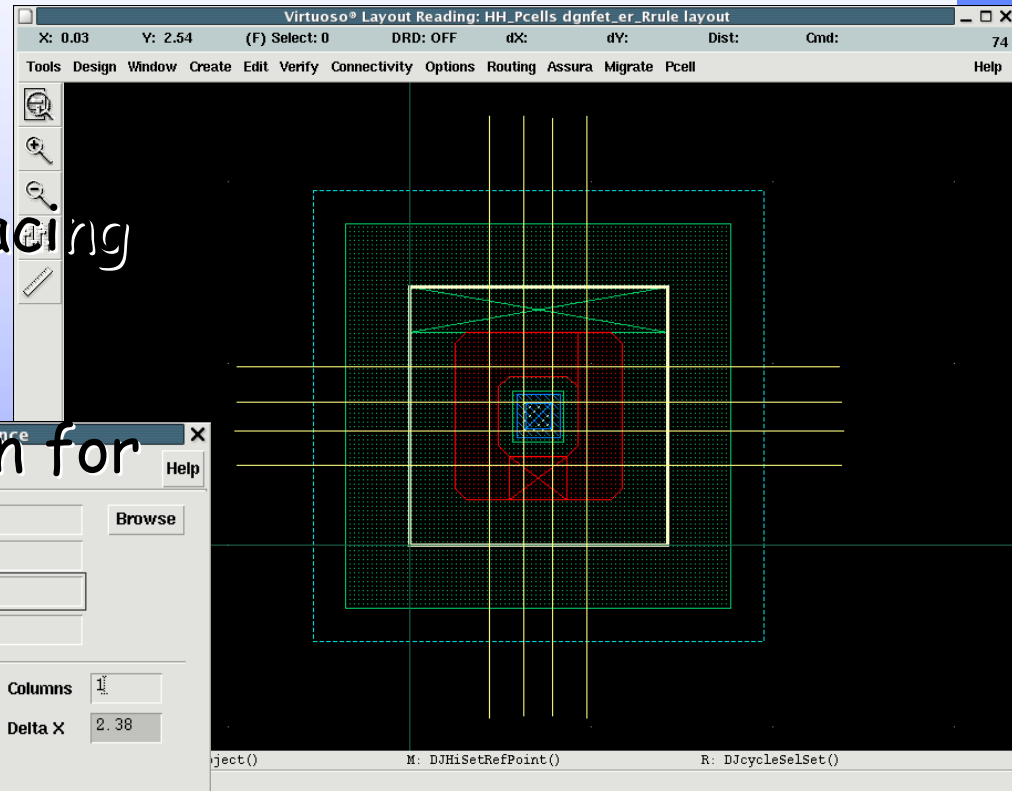
Ultra-pcell selection of

- RRULE or GRLOGIC spacing
- $V_{th}$ -selection
- Simple callback function for

$$W_{tot} = 2W_1 + 2W_2 + 2L$$

Create Instance dialog box showing configuration for a pcell:

- Library: HH\_pcells
- View: layout
- Names: pfet\_enci
- Mosaic: Rows: 1, Columns: 1, Delta Y: 2.38, Delta X: 2.38
- Magnification: 1
- Options: Rotate, Sideways, Upside Down
- Rule:  GRLOGIC  Rrule
- Vt:  lp  norm  lvt
- W1: 0.44
- W2: 0.44
- L: 0.12
- Wtot: 2.26





# Do we need a library with radiation hard logic gates?

- Radiation hardness
  - HPAD:
    - 1GGy (100Grad) @ sensor
    - 80% efficient
    - 20MGy @ ASIC
- Leakage currents
  - Driving strength
  - Timing
  - Power consumption
- **YES!**

# Common analog cells

- Comparator
- PP-buffer
- ZVT-buffer
- DACs
- Quasi-analog cells
  - Level shifter 1.2V-2.5V
  - Delay element (400ns, I<sup>2</sup>C)
  - OD-I<sup>2</sup>C I/O pads
  - LVDS I/O

# Conclusions

## What-Who-When

|                                       |             |          |
|---------------------------------------|-------------|----------|
| • CMRF8SF-Wiki                        | HPAD (M.K)  | July 08  |
| • DRC-Procedure                       | HPAD (M.K)  | July 08  |
| • LVS-Procedure                       | HPAD (M.K)  | July 08  |
| • ELT-Extraction (Assura)             | LPD (F.K.)  | end 08   |
| • ELT Pcells with contacts            | HPAD (U.T.) | Q4/08    |
| • ELT Std. cell lib & synthesis files | LPD (F.K.)  | end 08   |
| • Common analog cells                 |             |          |
| • Pads                                | HPAD (B.S.) | Sept. 08 |
| • LVDS                                | HPAD (R.M.) | end 08   |
| • Level Shifter & Open Drain I/O      | HPAD (U.T)  | end 08   |
| • Delay (400ns, I <sup>2</sup> C)     | HPAD (U.T)  | end 08   |

Follow-Up tentatively scheduled for 6.-7. November at MPI Munich