Interface electronics

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- Links to backend/control
  implications to mechanical design,
  to effort in FPGA's
- specifications of signals at interfaces and connectors
  possible mechanical arrangements
- Communication to control-system
- ADC pre-checks
- time line

Common projects

Most important changes:

- backend and control systems are
  "Common projects"
  for XFEL detectors.

Consequences for HPAD

- will result in similar systems
- some tasks less in HPAD .... also less freedom
- Process ongoing to get
  specifications/border definitions ongoing.

Links to backend/control

Our data rate to backend: 2.1Gbit/s

400 frames/train, 10trains/sec, 16bit/pixel, 32modules/1Mpixel

+ slow

+ flags

+ checks

For us multiple 1G-link in one bundle is sufficient, up to date technology in n years?

Backend prefers 10G-Ethernet 10Gbit/s/link

less links, less time-scheduling, future-technology ?!?!

Backend links low number of links 10, for sure≤16 links

we have 32 modules !!!!

Can AP-HPAD can combine two modules to one link ?

Also PCB designs likes much more 10cm width

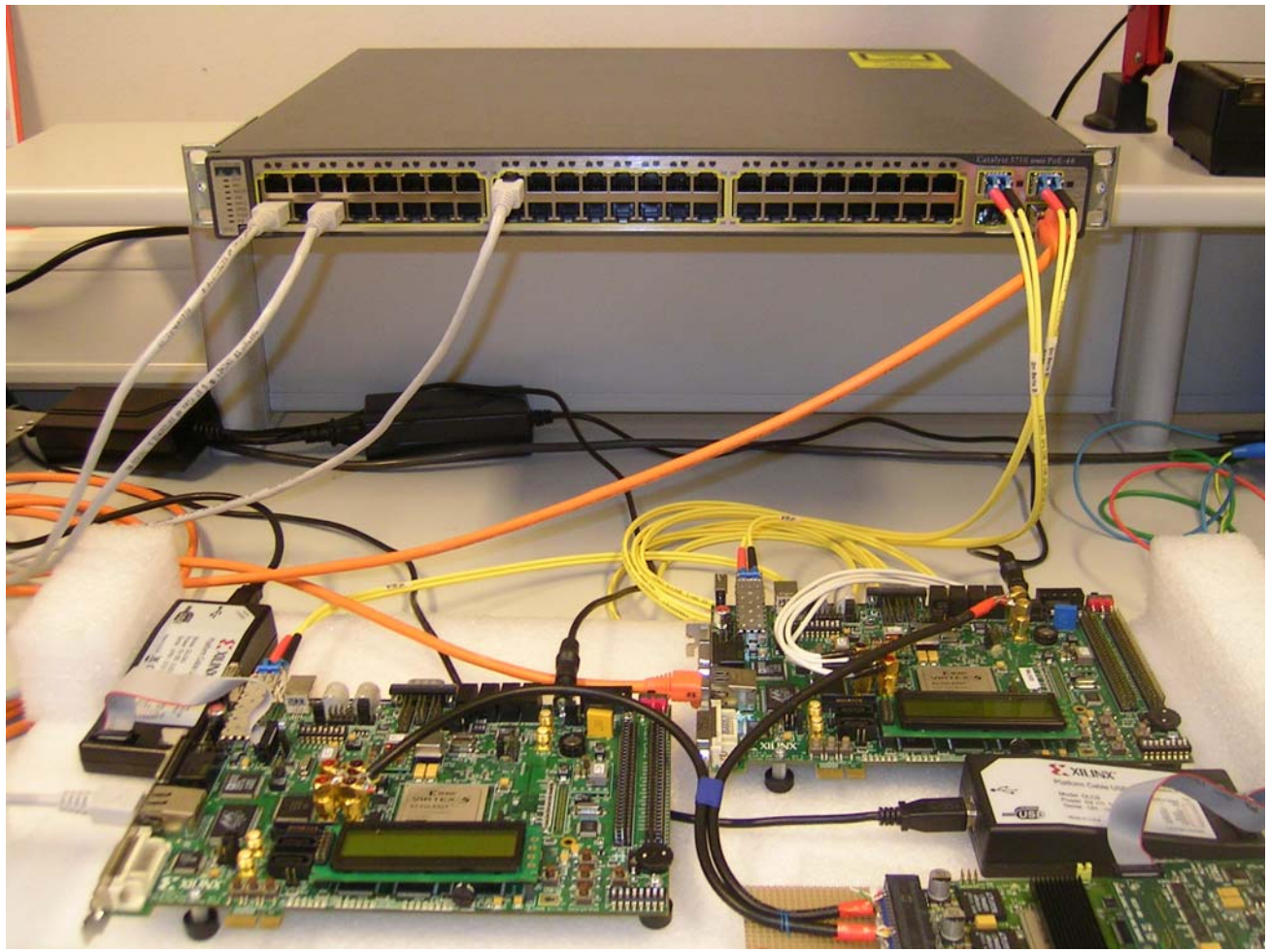
Larger FPGA's , easier for analog+control

Links to backend: Tests

Test based on commercial evaluation boards Virtex5,
+ switch + PC

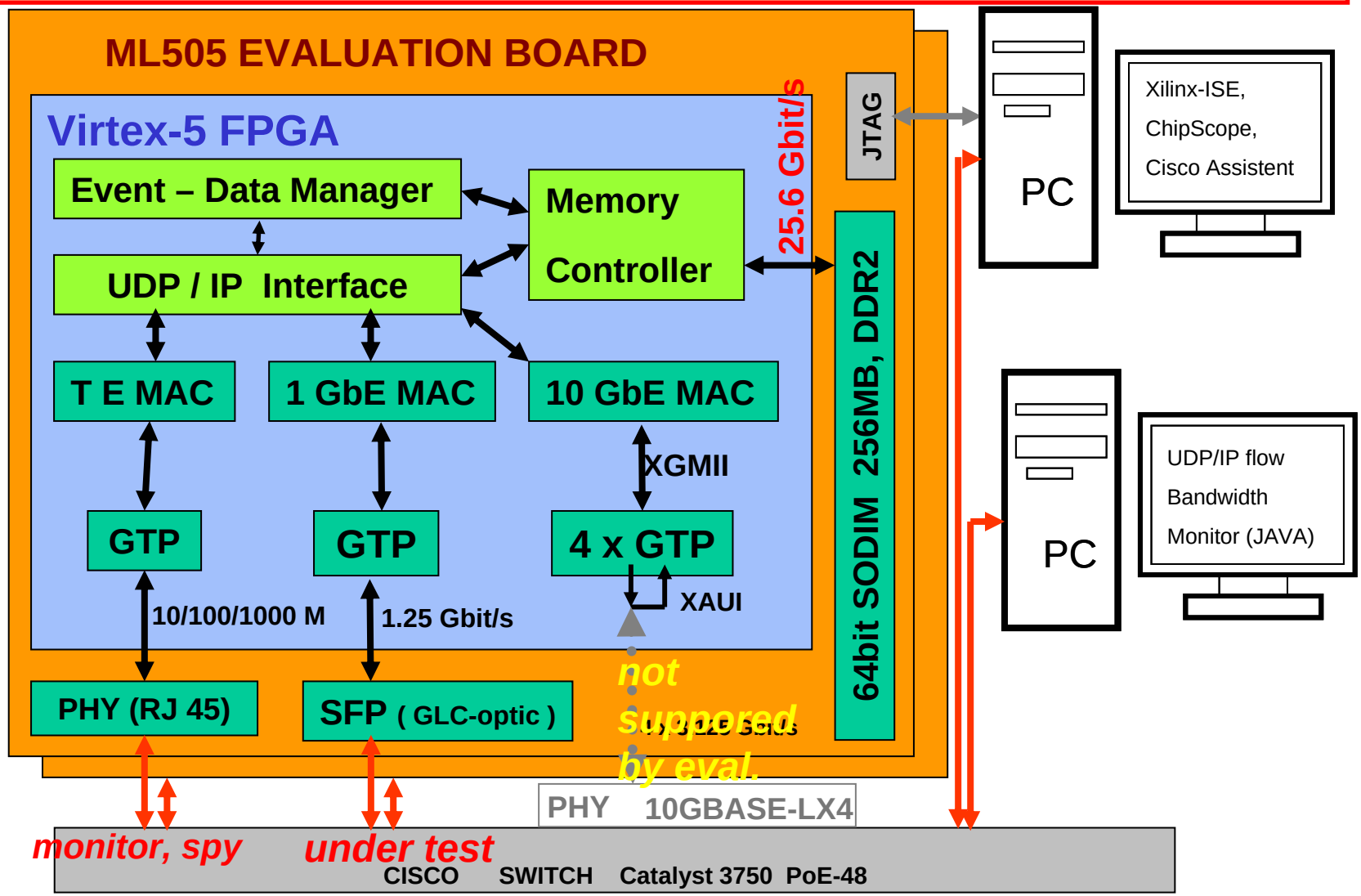
Firmware for
- 1GbE/UDP,

- 10GbE:
 * internal tests
 * Boards etc.
 ordered

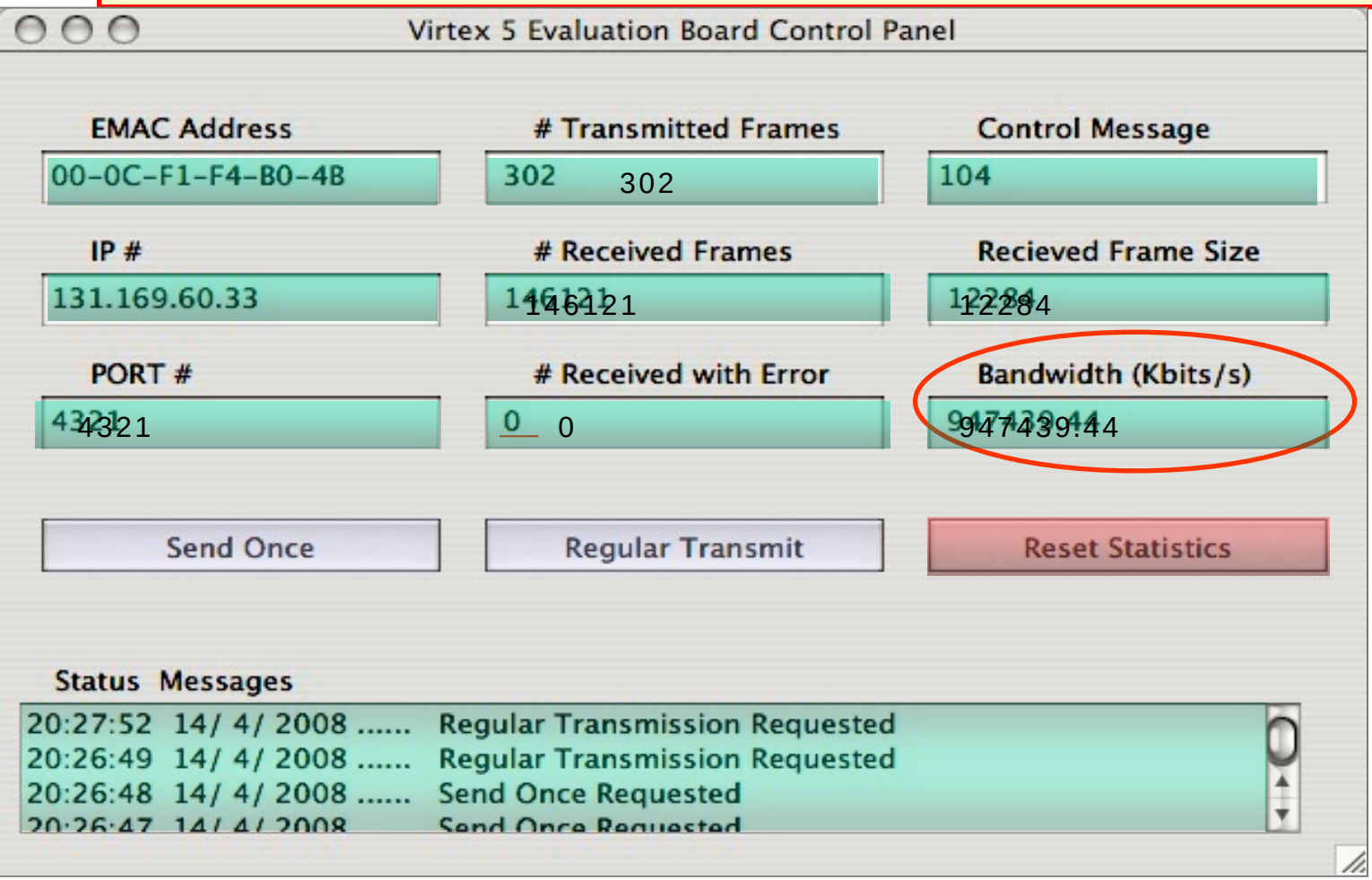


data rates, VHDL coding

I.Cheviakov



data rates, results



94% efficiency

Planning with ..... is on the safe side from viewpoint of FPGA

80% for pixel-data

+10% for monitoring, checksums, train-/frame-number

data rates, results

	Used XILINX XC5VLX30T		Only complied for larger XC5VLX50T	
	4x1 Gbit/s	10 Gbit/s	4x1 Gbit/s	10 Gbit/s
Slice Registers	33%	36%	22%	24%
Block RAM/FIFO	52%	58%	31%	35%
GTP_DUALs	75%	75%	50%	50%
Bonded IO Bs	56%	56%	42%	42%

⇒ both options looks promising,

fits well into a XILINX

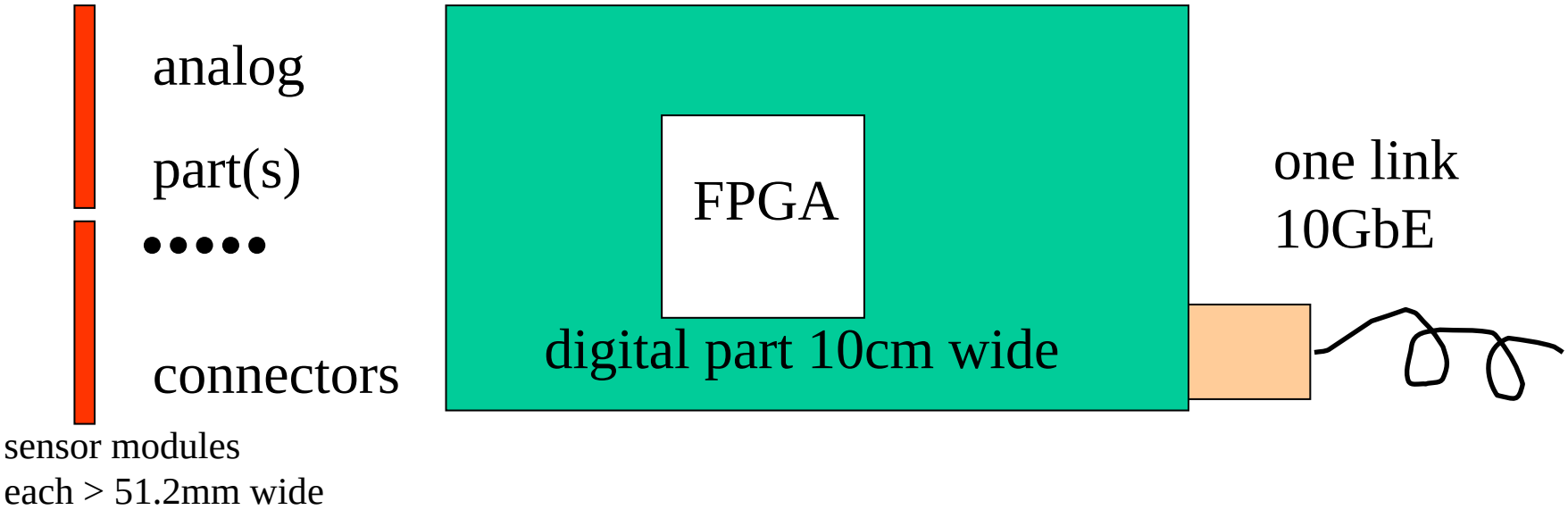
high efficiency for payload on the links

RAM access will be increase in design by wider address bus/two modules

10G-Ethernet only internally tested (limited by evaluation)

Space/circuit requirement under investigation by P.Vetrov

digital part: preferred design

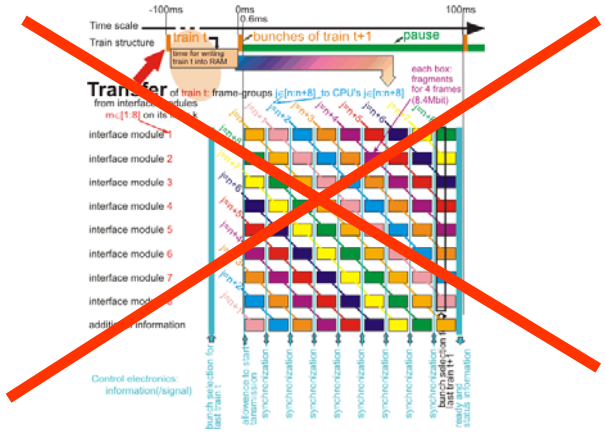


By that, AP-HPAD gets

16 output/1M with 10GbE
with 50% payload
Backend is investigating, that 16 links are OK.

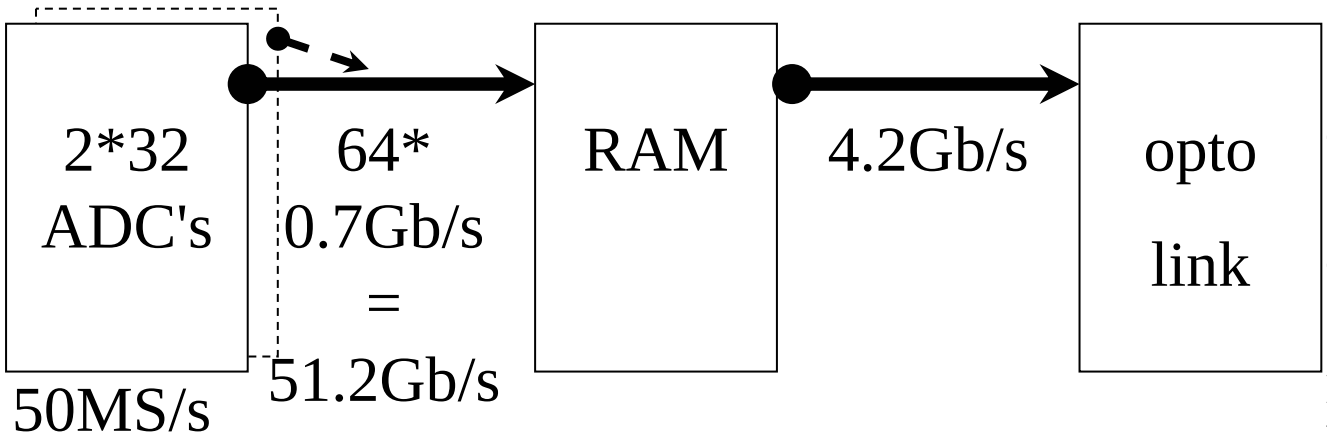
Alternatively: two digital parts with intercommunication,
but FPGA size limited. "more crasy mechanics"

Moved from AP-HPAD to Common



- No more HPAD:
  data sorting to groups of frames
  by time scheduled data transfers

- Left is still the algorithm for
  ADC to RAM and delayed read, reduce rate and cables!



protocol

- company independent
  XILINX, ALTERA,...
- platform independent
  FPGA, CPU

Keep useful at other laboratories

Signals at Board/Board connectors

Start point to be discussed

Input of Interface from Sensor side (=8 ASIC's)

32	pairs with shield		for analog from ASIC
8	pairs	100MHz	for gain of cell
3	pairs		for ASIC readout
		50MHz	Readout CLK, pixel increment cell increment
4	pairs	5MHz	for signal to Cap-cells write-CLK, read/write, fast-reject, calib
8	pin or multiple		Power 8 times 2? full time?
1	pin		Power ON/Standby (train)
1	pin, but isolated		HV - What voltage/polarity?
few	pins		GND, also in the shields.
2	pins		Slow control - I2C like

Count is around 120 pins plus shields or in between GND's

Can gains per ASIC be coded to 1 pair? 32Mb/s/ASIC or all parallel?

Signals at Board/Board connectors

analog to digital part:

32	pairs with shield	700Mb/s	for ADC-out
8	pairs with shield	700Mb/s	for ADC-sync
8	pairs	50MHz	for gains
3		50MHz	Readout CLK, pixel increment cell increment
5	pairs	5MHz	for signal to Cap-cells write-CLK, read/write, fast-reject calib, 5MHz
4	pins		Slow control - I2C like

Count is around 120 pins plus shields or in between GND's

And space for bypass of cables from analog part to back-panel

Signals at Back-panel

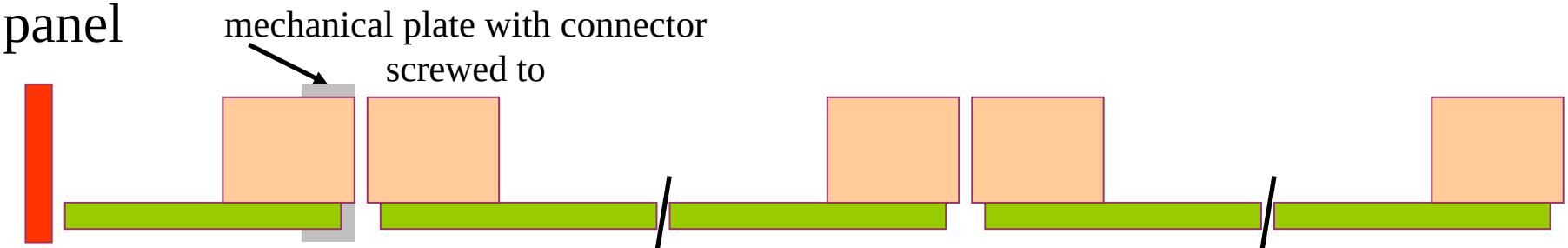
from analog/digital part:

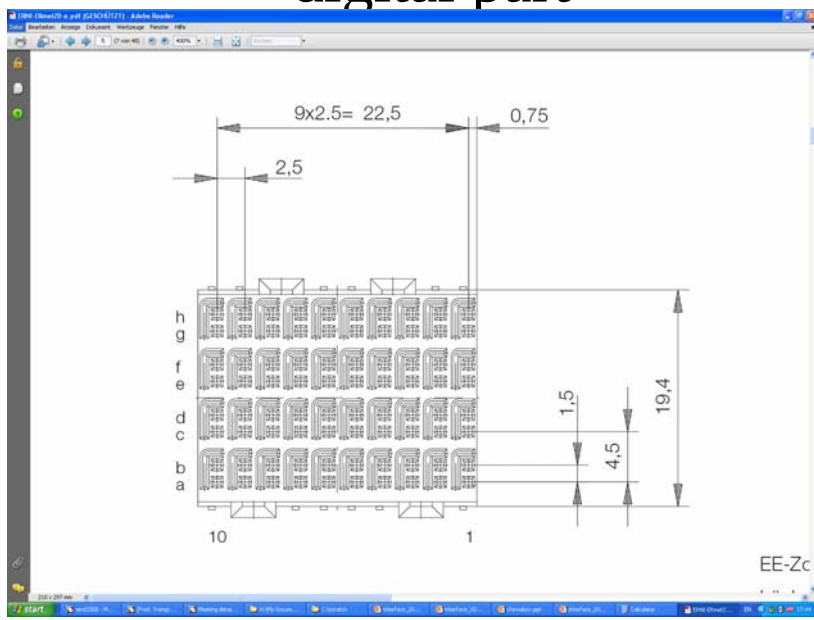
1	Opto SFP+		10GbE
6	pairs	5MHz	train_start, bunch_clk, 5MHz_clk
			fast_reject, calib, one spare
2	pairs	125MHz	Slow control
			via 100MbE/TCP-IP
.....	pins		remote firmware upgrades
1	shielded		HV for bias
....			Power for analog part+ASIC
....			Power for digital part

GND-point to PE is the detector head (ASIC/sensor/analog)

Mechanical design from electronic

Option: digital/analog part possible to be pulled out to the back panel



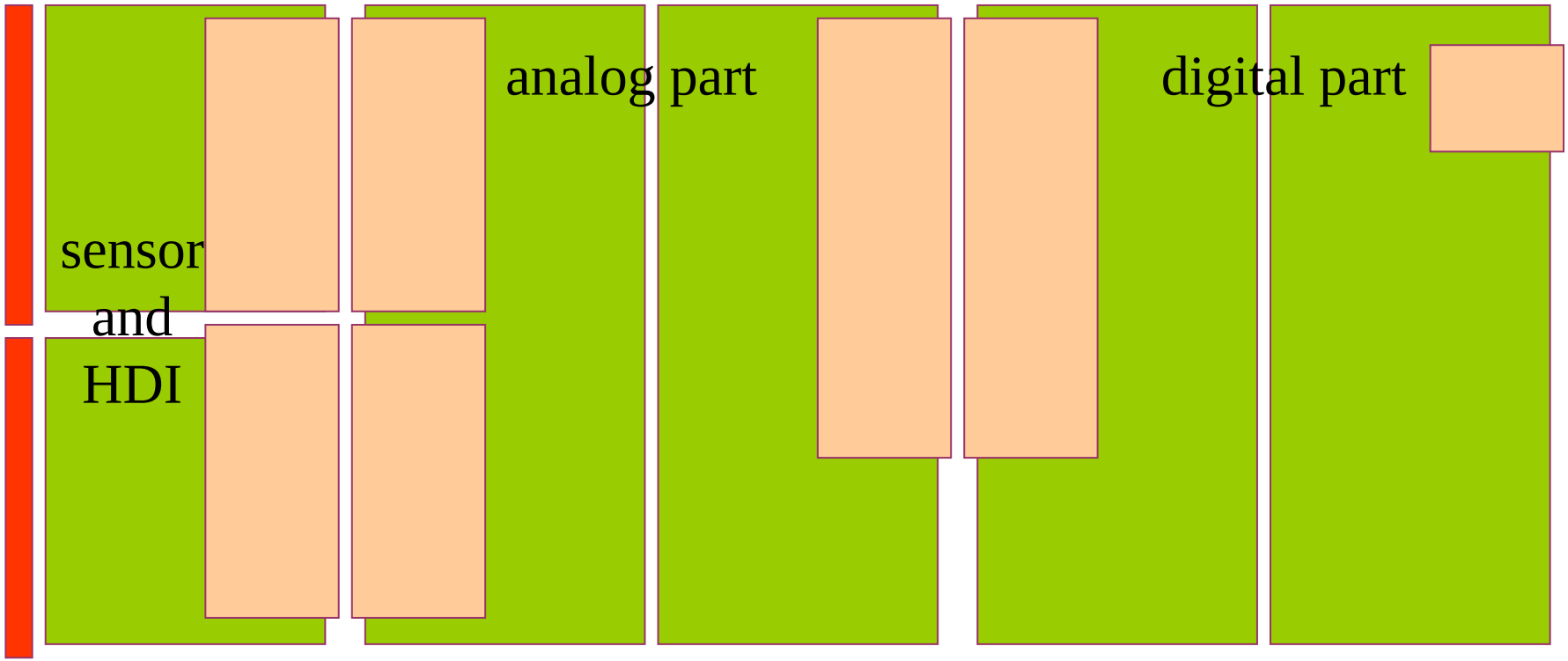


- Connectors with that density are available, but already tight, ERNI (ATCA,5Gbit/s)

- HV and power with other connectors, beside.

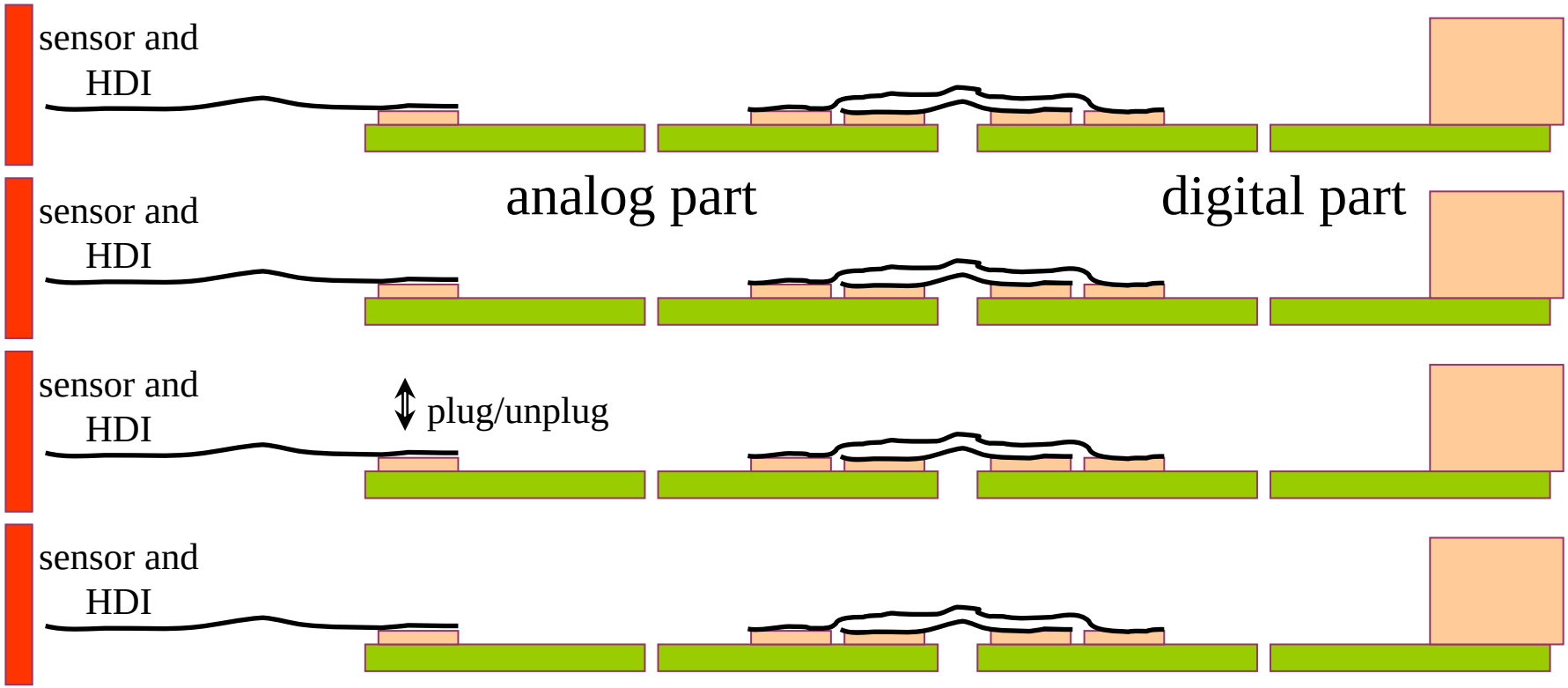
Connector for PCB to PCB

Option: digital part, analog part are possible to pull out to the back panel



Connector for PCB to PCB

Option: every thing to the front
or disassemble more to get to inner region
has more freedom for the connector choise.



Connectivity to control system

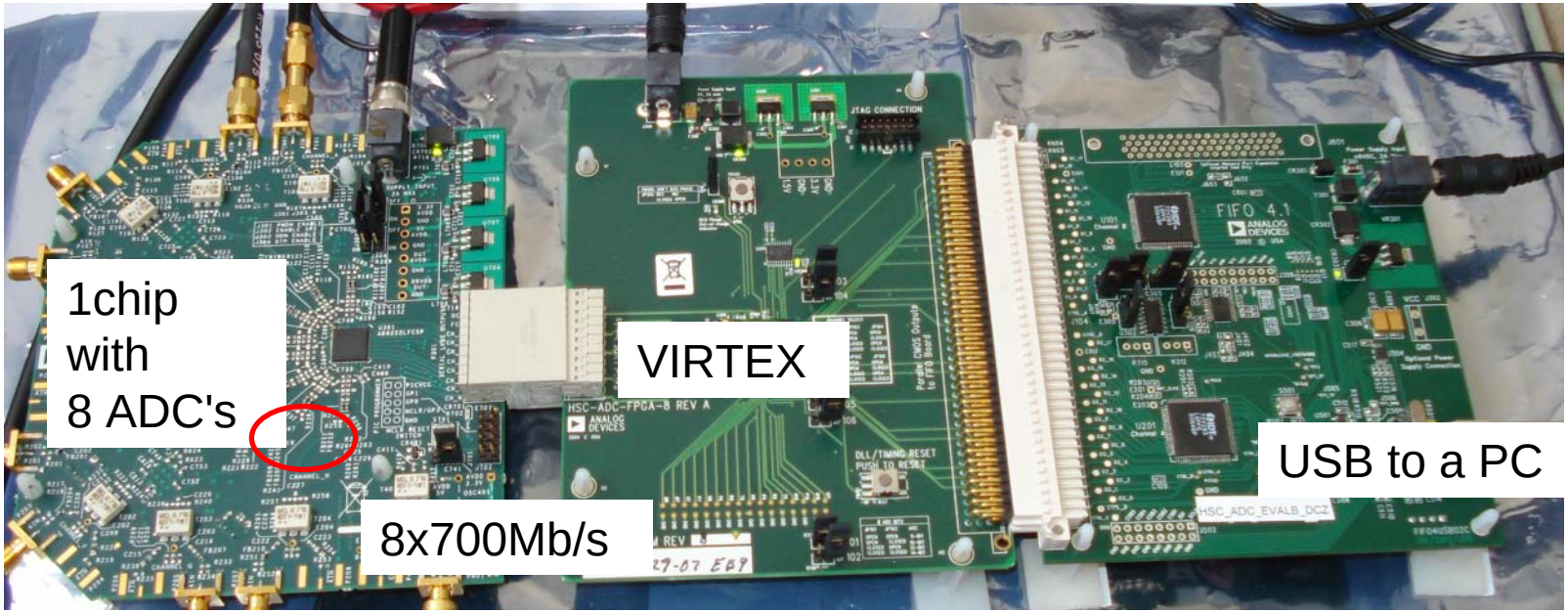
- Boot and monitor data (per train) 100MbE TCP/IP
  protocol is supported by uC and FPGA
- Clocks for train synchronization 5MHz
- remote firmware upgrade
- Power
- HV

GND reference is the detector head:

- control must float per module
- drive copper based signals to GND returned from detector head
- all wire runs per detector module as nearby bundle
  EMI- (small L, transformers)

ADC to FPGA

H.Wentzlaff



System of evaluation boards: ADC...PC:

Boards ordered,... dig.part not OK.,
end back, will come back in July

Open VHDL code: Good for start up of final program

HPAD: 1FPGA for 4 of these ADC chips: 4 clocks, 32x700Mb/s

Could also be a base for easy evaluation of ASIC's???

Needed only first amplification stage and pattern-gererator

Interface-electronic ASIC'2009