Firmware Status, Basic concepts

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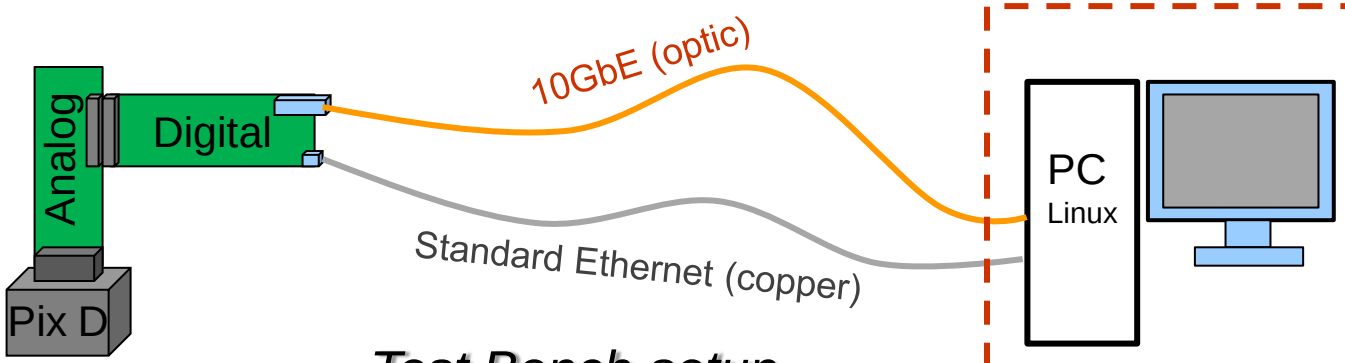
Outline

- *Basic Concepts & Features*
- *Local Test Bench setup*
- *Firmware structure*
- *Periphery steering*
- *Readout Scheme*
- *Gain data merging*
- *FW status*
- *HW status*

Firmware basic Concepts and Features

- *Real time steering of the AGIPD Periphery configuration*
- *ADC pix data to DDR2 bandwidth > 51 Gbit/s*
- *Scalable 10GbE channels*
- *BRAM ⇔ File interfaces including FE file system*
- *FPGA ⇔ uController & Standard Ethernet interfaces*
- *I2C, SPI supporting for Slow Control tasks*

Local DAQ Test Bench setup



Test Bench setup

Configuration , Monitoring (via standard Ethernet).

Pix Data through 10GbE

Files:
- *FPGA configuration*
- *AGIPD Periphery const.*

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Real time:
- *patterns: Bunch-Veto*
- *operation modes*
- *10GbE data monitoring*

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For Final System PC replaced by:

Train Builder <= 10GbE data

C&C System => Bunch pattern, Veto

Central SC , CDB => DAQ Configuration

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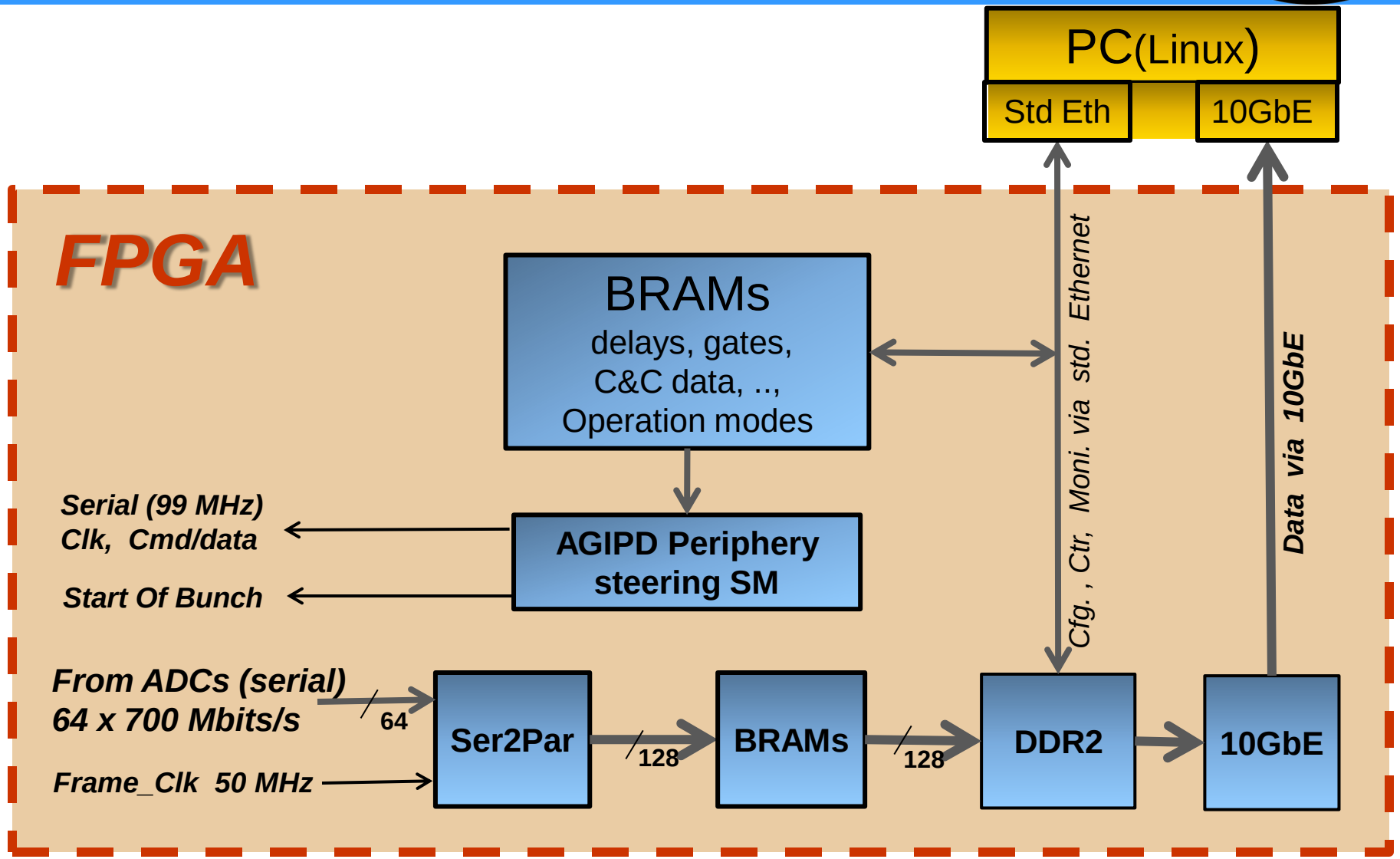
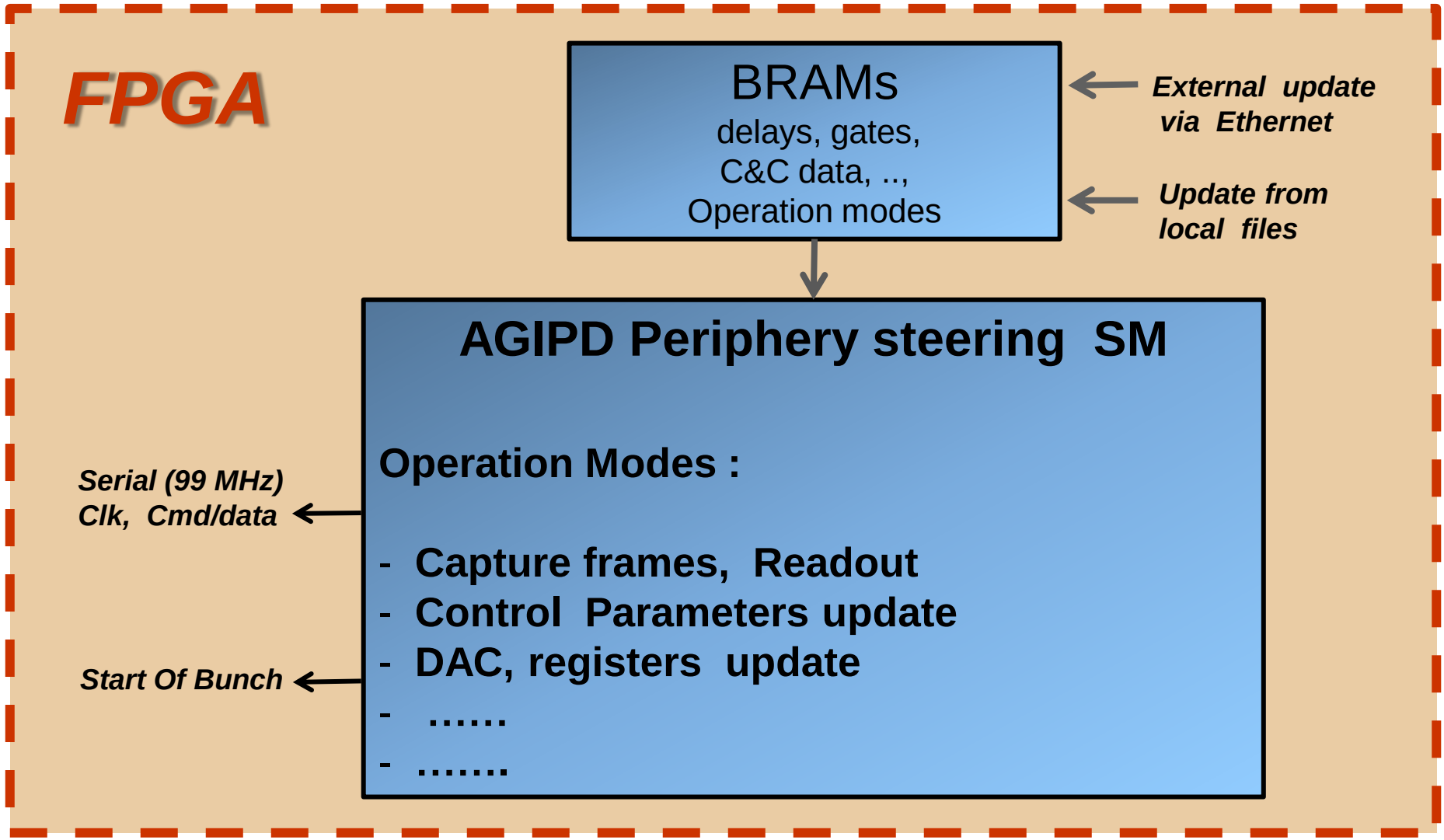
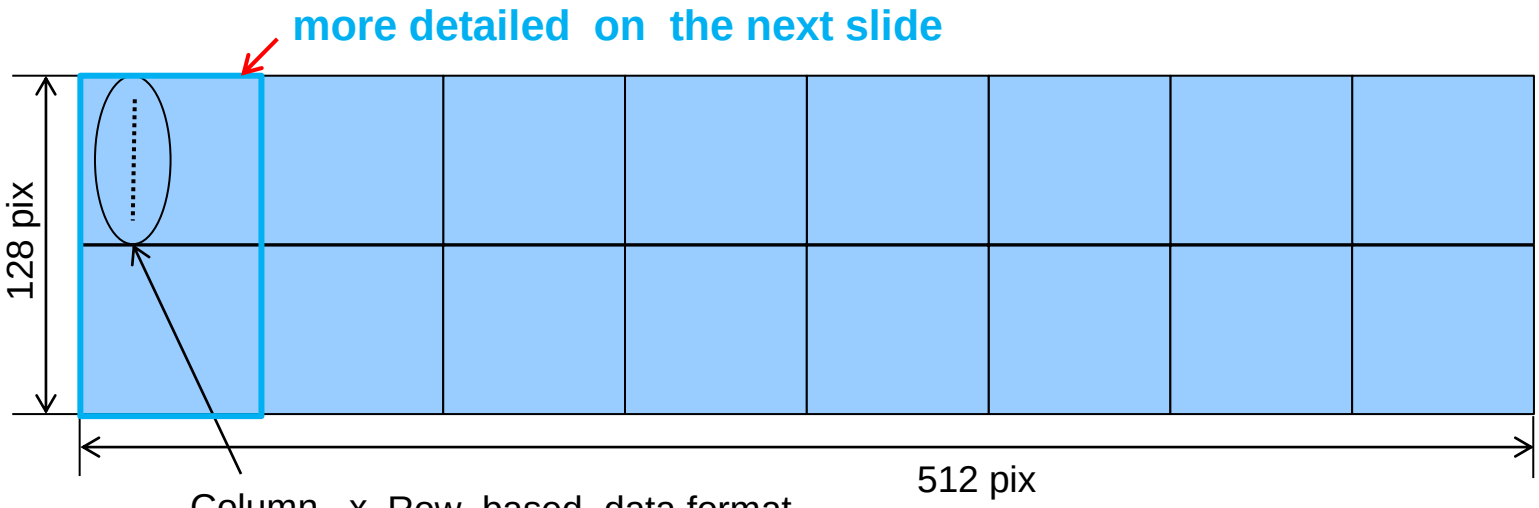
Firmware Structure (test bench)



AGIPD Periphery Steering Concept



Front End reordering the pix data (optional)



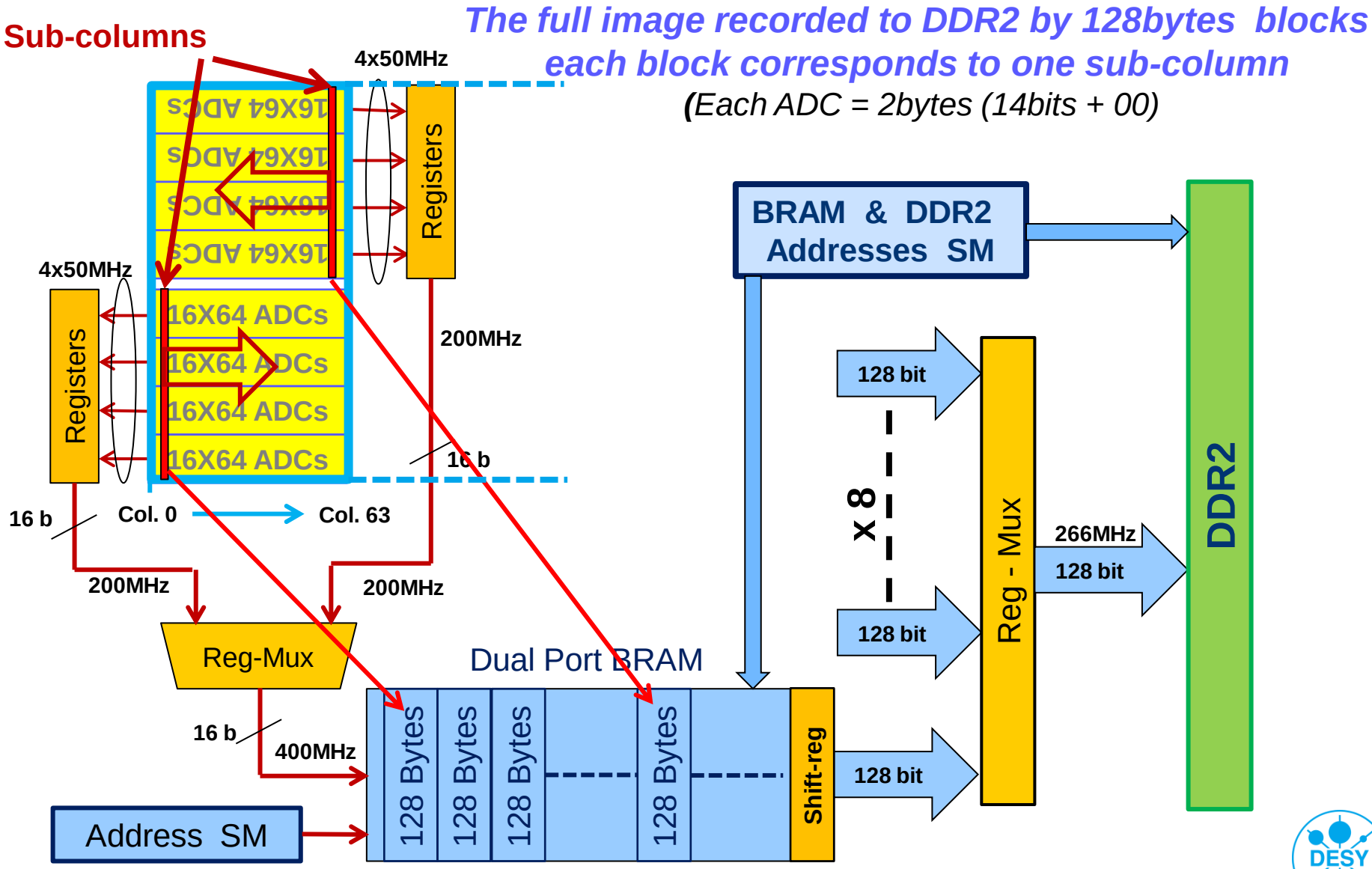
- These ADC values are placed in sequential addresses of BRAM to produce certain data blocks to be transferred then to DDR2 memory.

- The data blocks should have a sizes allowed an effective DDR2 access.

- A DDR2 address of each data block is assigned to corresponding position in the whole image data structure depending on row or column based format.

ADDERSS = row_Nr + 128 x column_Nr - column based
ADDRESS = column_Nr + 512x row_Nr - row based

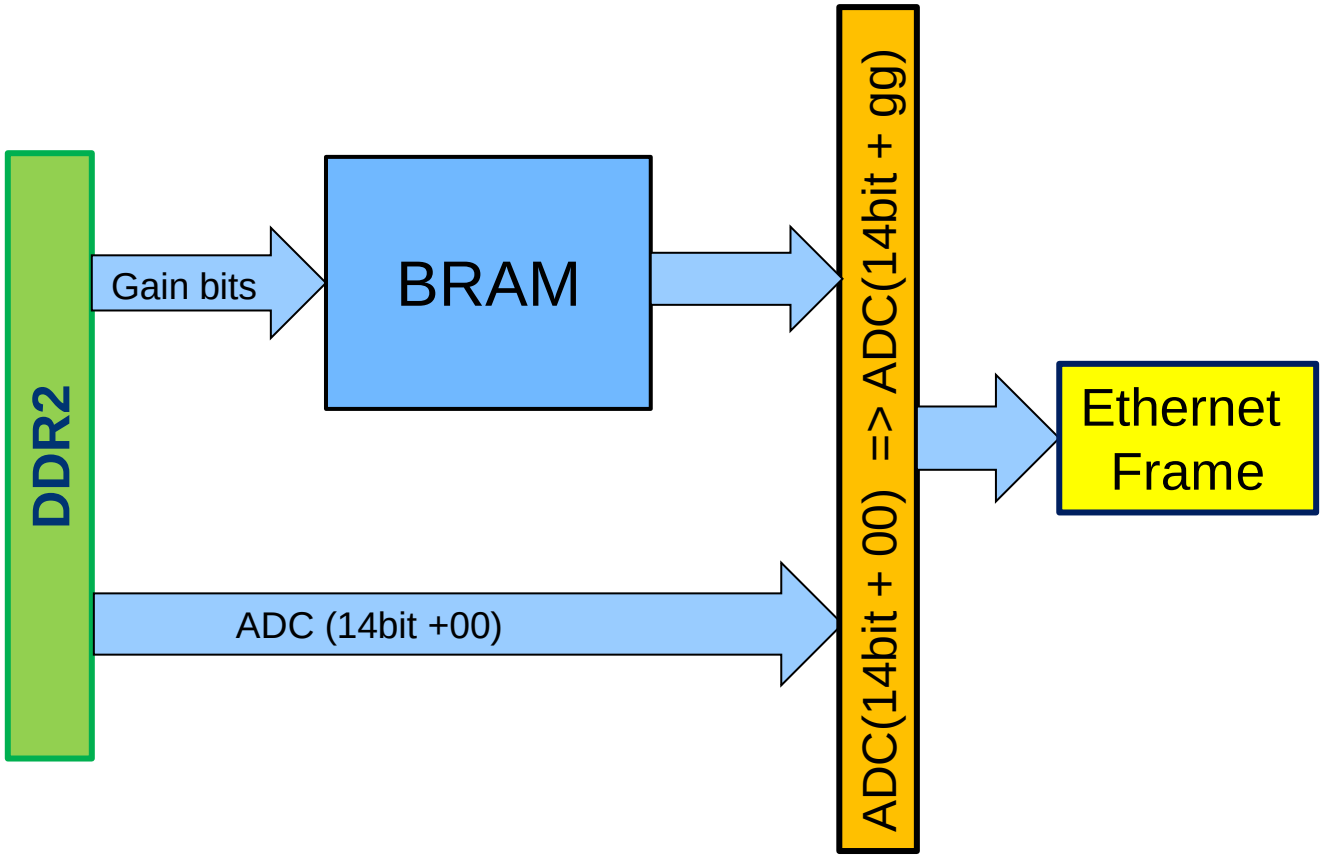
DDR2 Data Image-like Alignment Scheme (optional)



Gain Data Merging during Ethernet Framing

Scheme for reducing a number of DDR2 accesses

Storing corresponding part of gain bits into BRAM
to fast access during merging them into 16bit word



Firmware Status

Most of components have
EITHER the operational prototypes:

- ADC readout
- DDR2 data flows control

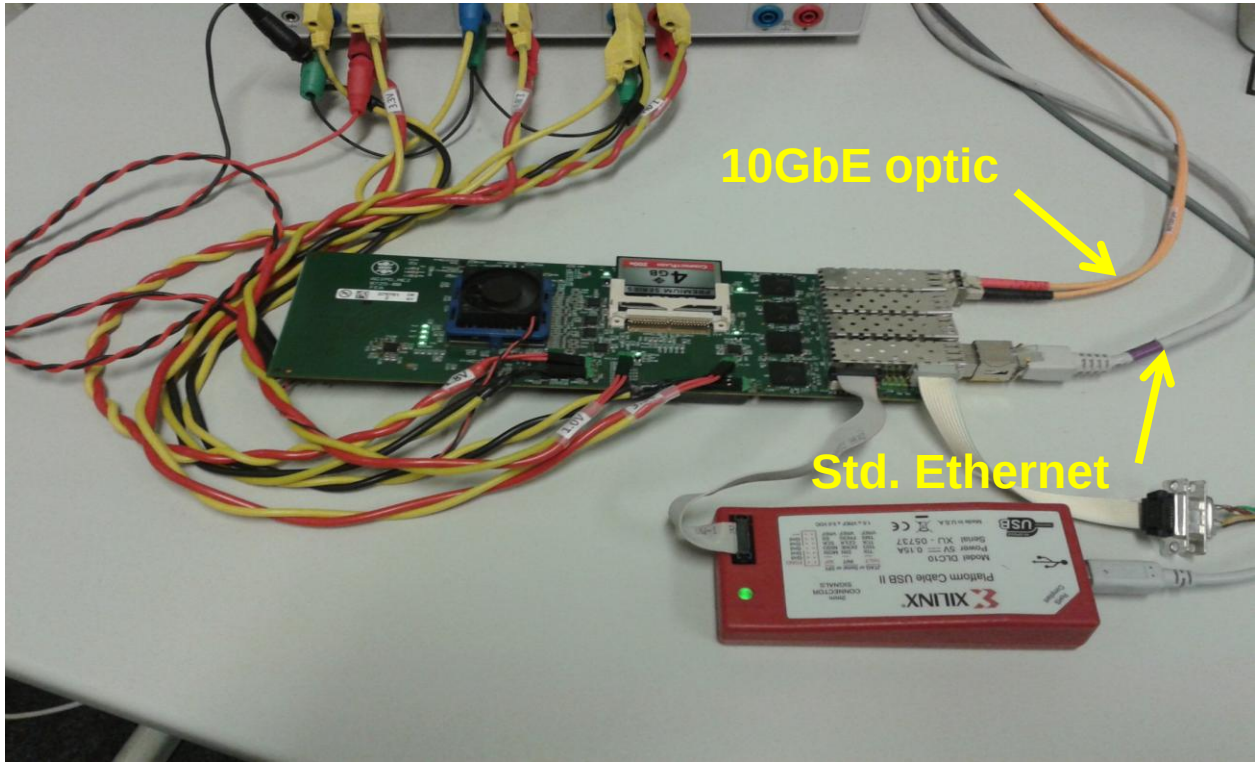
OR Completely tested in the final version
with full bandwidth operation:

- 4 x 10GbE + 2 x DDR2 modules => Bit Error < 10E-15 or less

Components in the development phase:

- AGIPD Periphery steering
- Data monitoring
- FPGA ⇔ FPGA fast communication
- Slow Control (based on I2C, SPI)
- FE File system (Flash memories <=> HD function)

FPGA Mezzanine Board



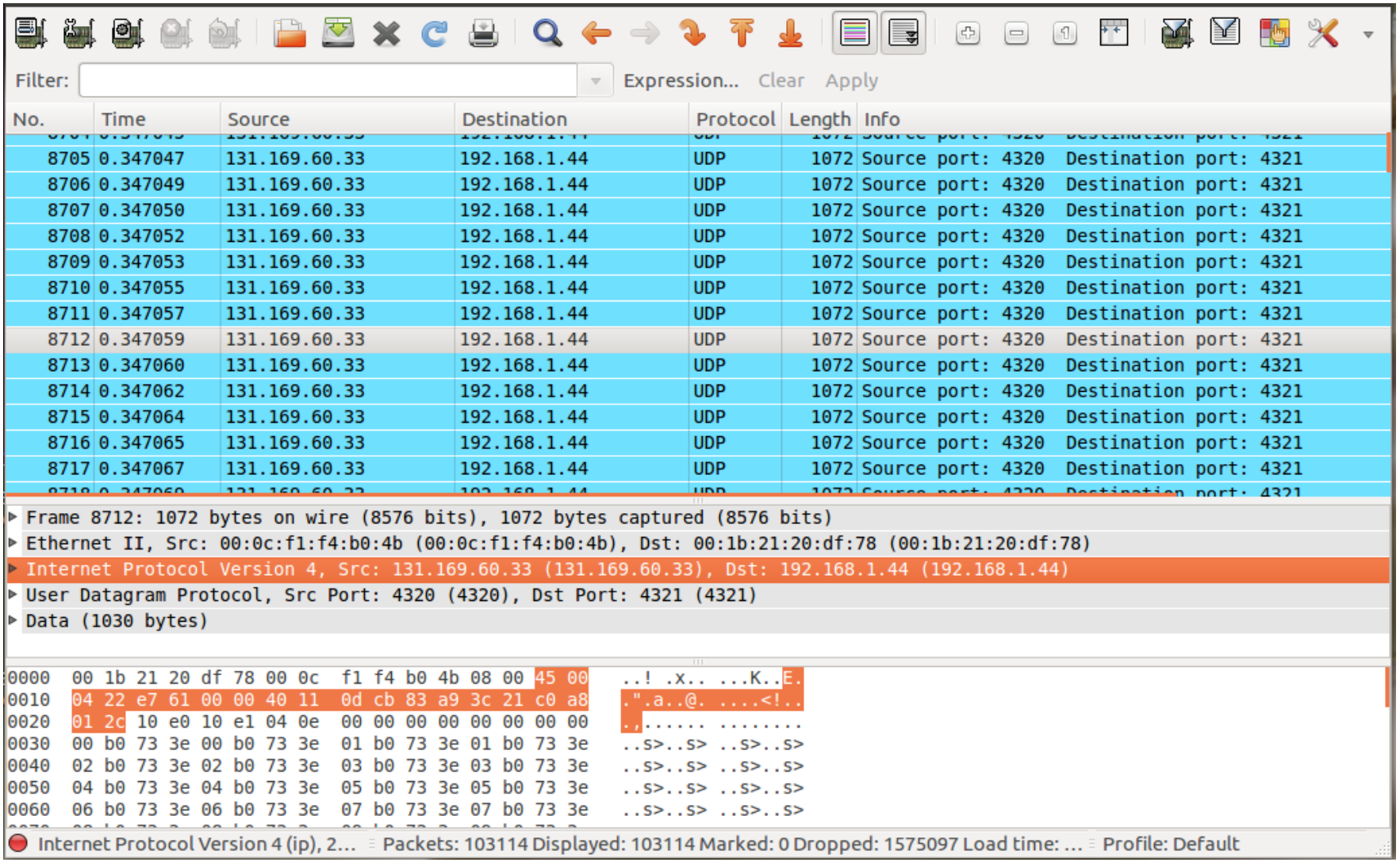
- The Carrier Board now under production phase

Outlook

- *Basic Firmware components related to FE => 10GbE data flow are available as working prototypes or already in it's final version.*

- *AGIPD Periphery Steering FW components are in development stage*

- *Complete Digital Boards setup hopefully will be available in May*


Filter:
Expression... Clear Apply
No. Time Source Destination Protocol Length Info
8705 0.347047 131.169.60.33 192.168.1.44 UDP 1072 Source port: 4320 Destination port: 4321
8706 0.347049 131.169.60.33 192.168.1.44 UDP 1072 Source port: 4320 Destination port: 4321
8707 0.347050 131.169.60.33 192.168.1.44 UDP 1072 Source port: 4320 Destination port: 4321
8708 0.347052 131.169.60.33 192.168.1.44 UDP 1072 Source port: 4320 Destination port: 4321
8709 0.347053 131.169.60.33 192.168.1.44 UDP 1072 Source port: 4320 Destination port: 4321
8710 0.347055 131.169.60.33 192.168.1.44 UDP 1072 Source port: 4320 Destination port: 4321
8711 0.347057 131.169.60.33 192.168.1.44 UDP 1072 Source port: 4320 Destination port: 4321
8712 0.347059 131.169.60.33 192.168.1.44 UDP 1072 Source port: 4320 Destination port: 4321
8713 0.347060 131.169.60.33 192.168.1.44 UDP 1072 Source port: 4320 Destination port: 4321
8714 0.347062 131.169.60.33 192.168.1.44 UDP 1072 Source port: 4320 Destination port: 4321
8715 0.347064 131.169.60.33 192.168.1.44 UDP 1072 Source port: 4320 Destination port: 4321
8716 0.347065 131.169.60.33 192.168.1.44 UDP 1072 Source port: 4320 Destination port: 4321
8717 0.347067 131.169.60.33 192.168.1.44 UDP 1072 Source port: 4320 Destination port: 4321
Frame 8712: 1072 bytes on wire (8576 bits), 1072 bytes captured (8576 bits)
Ethernet II, Src: 00:0c:f1:f4:b0:4b (00:0c:f1:f4:b0:4b), Dst: 00:1b:21:20:df:78 (00:1b:21:20:df:78)
Internet Protocol Version 4, Src: 131.169.60.33 (131.169.60.33), Dst: 192.168.1.44 (192.168.1.44)
User Datagram Protocol, Src Port: 4320 (4320), Dst Port: 4321 (4321)
Data (1030 bytes)
0000 00 1b 21 20 df 78 00 0c f1 f4 b0 4b 08 00 45 00 ..! .x.. ...K..E.
0010 04 22 e7 61 00 00 40 11 0d cb 83 a9 3c 21 c0 a8 ."a..@. ....<!..
0020 01 2c 10 e0 10 e1 04 0e 00 00 00 00 00 00 00 00 .,...... ....
0030 00 b0 73 3e 00 b0 73 3e 01 b0 73 3e 01 b0 73 3e ..s>..s> ..s>..s>
0040 02 b0 73 3e 02 b0 73 3e 03 b0 73 3e 03 b0 73 3e ..s>..s> ..s>..s>
0050 04 b0 73 3e 04 b0 73 3e 05 b0 73 3e 05 b0 73 3e ..s>..s> ..s>..s>
0060 06 b0 73 3e 06 b0 73 3e 07 b0 73 3e 07 b0 73 3e ..s>..s> ..s>..s>
Internet Protocol Version 4 (ip), 2... Packets: 103114 Displayed: 103114 Marked: 0 Dropped: 1575097 Load time: ... Profile: Default