# asic design

Presentations:

- Xintian: AGIPD04, improvements for column buffer
- Dominic: noise measurements (AGIPD02 03 04)
- Ulrich: changes in comand based interface

- discussion (chip design review, full chip submission, possible improvements)

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Chip design review:

Went through comments and formulated answers for things which are known, wait for final AGIPD04 results before we send final answers

Should send email now to let reviewers know where we are and when they can expect an answer

Need to irradiate AGIPD04 and measure noise, storage cells after Irradiation (not until end of APRIL)

Need to measure full chip readout (leakage of storage cells due to readout) also after irradiation

# asic design

Next chip submissions:

AGIPD04 seems to be a usable design → full submission possible

Risks:

- command based interface (very easy to get it wrong)
- possible improved CDS buffer with larger dynamic range
  shift voltage range from 0.5-1.1 to 0.65-1.3
  - lower on resistance
  - smaller voltage dependence (signal height) of capacitance → better linearity
- readout buffer in column instead of pixel (reduces power consumption, could reduce noise (heigher current possible)

Need MPW for testing and understanding of full chip (due to comand based interface not possible)

Need MPW for CDS buffer and column buffer

MPW for comand based interface desirable