



State of ASIC Design

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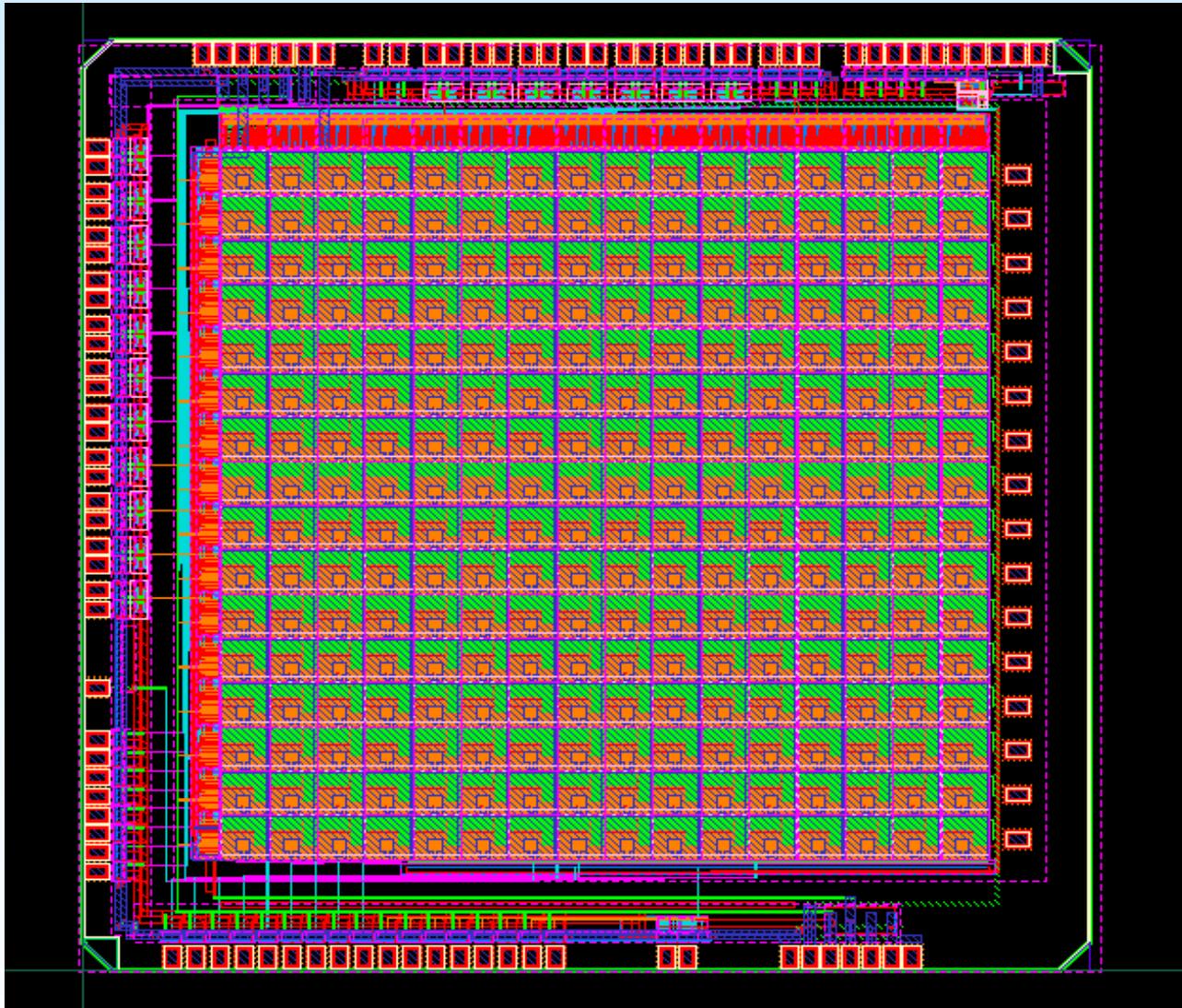
03.04.2012

AGIPD04 Prototype



- AGIPD04 was received in February and is being tested.
- The measurements so far looks quite promising. Dominic will give the details about the measurement results.

AGIPD04 Prototype



AGIPD04 Prototype



- 16 x 16 pixel array with 4 pixel variations.
- 352 memory cell / pixel
- Charge readout pixel buffer
- High gain pixel -> 60 fF integration capacitor
- Pixel with protection diode at the preamplifier input
- Pixel with protection NMOS at the preamplifier input
- New readout scheme ->
 - sampling one pixel row / readout another pixel row in parallel
- New chip readout buffer -> 40 MHz speed, driving 100 Ω termination resistor
- Shift register based-addressing logic

Possible Improvements

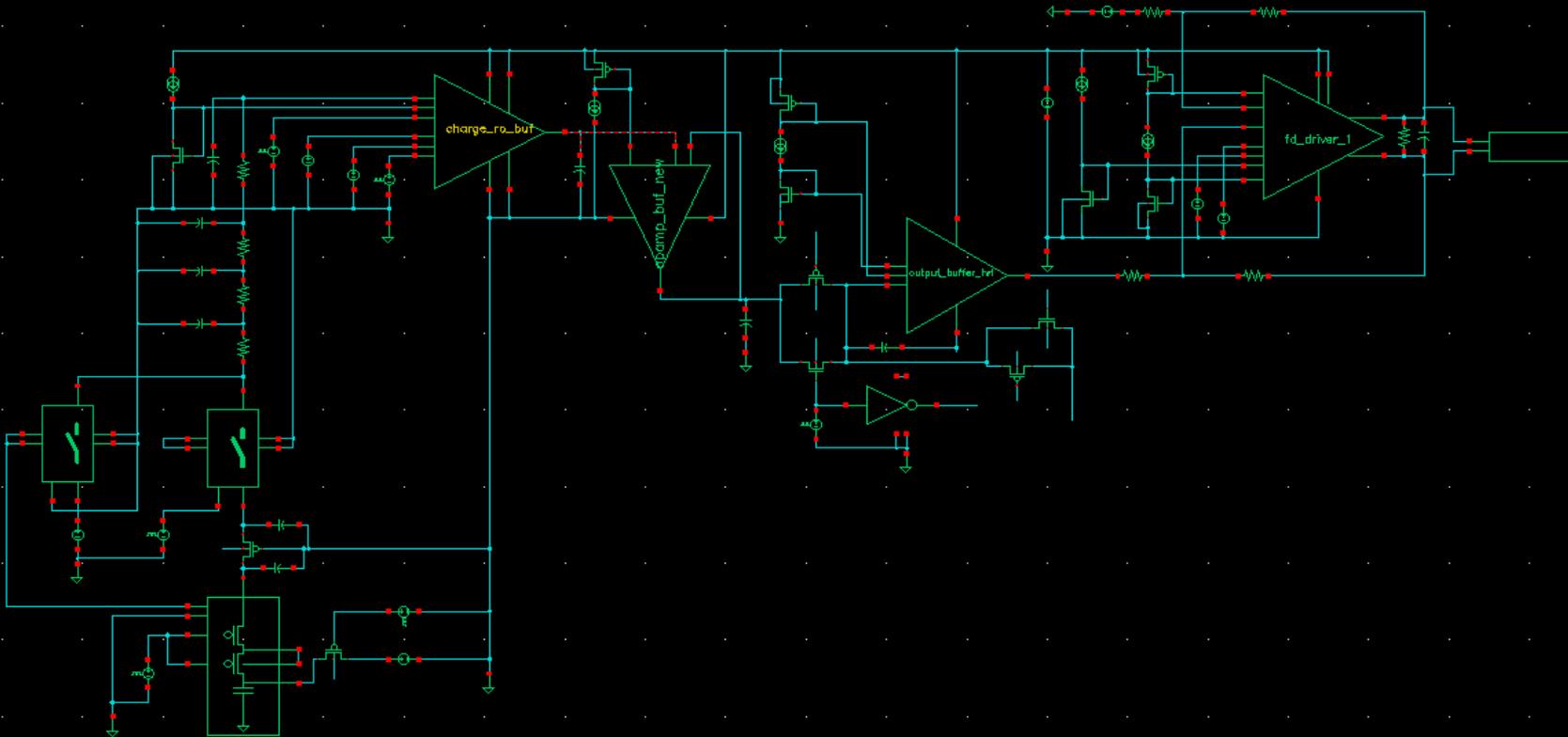


- Moving pixel readout buffer to the column bottom:
 - Reduce power consumption
 - More free space inside the pixel
- Redesign CDS buffer
 - Reduce power consumption
 - Reduce noise
 - Increase output dynamic range

Test Bench of Readout Chain



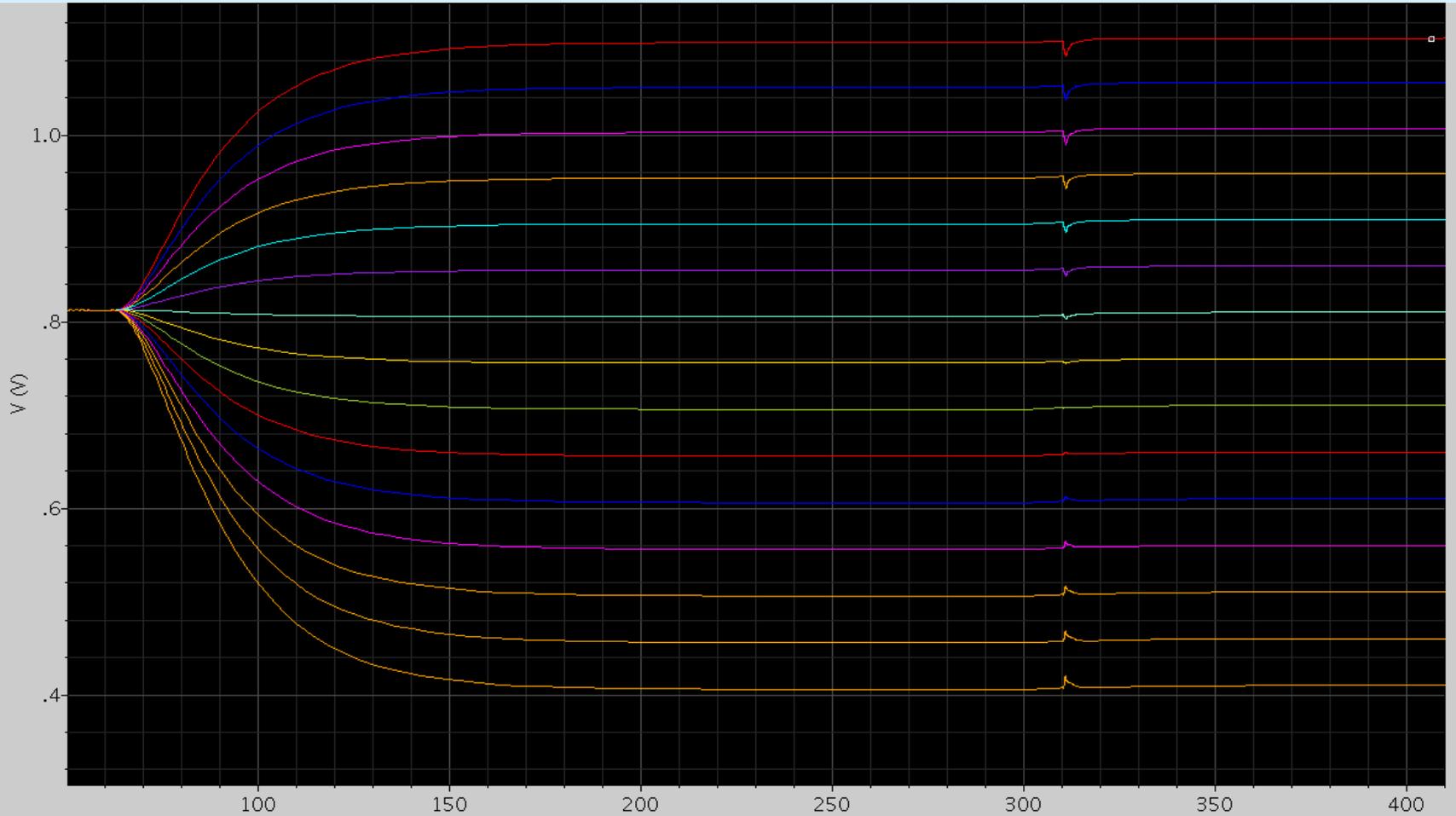
Current consumption: charge_rd_buf 50 uA, opamp_buf_new 260 uA, out_buffer_hrl 700 uA, fd_driver_1 15.5 mA.
Total current = $50\mu\text{A} \times 64 \times 64 + 260\mu\text{A} \times 64 \times 2 + (0.7\text{mA} + 15.5\text{mA}) \times 4 = 303\text{mA}$



Test Bench of Readout Chain



Simulated output of the charge readout buffer at the column bottom



AGIPD Detector



Simulated output of the mux (40 MHz sampling speed)

