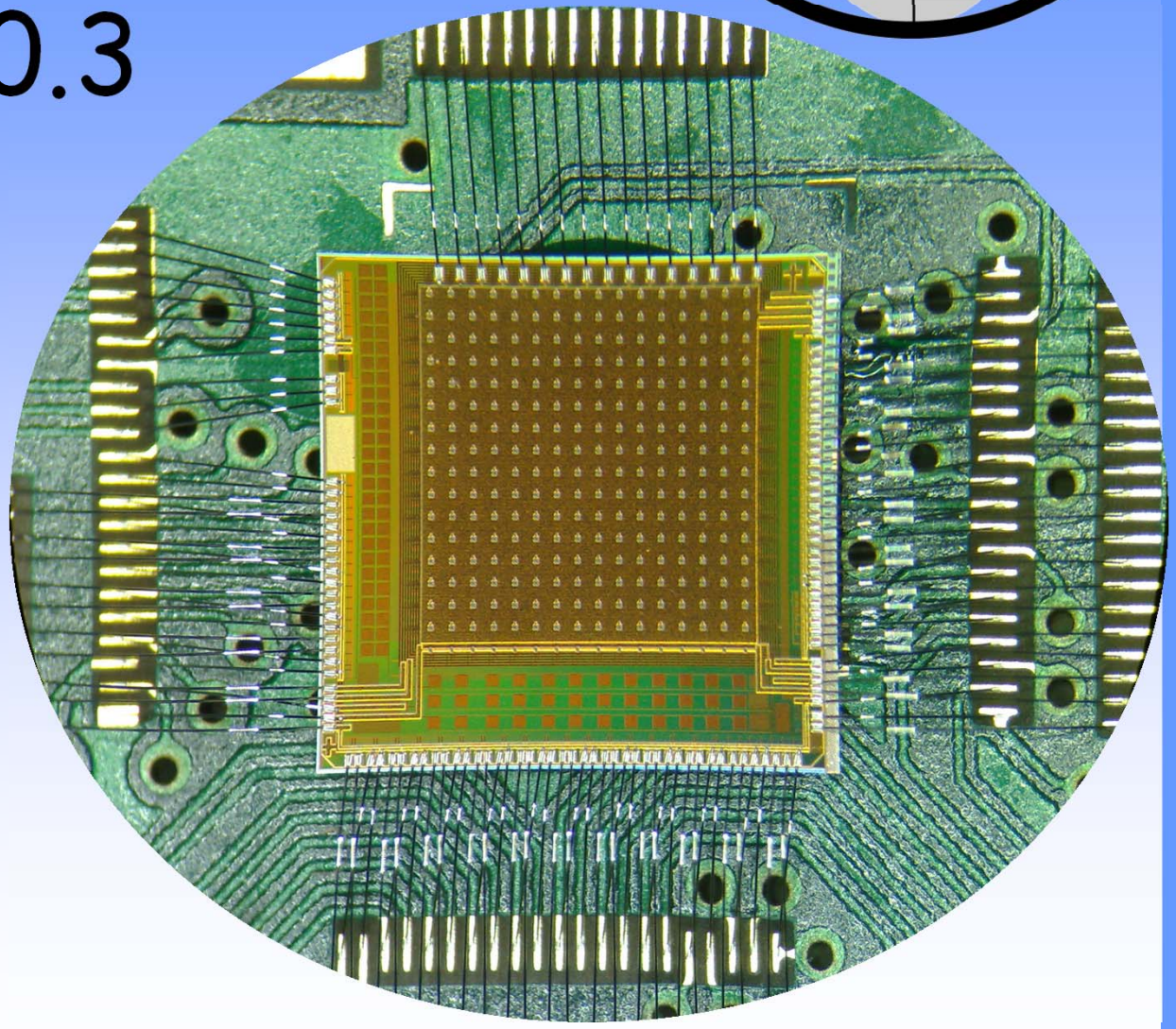
AGIPD 0.3

Logic, Analogue & Radiation Hardness Tests



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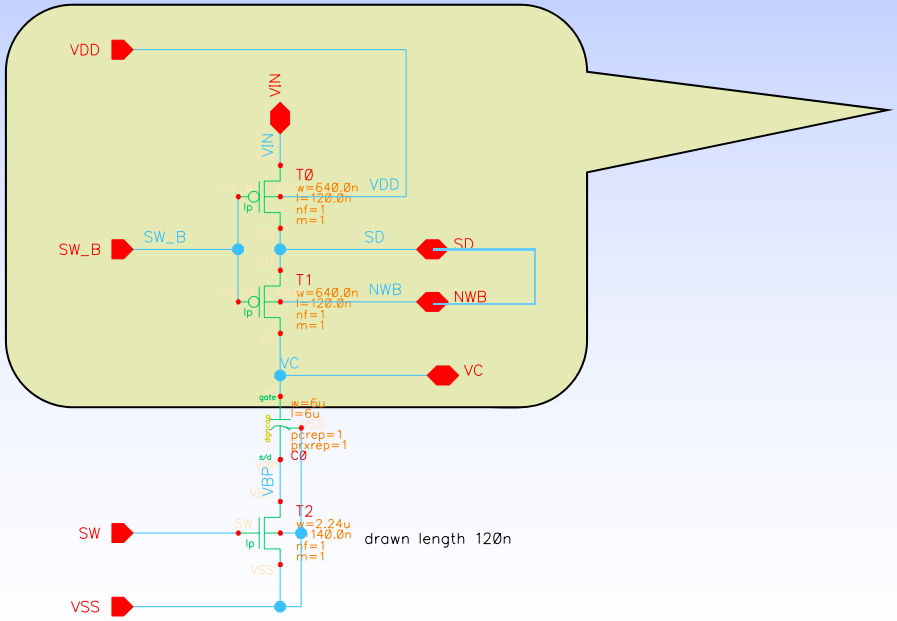
Outline

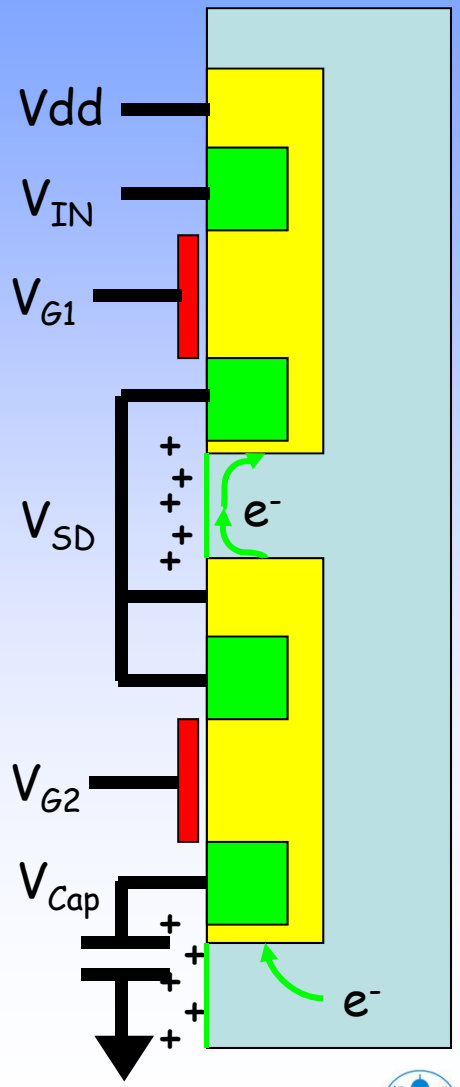
- AGIPD03
- Irradiated Chips
  - pristine
  - 100kGy
  - 1MGy
  - 10MGy (dead)
- Tests
  - Leakage of irradiated Chips
  - Gain
- AGIPD03-HOWTO
- New Readout
- Summary & Outlook

Failure Analysis of "Cell 8"

After Irradiation:

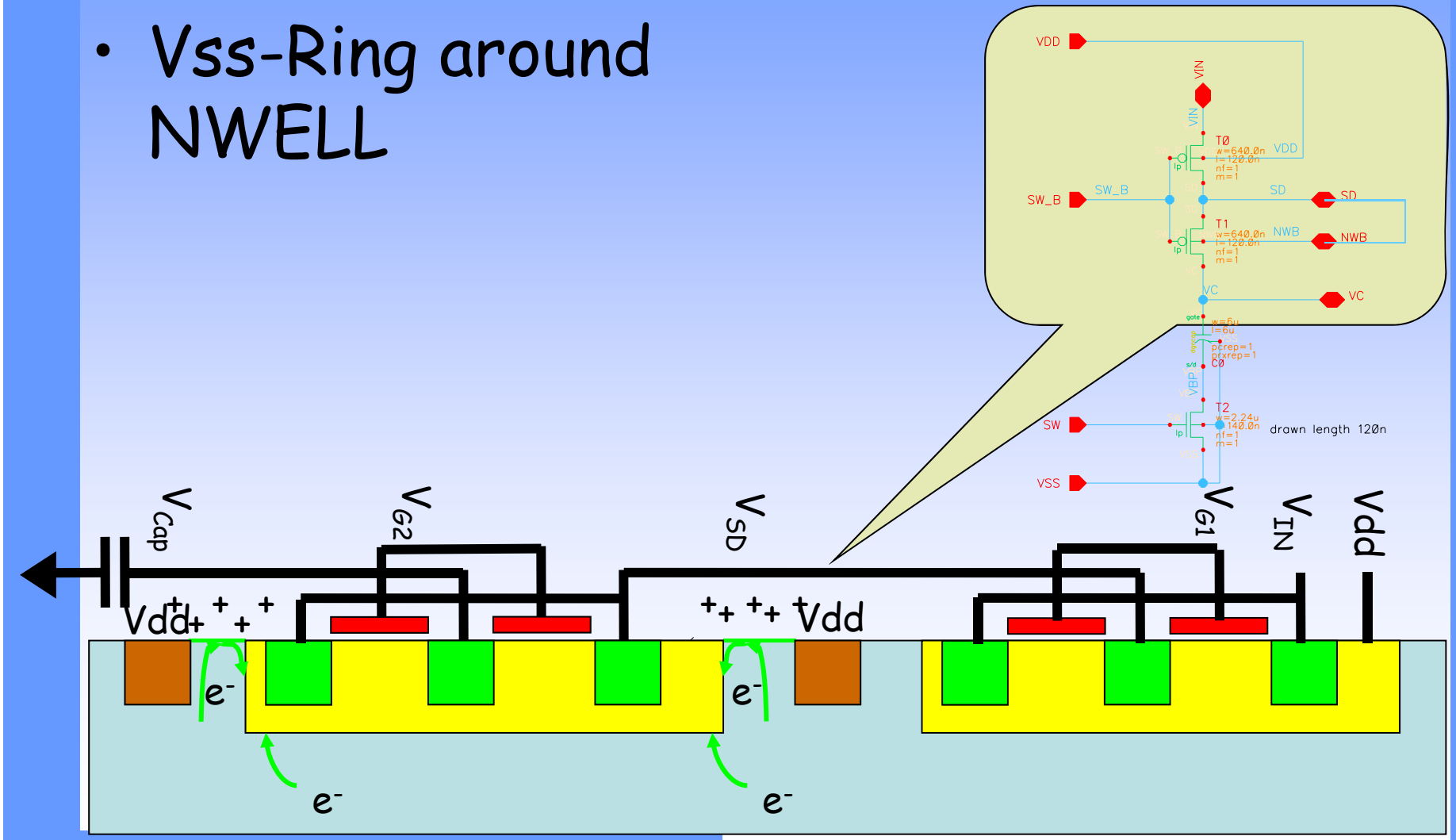
- Lower leakage of Enclosed Cells (1-3)
- High Leakage of "Cell 8"





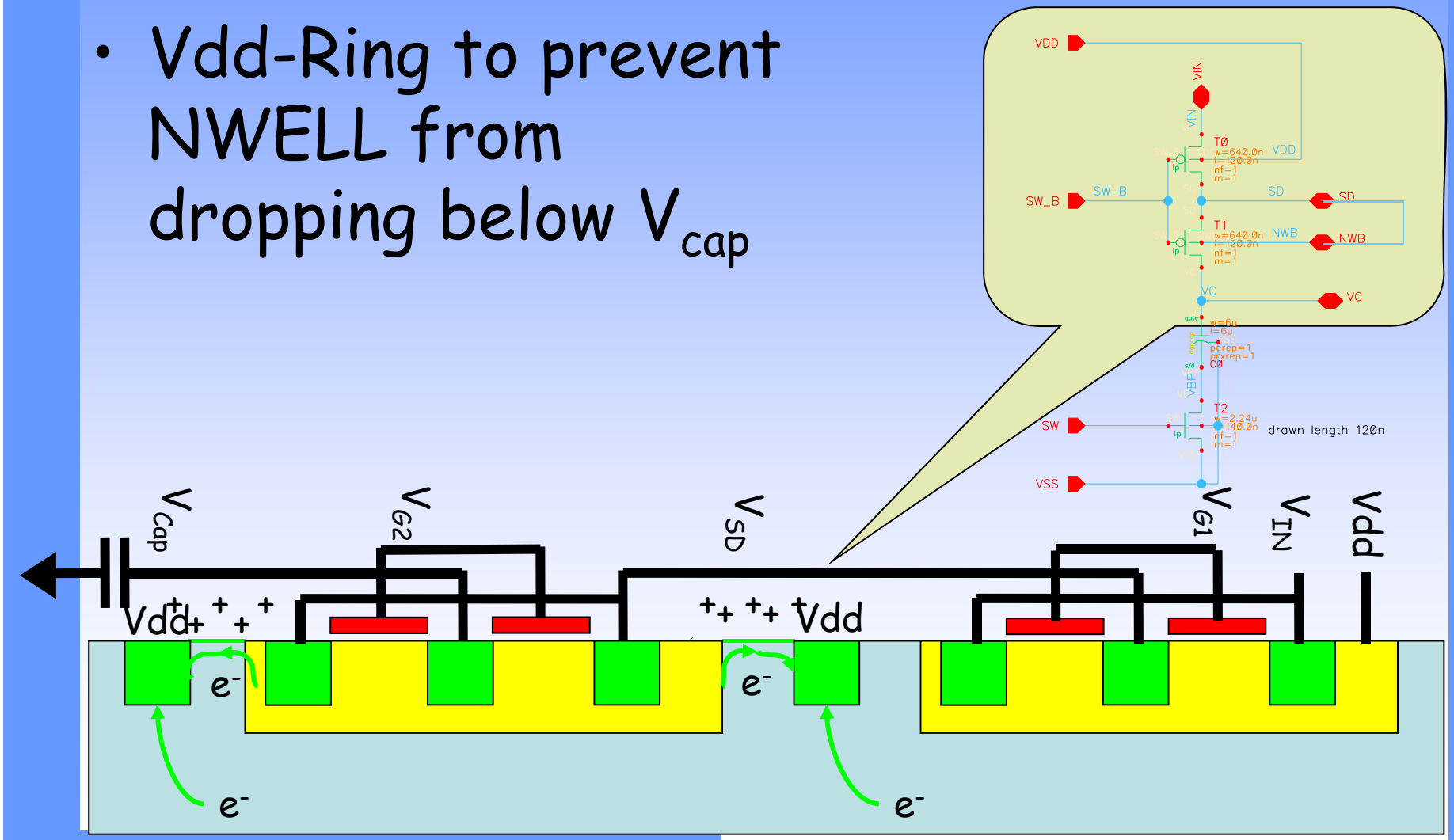
"Cell 8" with Ground Ring

- Vss-Ring around NWELL



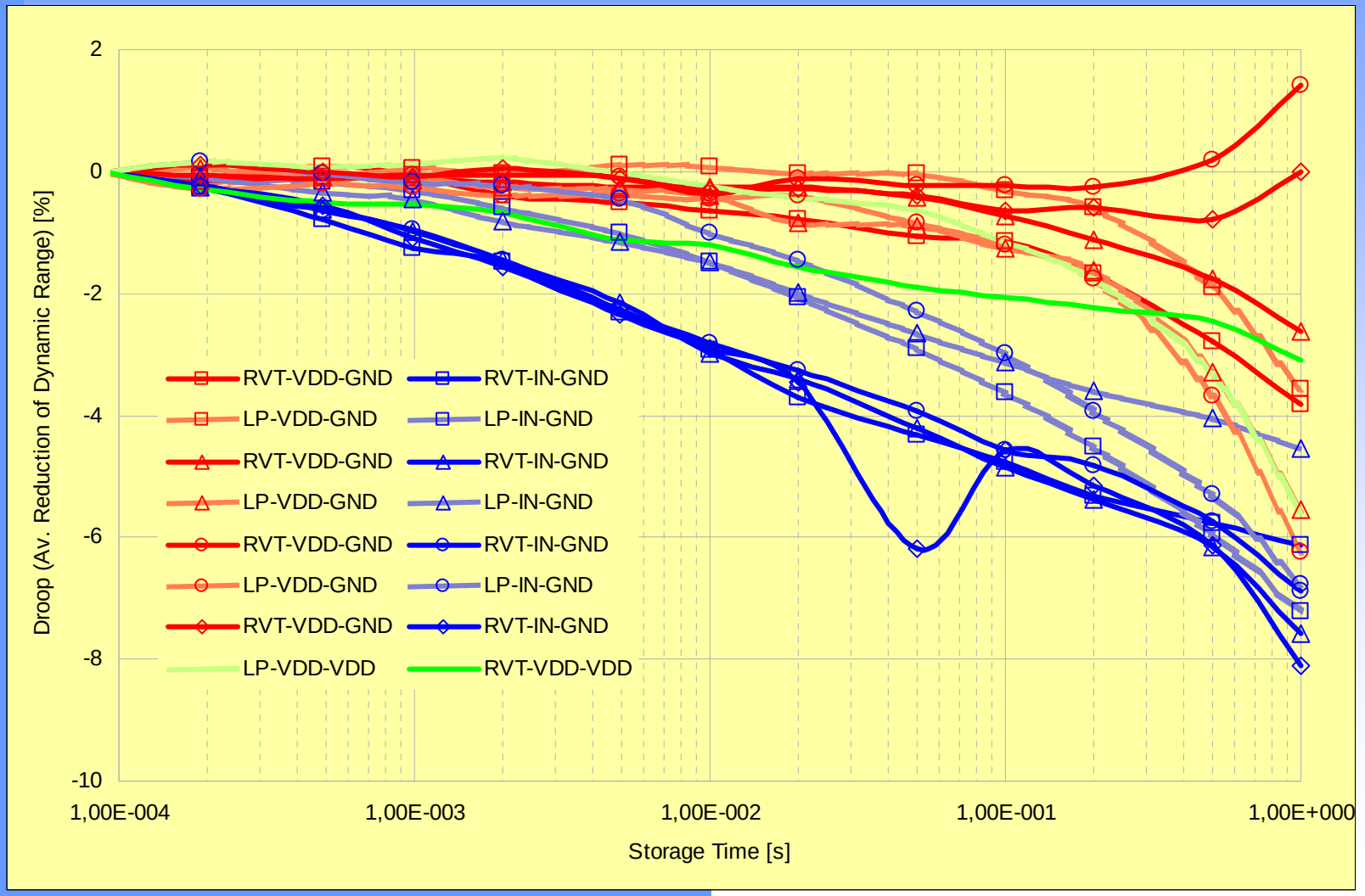
Modified "Cell 8"

- Vdd-Ring to prevent NWELL from dropping below V_{cap}



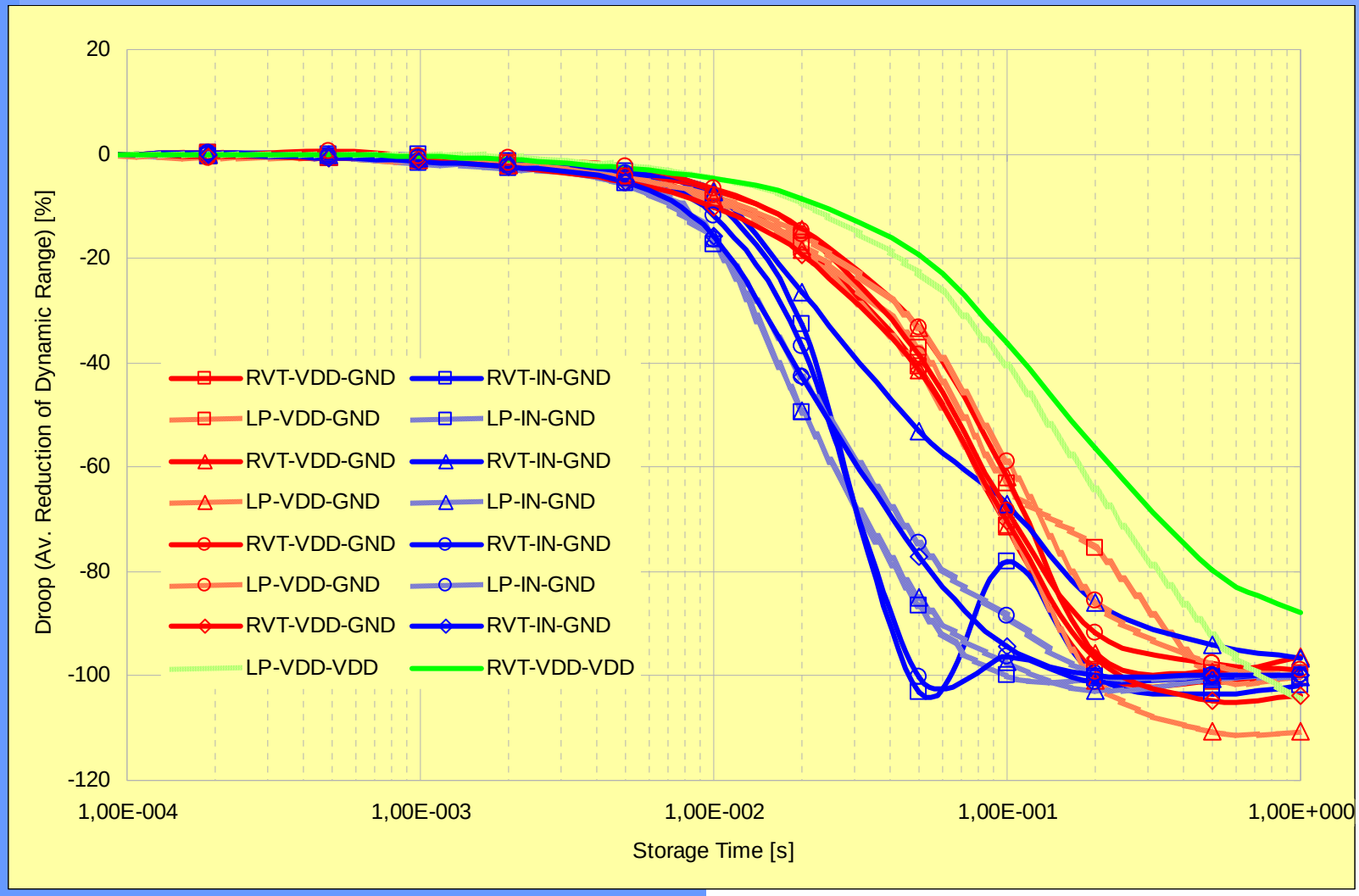
Leakage

0 Gy


2
0
-2
-4
-6
-8
-10
Droop (Av. Reduction of Dynamic Range) [%]
1,00E-004
1,00E-003
1,00E-002
1,00E-001
1,00E+000
Storage Time [s]
RVT-VDD-GND
RVT-IN-GND
LP-VDD-GND
LP-IN-GND
RVT-VDD-GND
RVT-IN-GND
LP-VDD-GND
LP-IN-GND
RVT-VDD-GND
RVT-IN-GND
LP-VDD-GND
LP-IN-GND
RVT-VDD-GND
RVT-IN-GND
LP-VDD-VDD
RVT-VDD-VDD

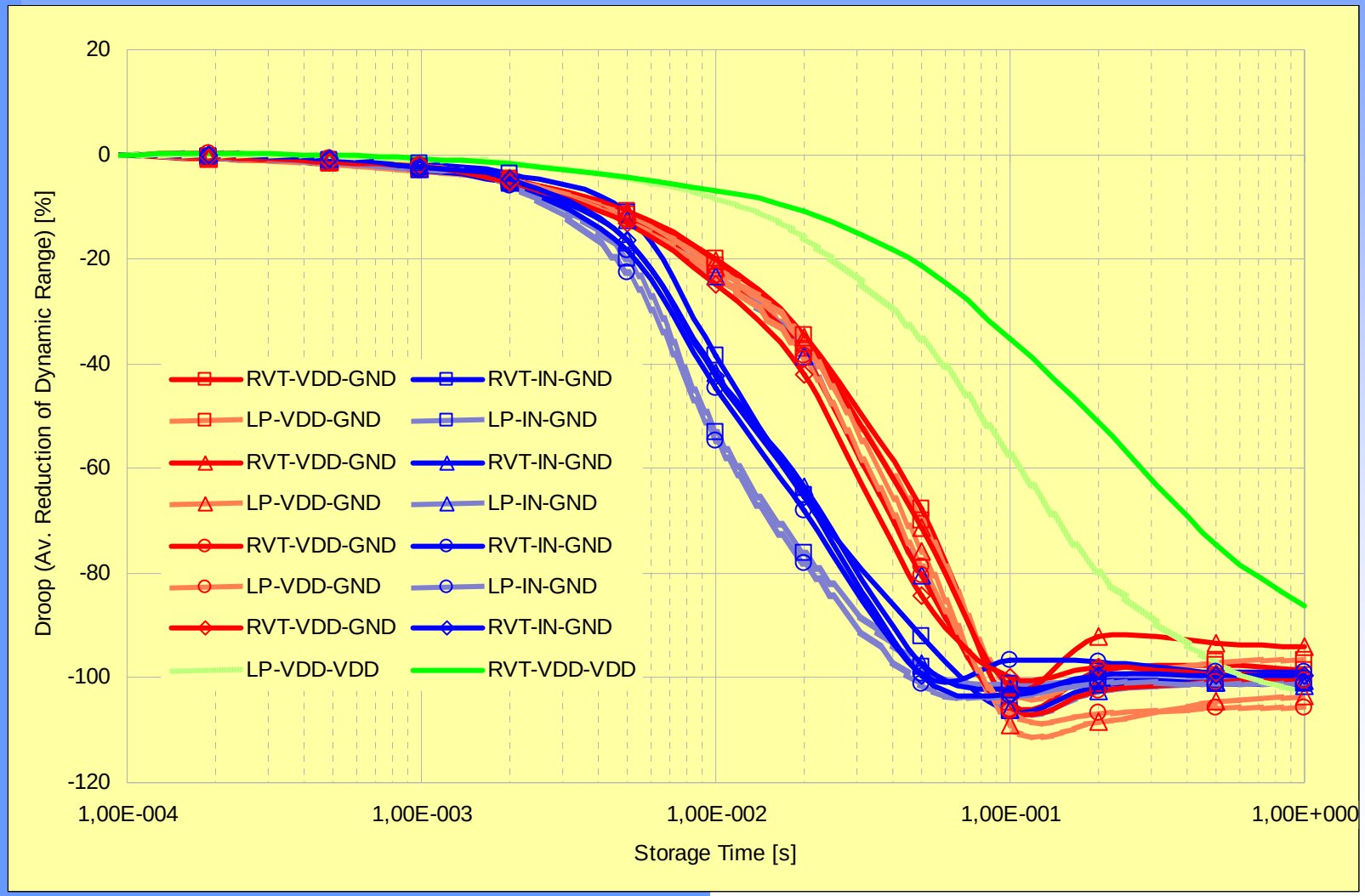
Leakage

100 kGy



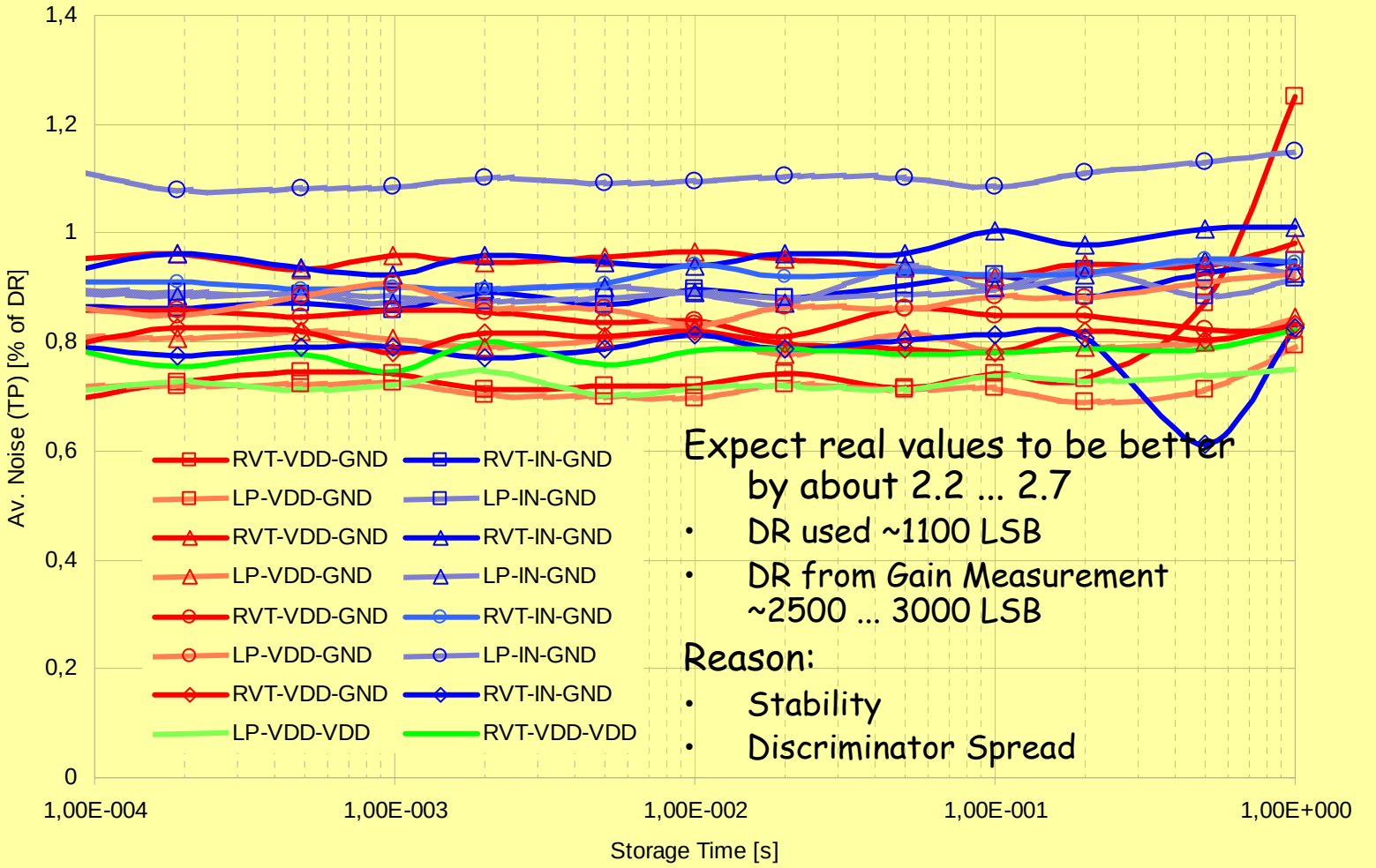
Leakage

1 MGy



Noise

w. Testpulse, 0 Gy



Expect real values to be better by about 2.2 ... 2.7

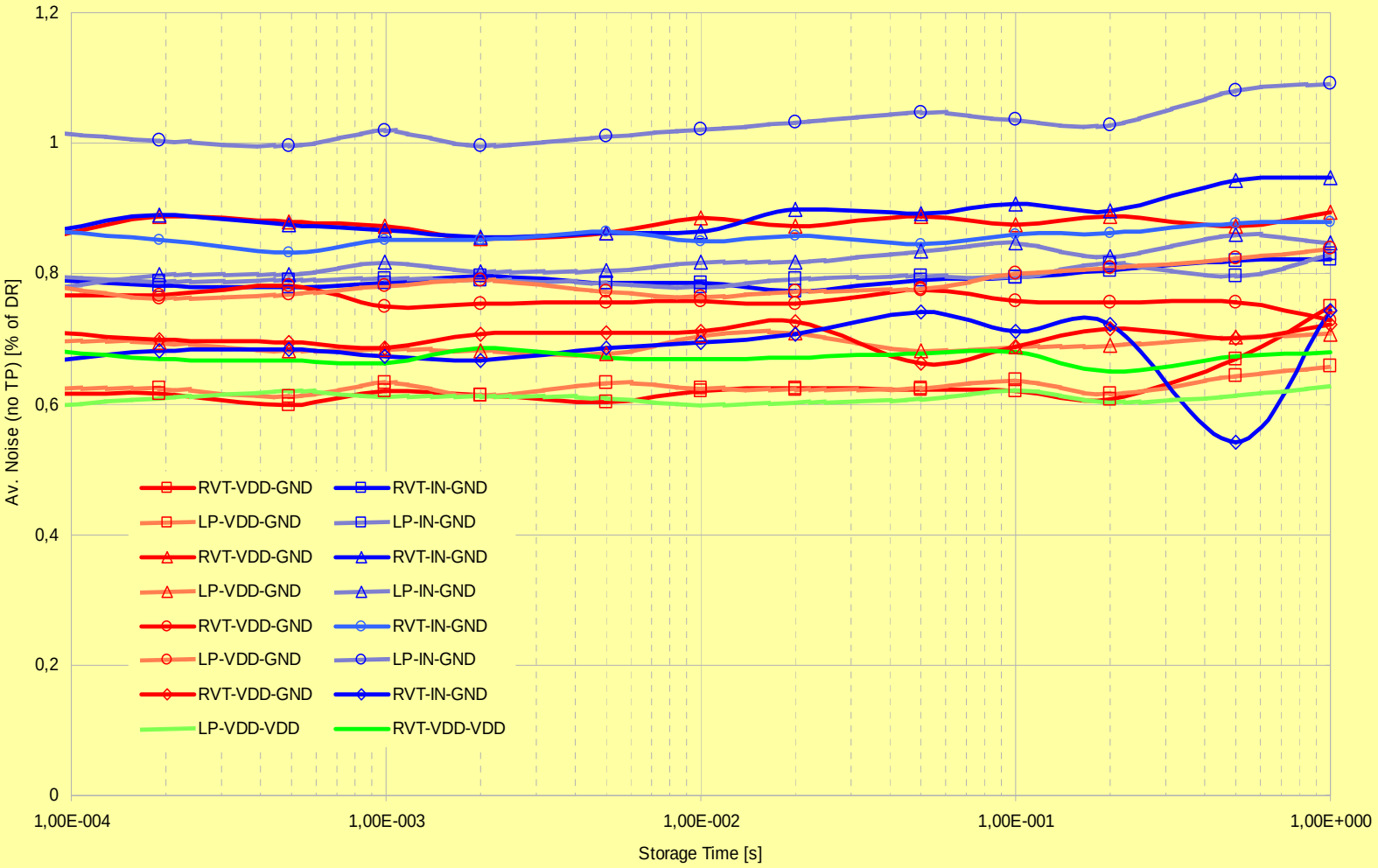
- DR used ~1100 LSB
- DR from Gain Measurement ~2500 ... 3000 LSB

Reason:

- Stability
- Discriminator Spread

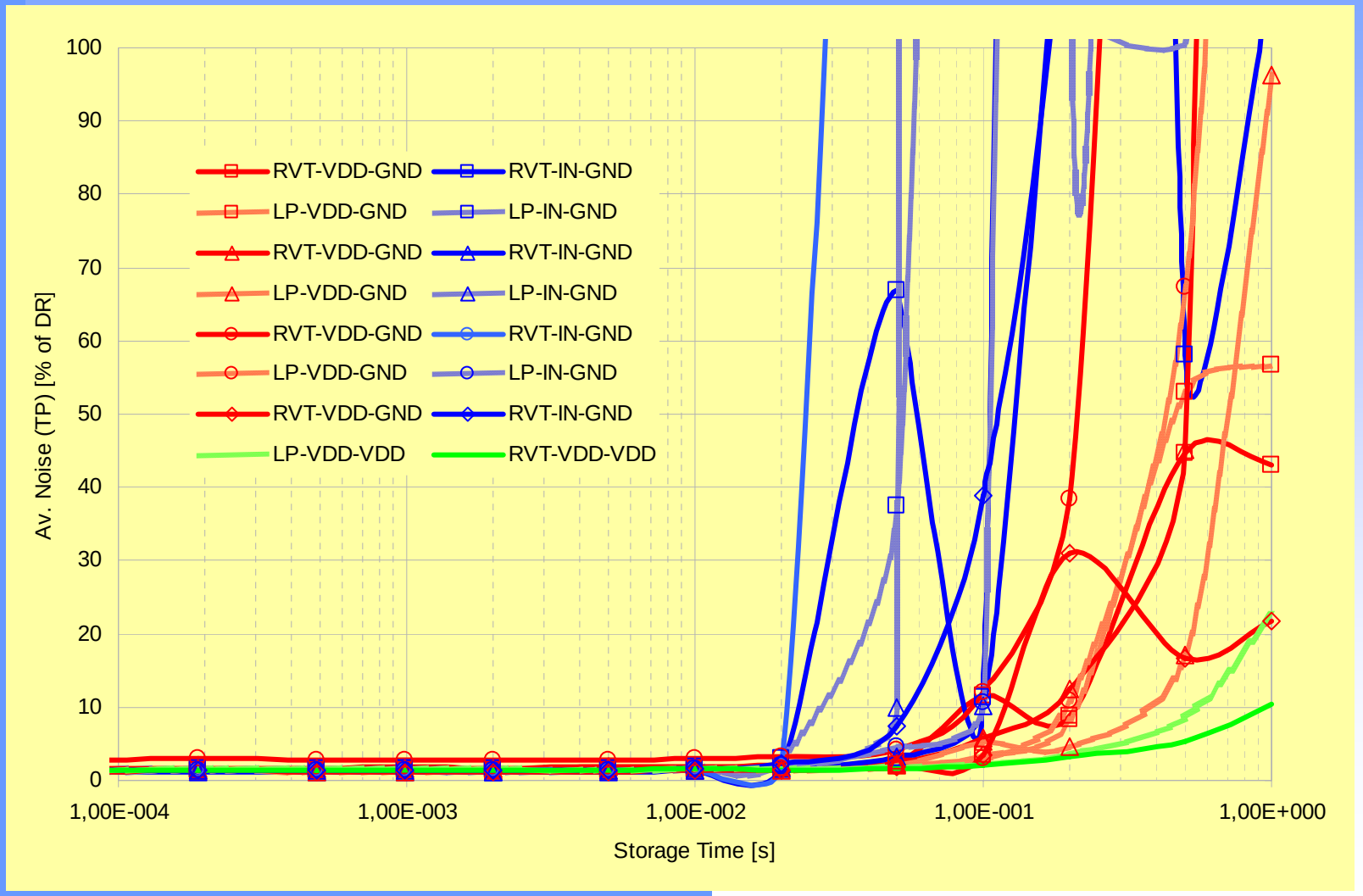
Noise

w/o. Testpulse, 0 Gy



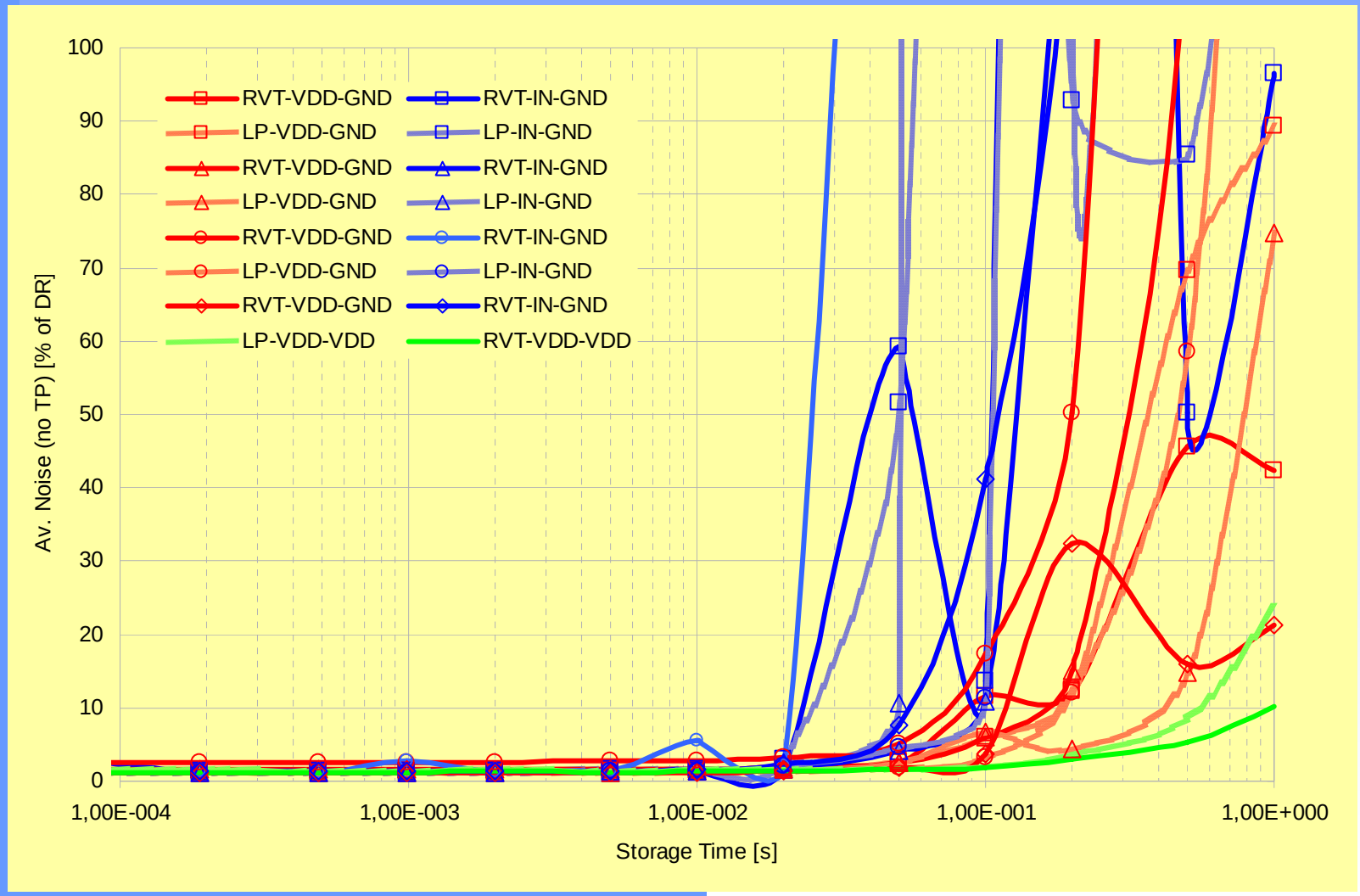
Noise

w. Testpulse, 100 kGy



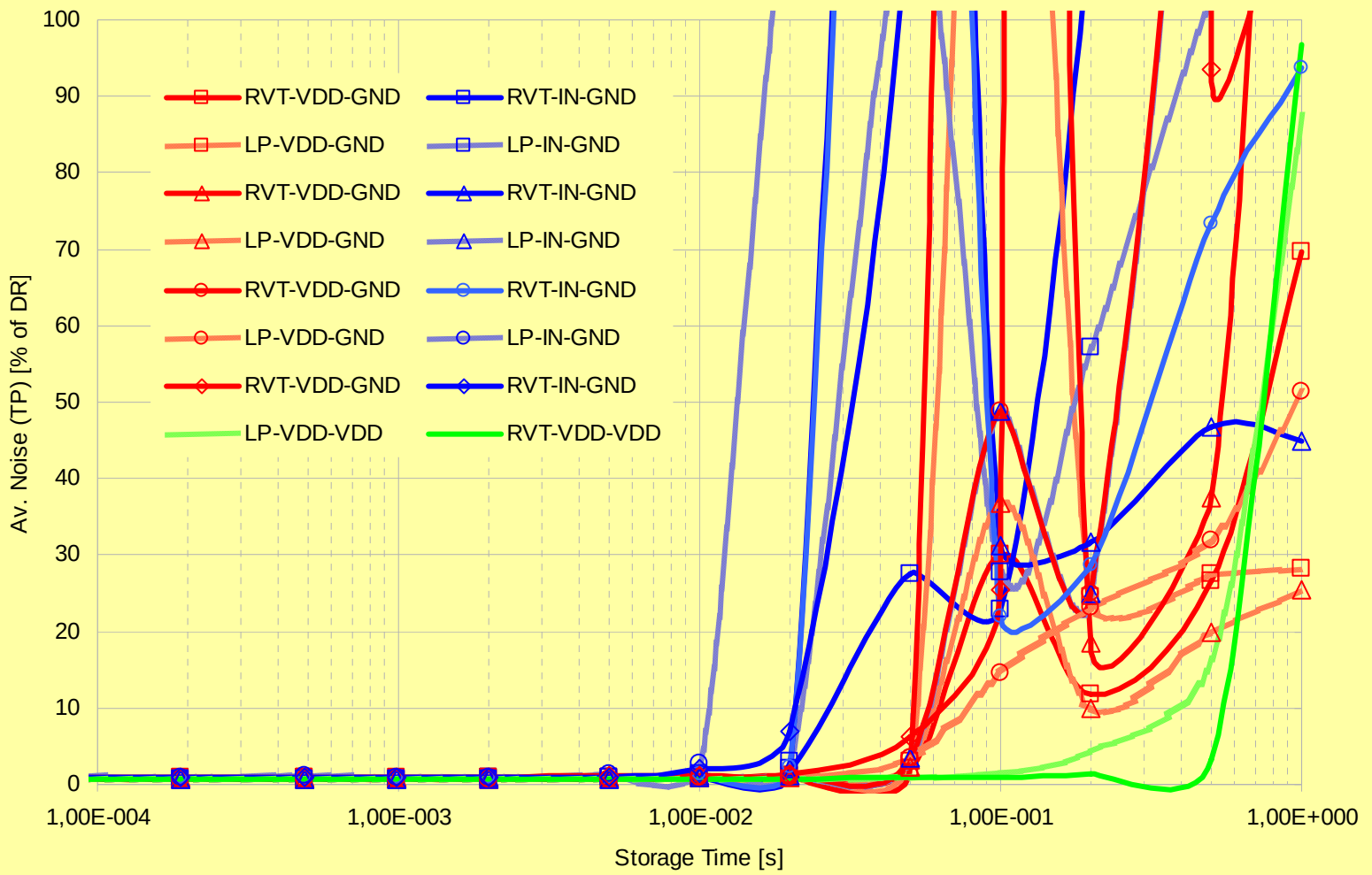
Noise

w/o. Testpulse, 100 kGy



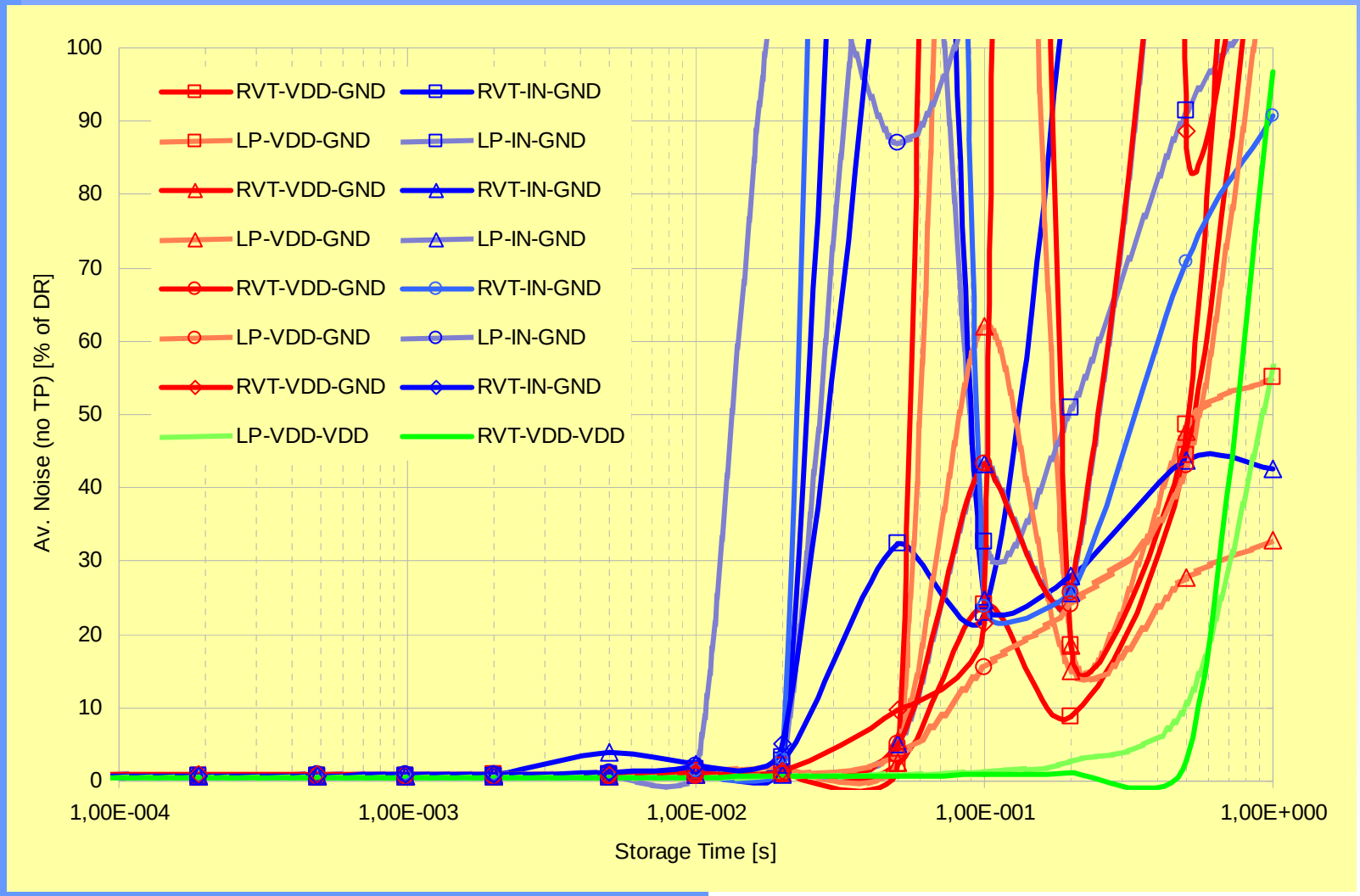
Noise

w. Testpulse, 1 MGy



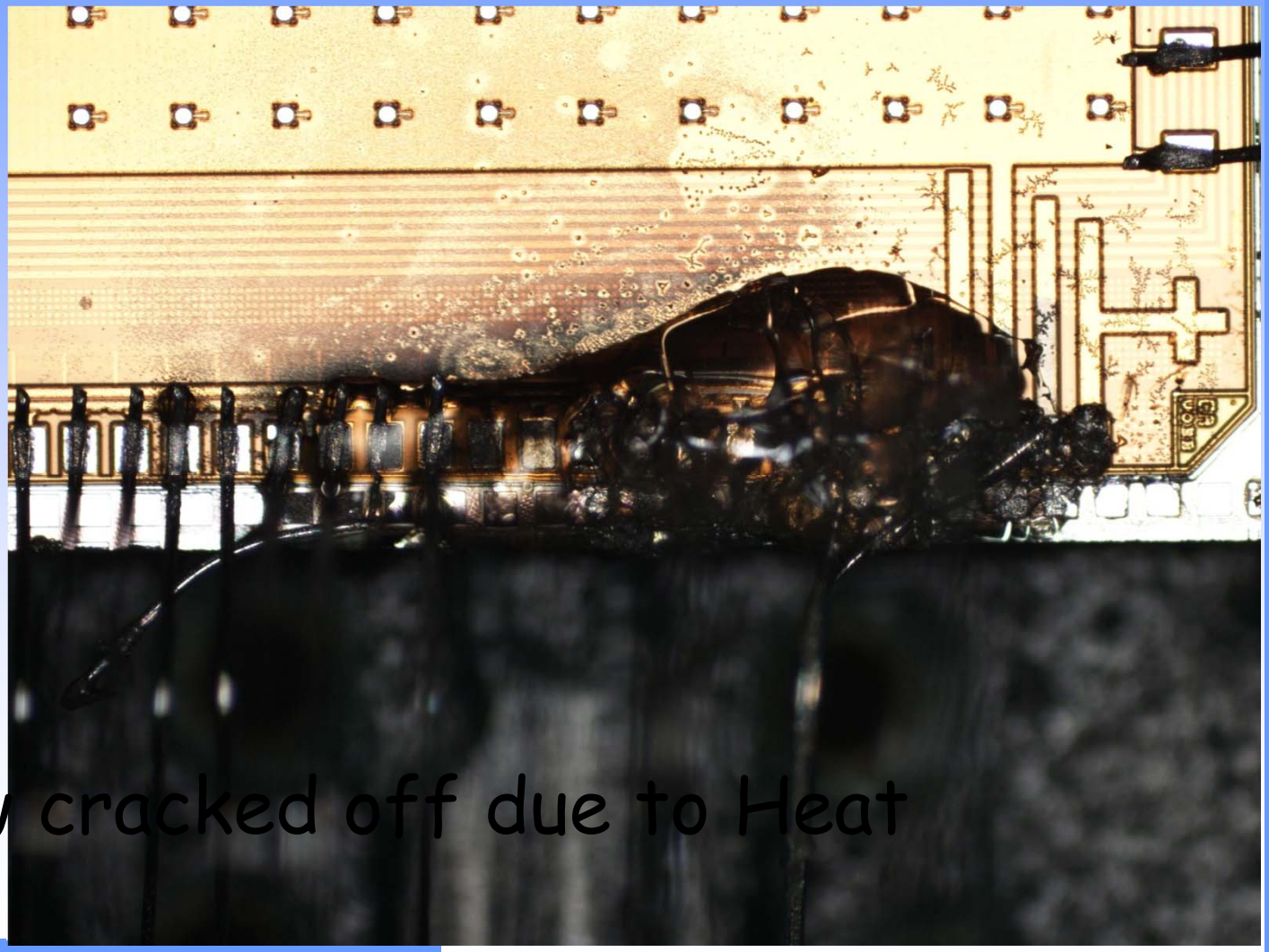
Noise

w/o. Testpulse, 1 MGy



Dead Chip

10 MGy

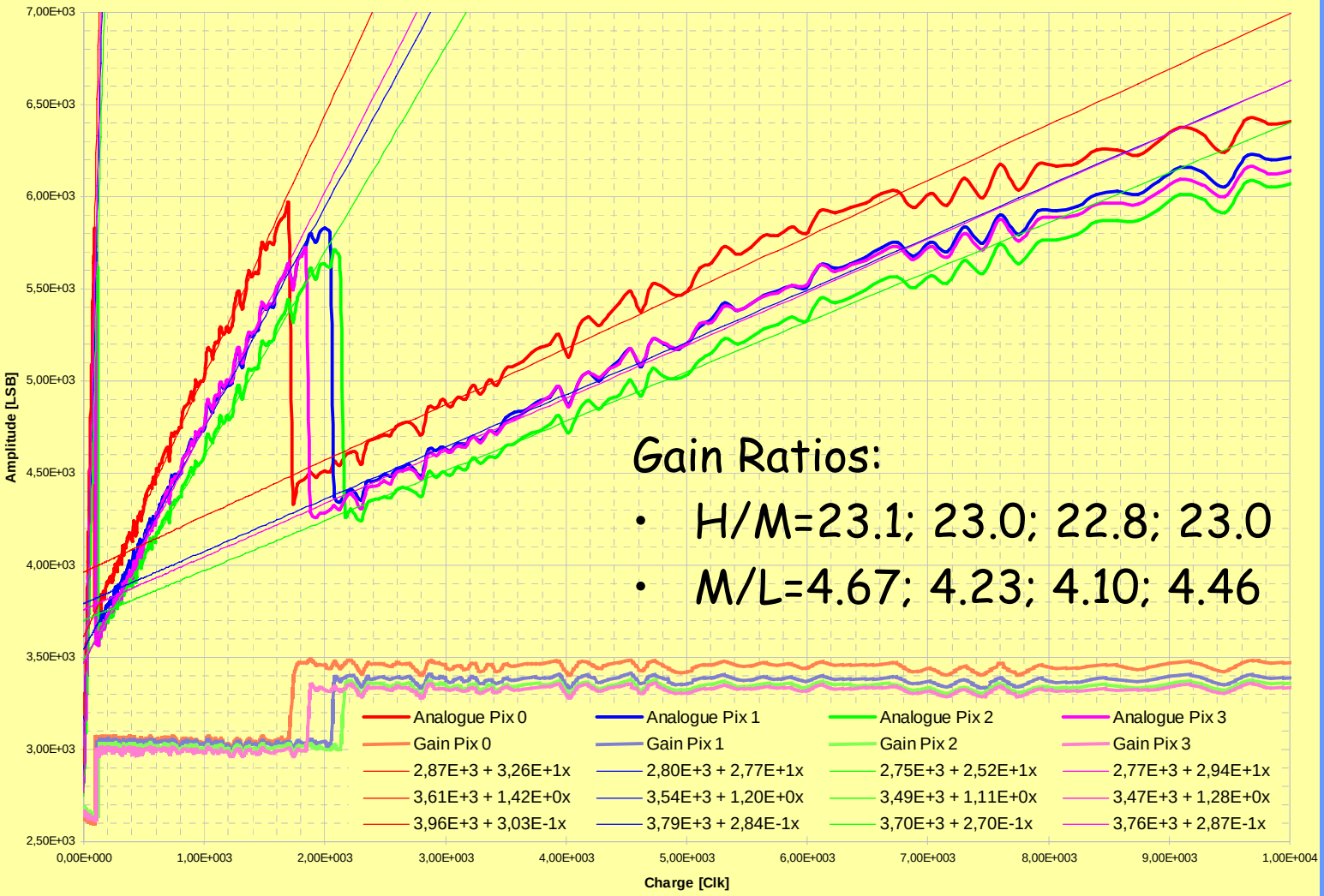


Reason:

Pad Row cracked off due to Heat

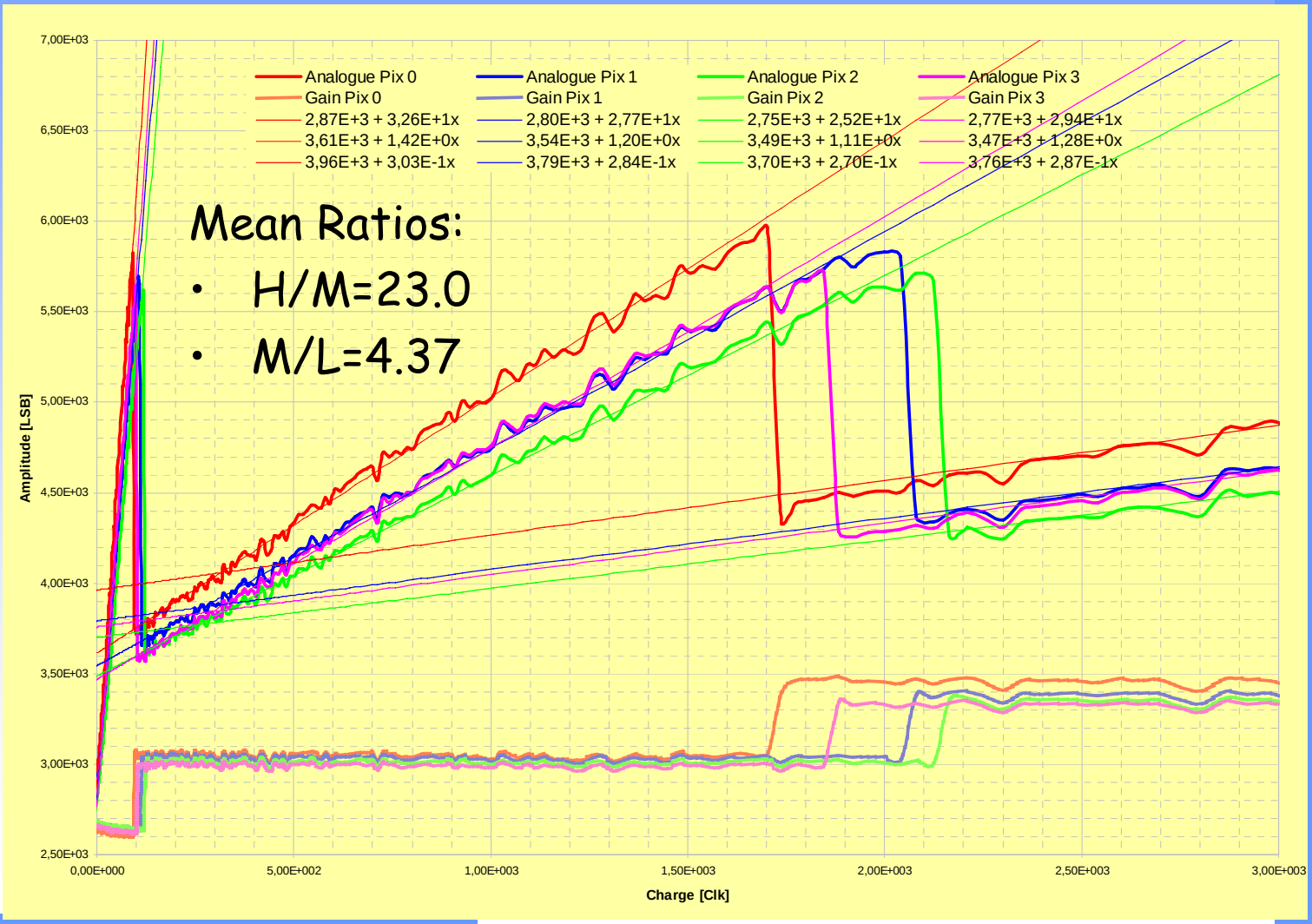
Gains

0 Gy

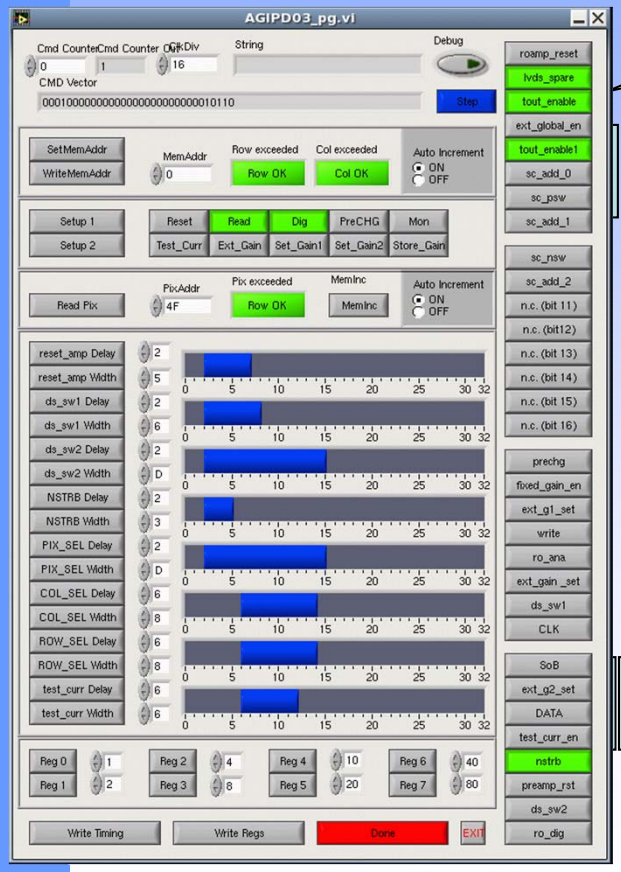

7,00E+03
6,50E+03
6,00E+03
5,50E+03
5,00E+03
4,50E+03
4,00E+03
3,50E+03
3,00E+03
2,50E+03
Amplitude [LSB]
0,00E+000
1,00E+003
2,00E+003
3,00E+003
4,00E+003
5,00E+003
6,00E+003
7,00E+003
8,00E+003
9,00E+003
1,00E+004
Charge [Clk]
Gain Ratios:
• H/M=23.1; 23.0; 22.8; 23.0
• M/L=4.67; 4.23; 4.10; 4.46
Analogue Pix 0
Analogue Pix 1
Analogue Pix 2
Analogue Pix 3
Gain Pix 0
Gain Pix 1
Gain Pix 2
Gain Pix 3
2,87E+3 + 3,26E+1x
2,80E+3 + 2,77E+1x
2,75E+3 + 2,52E+1x
2,77E+3 + 2,94E+1x
3,61E+3 + 1,42E+0x
3,54E+3 + 1,20E+0x
3,49E+3 + 1,11E+0x
3,47E+3 + 1,28E+0x
3,96E+3 + 3,03E-1x
3,79E+3 + 2,84E-1x
3,70E+3 + 2,70E-1x
3,76E+3 + 2,87E-1x

Gains

0 Gy


Analogue Pix 0
Gain Pix 0
2,87E+3 + 3,26E+1x
3,61E+3 + 1,42E+0x
3,96E+3 + 3,03E-1x
Analogue Pix 1
Gain Pix 1
2,80E+3 + 2,77E+1x
3,54E+3 + 1,20E+0x
3,79E+3 + 2,84E-1x
Analogue Pix 2
Gain Pix 2
2,75E+3 + 2,52E+1x
3,49E+3 + 1,11E+0x
3,70E+3 + 2,70E-1x
Analogue Pix 3
Gain Pix 3
2,77E+3 + 2,94E+1x
3,47E+3 + 1,28E+0x
3,76E+3 + 2,87E-1x
Mean Ratios:
• H/M=23.0
• M/L=4.37
Amplitude [LSB]
7,00E+03
6,50E+03
6,00E+03
5,50E+03
5,00E+03
4,50E+03
4,00E+03
3,50E+03
3,00E+03
2,50E+03
0,00E+000
5,00E+002
1,00E+003
1,50E+003
2,00E+003
2,50E+003
3,00E+003
Charge [Clk]

AGIPD03 (Periphery) Test Bed



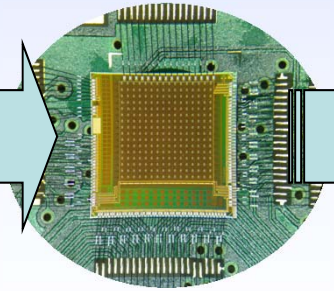
Stimulus Generation vi

Verilog Simulation

Functional

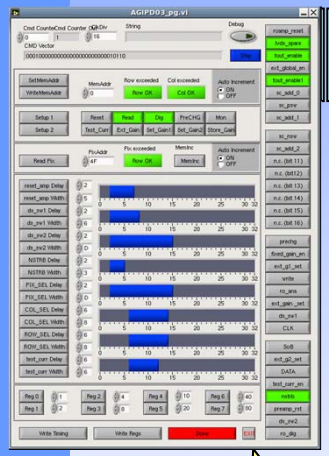
Netlist

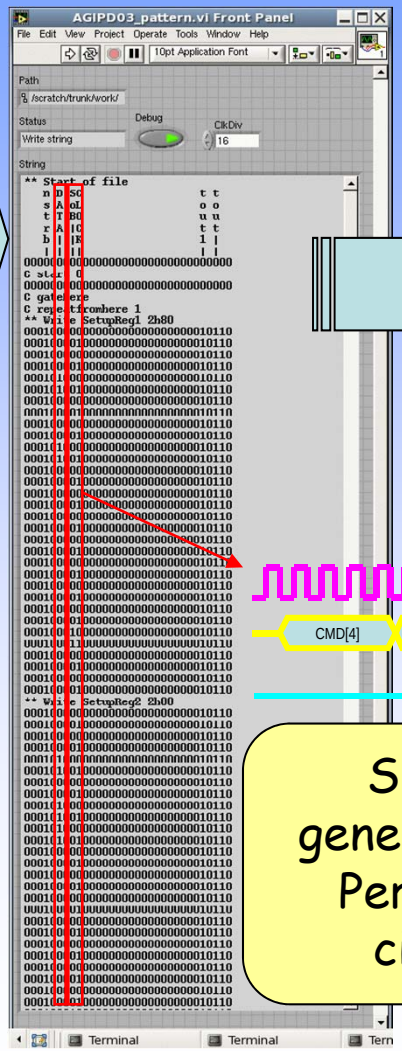
Visualisation vi

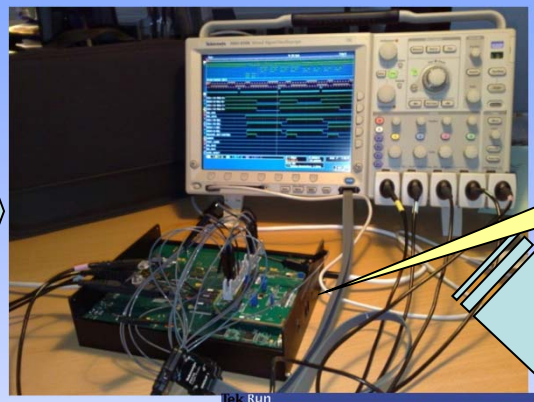


Visualisation (chiptest_gui)

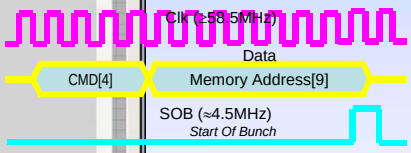
AGIPD03 Test Bed

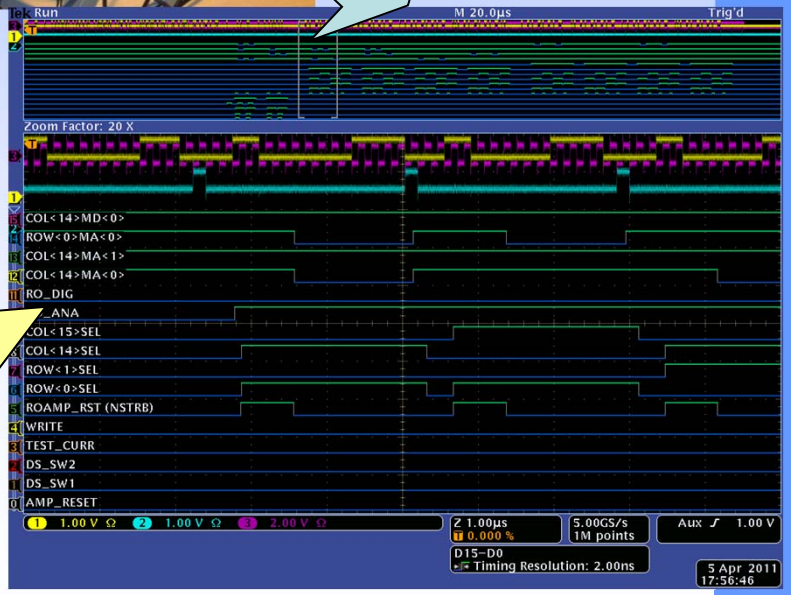






AGIPD Chiptestboard

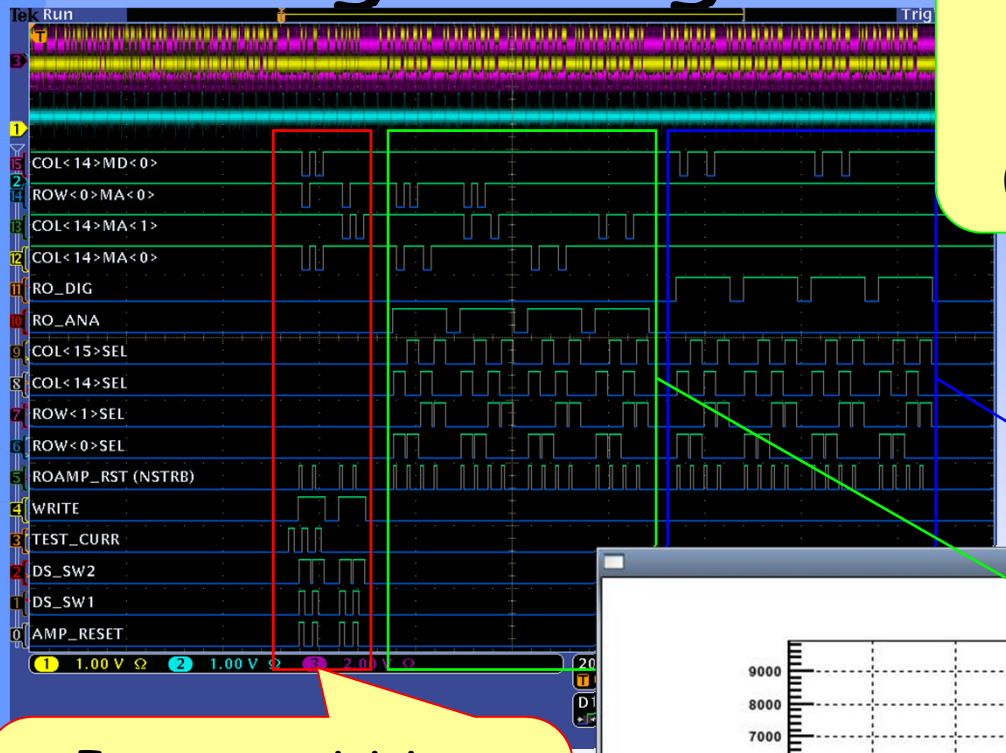




Stimulus Generation vi

Signals generated by Periphery circuit

AGIPD03 Analogue Signals



Amplitude readout of 4 pixels (0x0E, 0x0F, 0x1E, 0x1F) of 4 frames (mem 0x000, 0x001, 0x010, 0x011)

Readout of gain settings

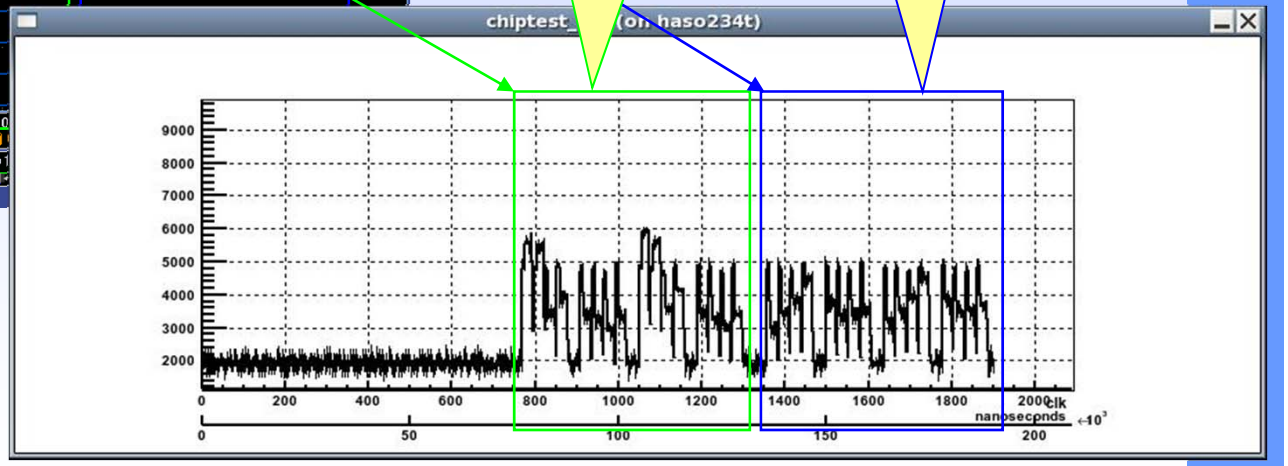


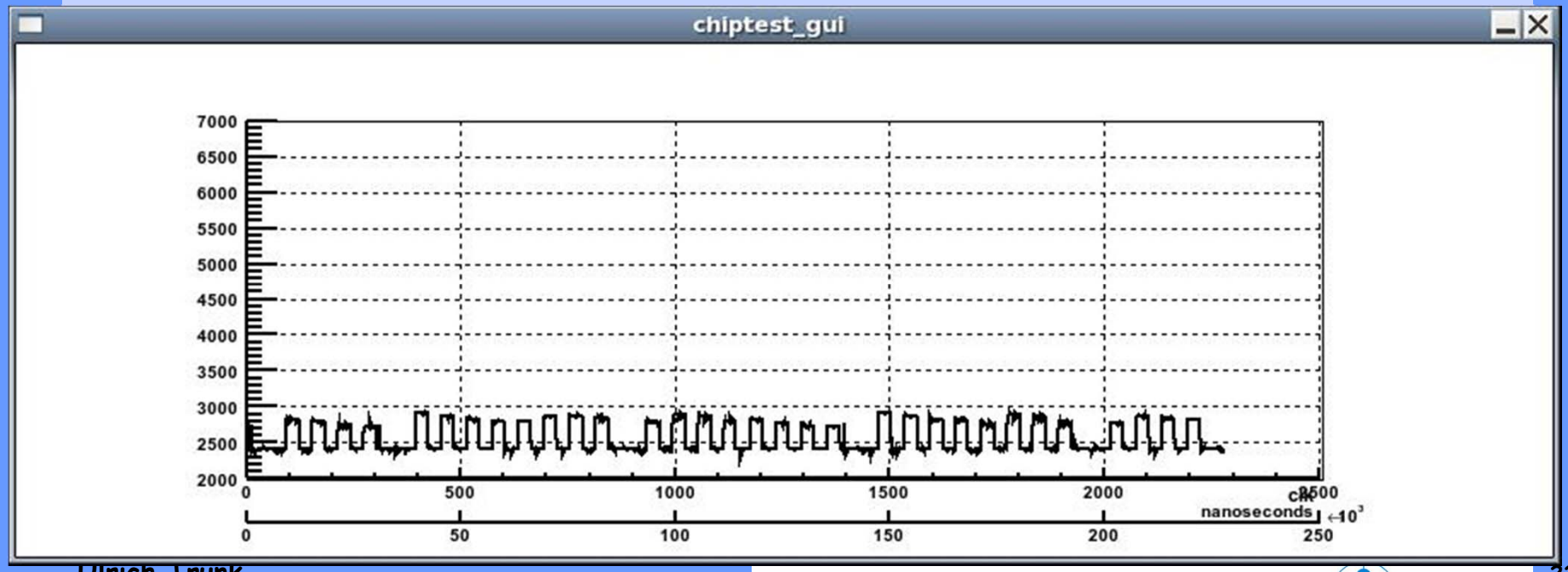
Image acquisition: 4 frames (mem 0x000, 0x010, 0x001, 0x011)

Column Parallel Readout
AGIPD04/AGIPD10

- Based double (even/odd row) column lines
- Uses 32 CH mux in interleaved order (1,3, … 31, 2, 4, … 32) (odd & even rows)
- Shorter (4 clk?) read commands
- No additional sampling at end of column

AGIPD03 Summary

- AGIPD03 works!
- No discrepancy from Verilog code found up to now!
- Preamp/DS-Amp/Ro-Amp should be reset via external signals, when not reading/writing data
  - Shortcoming of Verilog code
  - To be fixed in the next version
- Faster Readout (column parallel, w. shorter CMD) needed



Column Parallel Readout

AGIPD04/AGIPD10