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HPAD 0.2 Submission - Bonn

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Overview

- Motivation
- Implemented structures (test chip including 4 different developments)
  - switch test structures
  - 8 cell analog pipeline
  - I^2C interface (not connected to the above)
  - tripple-well nfet (*nfettw*) test structures
- Pipeline issues
- General remarks

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Motivation

- HPAD 0.1 switch test structures all *DGPFET* (thick gate oxide, 2.5V, reg. Vt)
- favorite device because:
  - no gate leakage
  - low off-current
  - sustain higher dynamical range (2.5V instead of 1.5V)

But, too bad:

- HPAD 0.1 irradiation results showed high V_{th} shift (< 700mV after 10MGy)

- Unless dose rate effect is not significant (is it?) we cannot use this type of transistor

Switch Design Challenges

- charge up the sampling capacitor within 200 ns sampling time
- store the voltage during 100ms (worst case) hold time
- do both with an error of less than 0.1% (1%)

settling time constant: $C_S \cdot r_{ON} = 28ns\ (43ns)$

hold time constant: $C_S \cdot r_{OFF} = 20s\ (2s)$

➔ ratio $r_{ON}/r_{OFF} = 7 \cdot 10^8\ (4 \cdot 10^7)$!

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Differences HPAD 0.1 ←→HPAD 0.2

On HPAD 0.1 there were two different type of structures to study device leakage

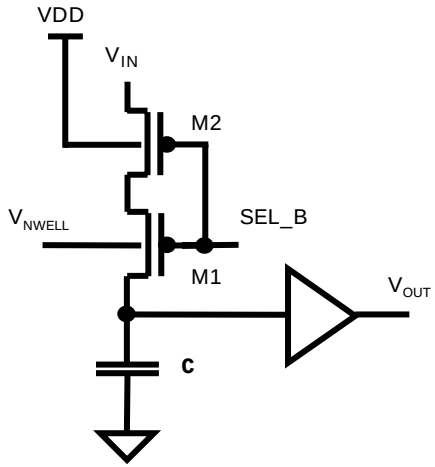
1. devices arrays (switches and capacitors)
   - many **devices in parallel** to make ultra low current measurements feasible (O(1000) devices, sub pA per device)
   - measure dc currents (**V-I curves**)
2. sampling cells
   - combination of switch, capacitor and buffer
   - measure (**time dependent**) voltage drop on sampling capacitor

New switch test structures are implemented as sampling cells

- ***DGNCAP*** capacitors (showed negligible leakage current on HPAD 0.1)
- Zero-VT *DGNFET* **source follower**
- different ***PFET*** (thin gate oxide) switch configurations

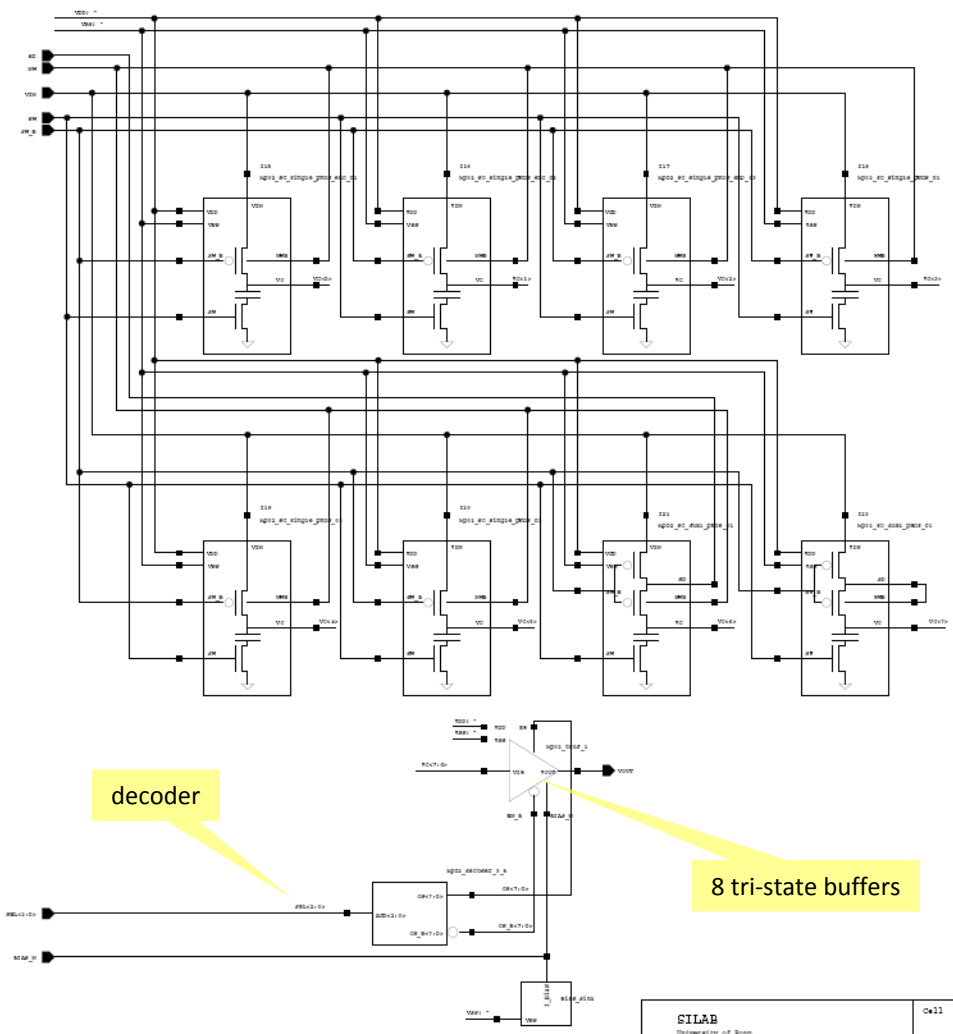
HPAD 0.2 Switch Test Structures

- Sampling cells, 8 variants:
  - all ***LPPFET*** (low power, high V_T):
  - single (w/o M2) or dual switch configurations
  - W/L variations
  - **enclosed** and **linear**
  - 6µx6µ *DGNCAP* (≥200fF, non-linear!) capacitor



Cell #	Enc.	D/S	V_{THR}	W/L	NWELL	SD	Comments
1	Y	S	LP	2.24/0.12	external	-	W_{min} = 2.24 for enc. layout
2	Y	S	LP	2.24/0.24	external	-	
3	Y	S	LP	2.24/0.36	external	-	
4	N	S	LP	0.32/0.12	external	-	
5	N	S	LP	0.64/0.12	external	-	
6	N	S	LP	0.64/0.24	external	-	
7	N	D	LP	0.64/0.12 (both)	external	external	
8	N	D	LP	0.64/0.12 (both)	-	-	$V_{SD} = V_{NWELL}$

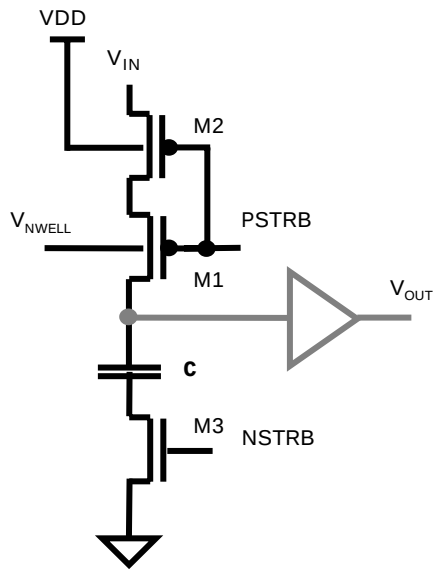
HPAD 0.2 Switch Test Structures



Towards the Analog Pipeline

- Analog memory test structure
  - 8 sampling cells
  - based on type 8 cell
    (dual switch, linear *lppfet*, W/L = 0.64/0.12)

- Modifications
  - added **bottom plate switch** for all cells
  - V_{SD} floating
  - One cell with buffer at capacitor node
  - small **digital part** to generate **control signals**



Analog Pipeline Issues

Charge injection

- hard to compensate off-line if **signal dependent**
- can be reduced to **constant offset** if switch source node sees a (low impedance) **constant voltage**

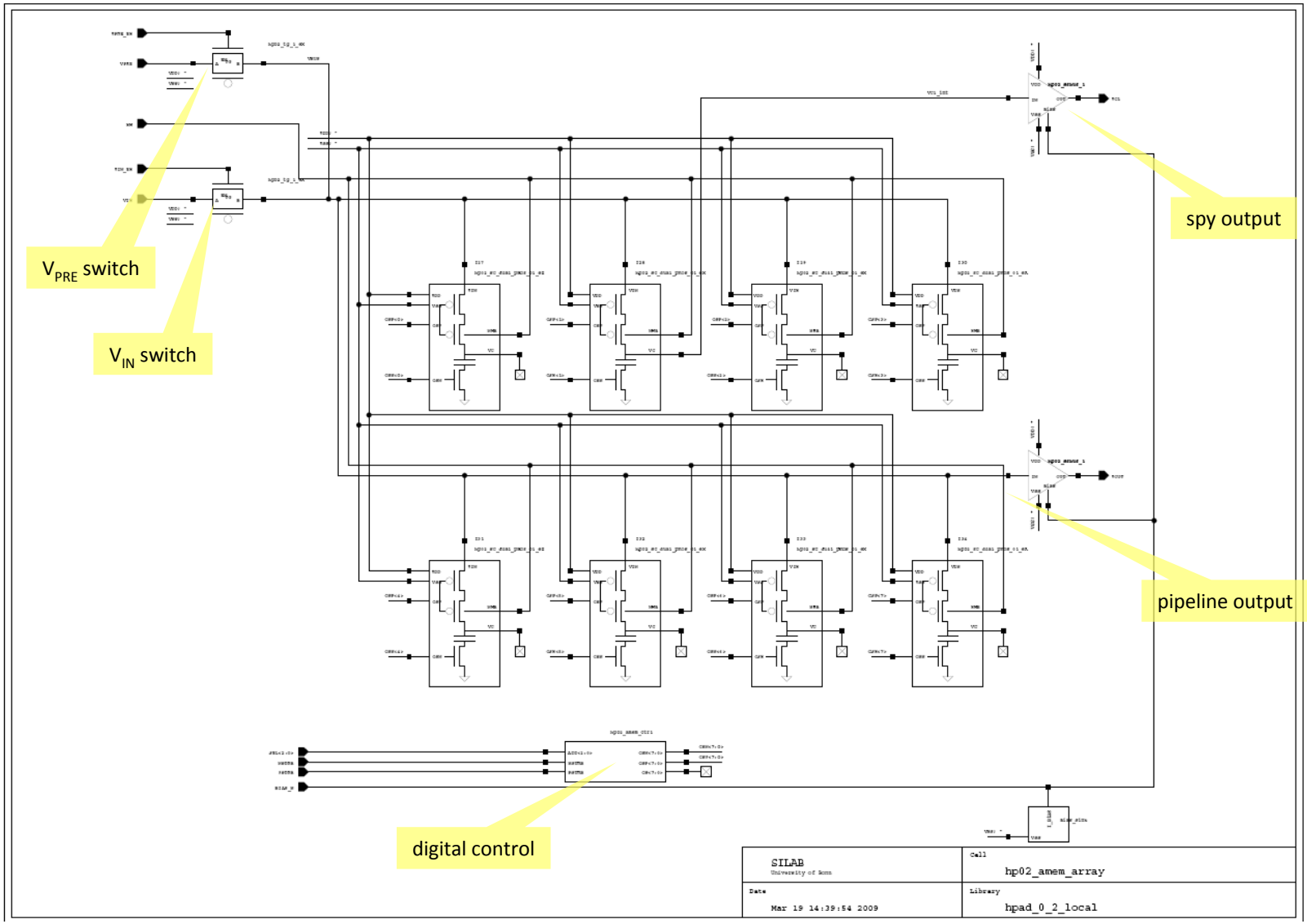
→ add **bottom plate switch**

- Write sequence
  - insert delay between top- and bottom plate switch off transition (switch off bottom first)

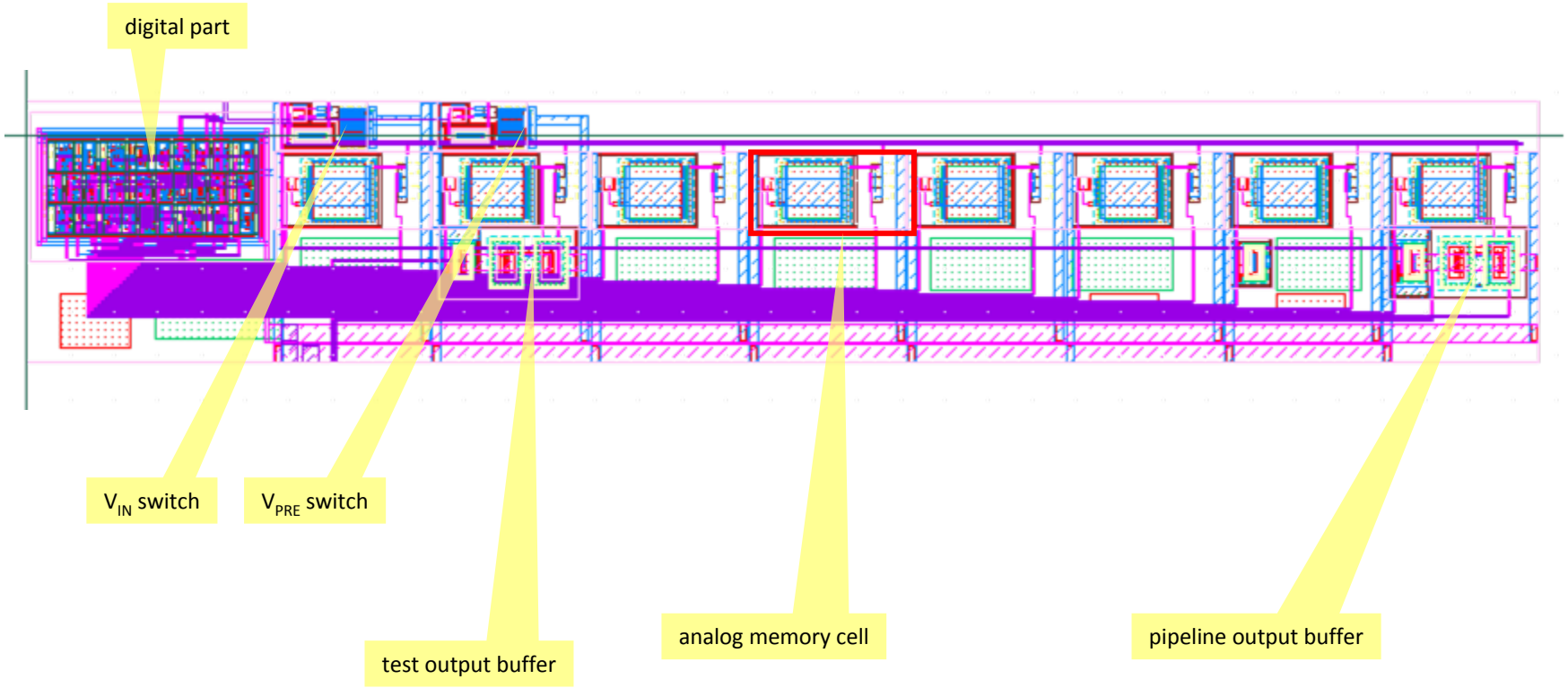
- Read sequence
  - switch bus line to fixed potential (pre-charge V_{PRE})
  - switch on top plate first

- KT/C noise (C_s = 200 fF): $Vn_{kT/C}$ = 100 µV

8-Cell Analog Pipeline Test Structure



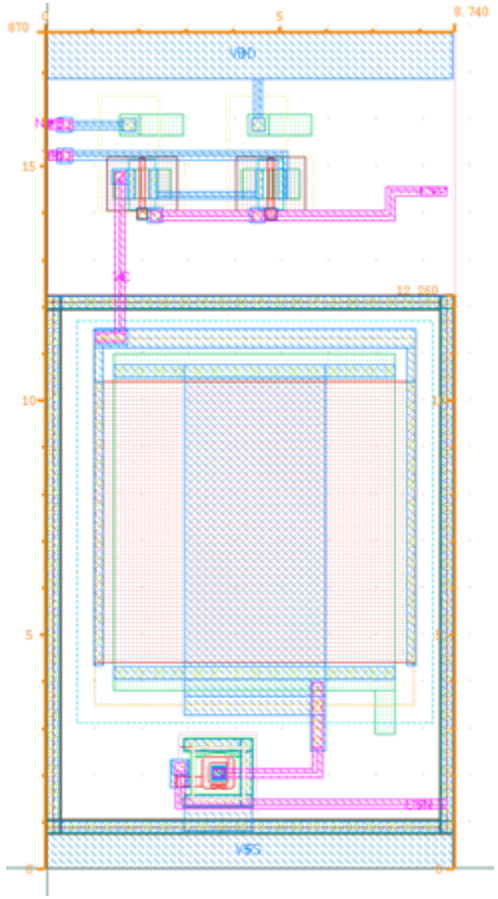
Analog Pipeline Test Structure - Layout



Analog Memory Cell – Layout Issues

Not area optimized!

- 200fF capacitance (6µ · 6µ *DGNCAP)*
- dual linear top plate switch (*PFET*)
- single enclosed bottom plate switch (*NFET*)



Estimation for optimized layout

- with *DGNCAP (~10fF/µm²):*
  - 10µ · 7µ overall
  - 400 cells → (167µm)²
  - need layout area for CSA, dig. control, dig. pipeline, buffer etc…

- with *MIMCAP (4.5fF/µm²)*: 12µ · 8µ (cap only!)
  - still dominated by cap. area
  - no common bottom plate, low density layout rules for MIM layers
  - 400 cells → (195µm)²
  - need to share layout area with C_F !

Analog Pipeline - Modes of Operation

- Write voltage, read voltage
  - voltage follower at the output, easy to implement
  - C_S does not have to be linear (use of *DGNCAP* ok)
  - read: sampled charge re-distributes on bus capacitance C_{PAR} and C_S
  - $C_S >> C_{PAR}$ otherwise signal loss due to capacitive charge division
  - signal division tolerable?

- Write Voltage, read charge
  - CSA as output driver
  - output signal (almost) independent of C_{PAR}
  - needs linear C_S (*MIMCAP*)

- Write Charge, read charge
  - possible but more complicated switching sequence

Preparation of 16 x 16 pixel matrix design

- input dynamic range: $V_{MIN} > V_{THR}$ (~0,5V, low power pmos switch)
- pixel driver: voltage buffer or CSA (switched capacitor, differential?)
- digital pipeline → same as analog with smaller capacitor
- digital blocks
  - in-pixel control: memory cell select, write/read clocks
  - pixel selection: row/column select
- number of storage cells
- floorplan!

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Some other Remarks

- A lot of measurement data of the HPAD 0.1 test structures has been produced
  - switch and capacitor arrays →parametric V-I curves
  - still some issues: are they (self) consistent?
  - conclusions?
- What is missing
  - DGNCAP pre- and after irradiation (capacitance and leakage)
  - results from OPA and alternative storage structures
- What about radiation with more realistic dose rates?
- General chip design issues
  - What is the status of the design of a radiation hard standard cell library?
  - What about enhanced pcells fo enclosed fets (with added RX contacts)
  - fix bug in ASSURA extraction for enclosed layouts
  - Does anybody has experience with HERCULES LVS/DRC
- Leakage performance of the non-irradiated switch still not shown
- rad-hard 'zero leakage' switch seem almost impossible → active compensation will help, but needs power and area

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