Vertically Integrated Circuits: Example of an Application to an x-ray Detector

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on behalf of the AGIPD collaboration

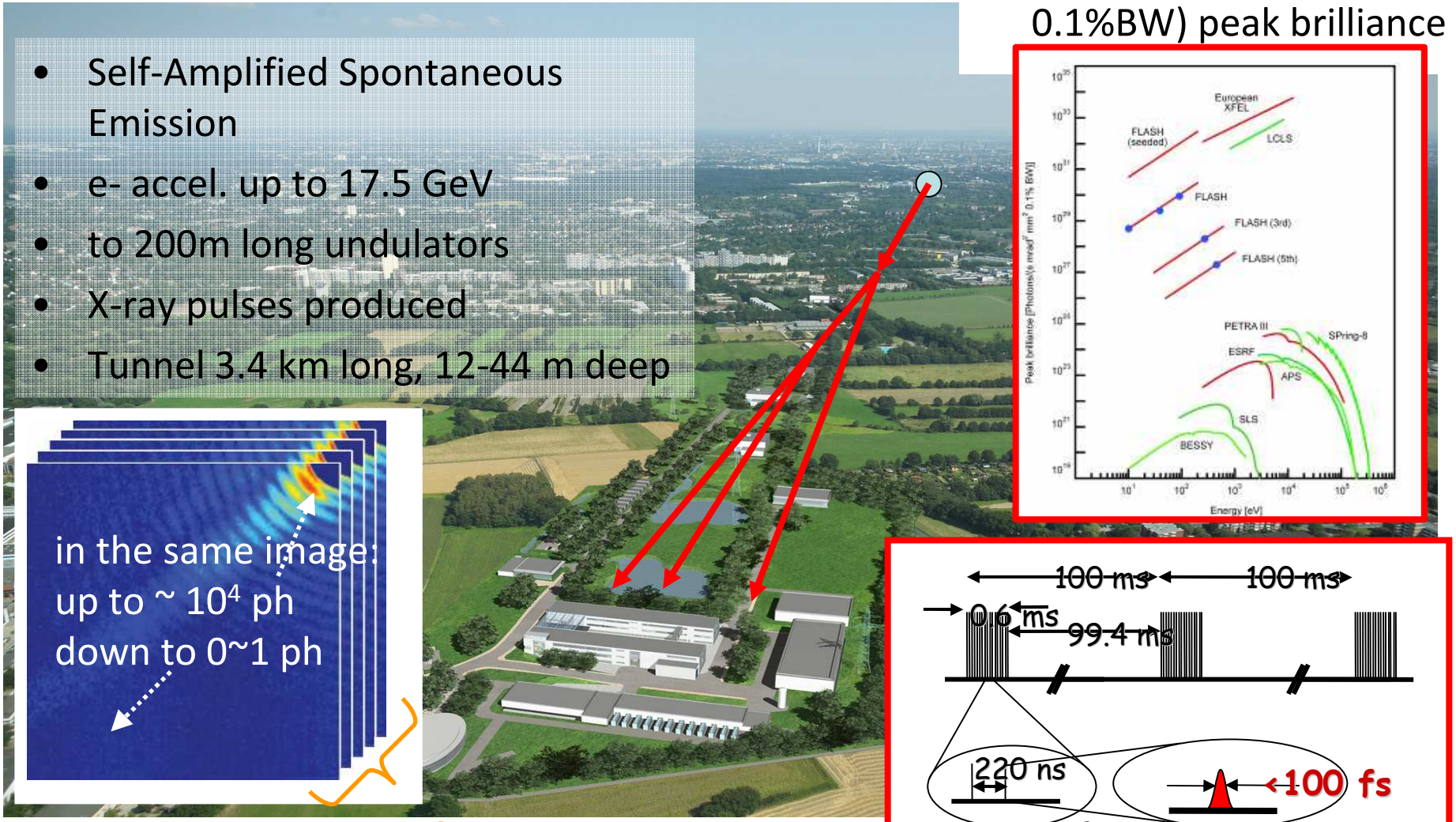
Outline

- The goal and the obstacles to overcome
  - X-ray sensors for advanced FEL
  - Adaptive Gain Integrating Pixel Detector (AGIPD)
  - 3DIC: a possible path to the solution
- design and test of 2-tier detector prototype
  - TSVs & tier-to-tier contacts
  - vertically integrated test circuits, matrix prototype
- Conclusion

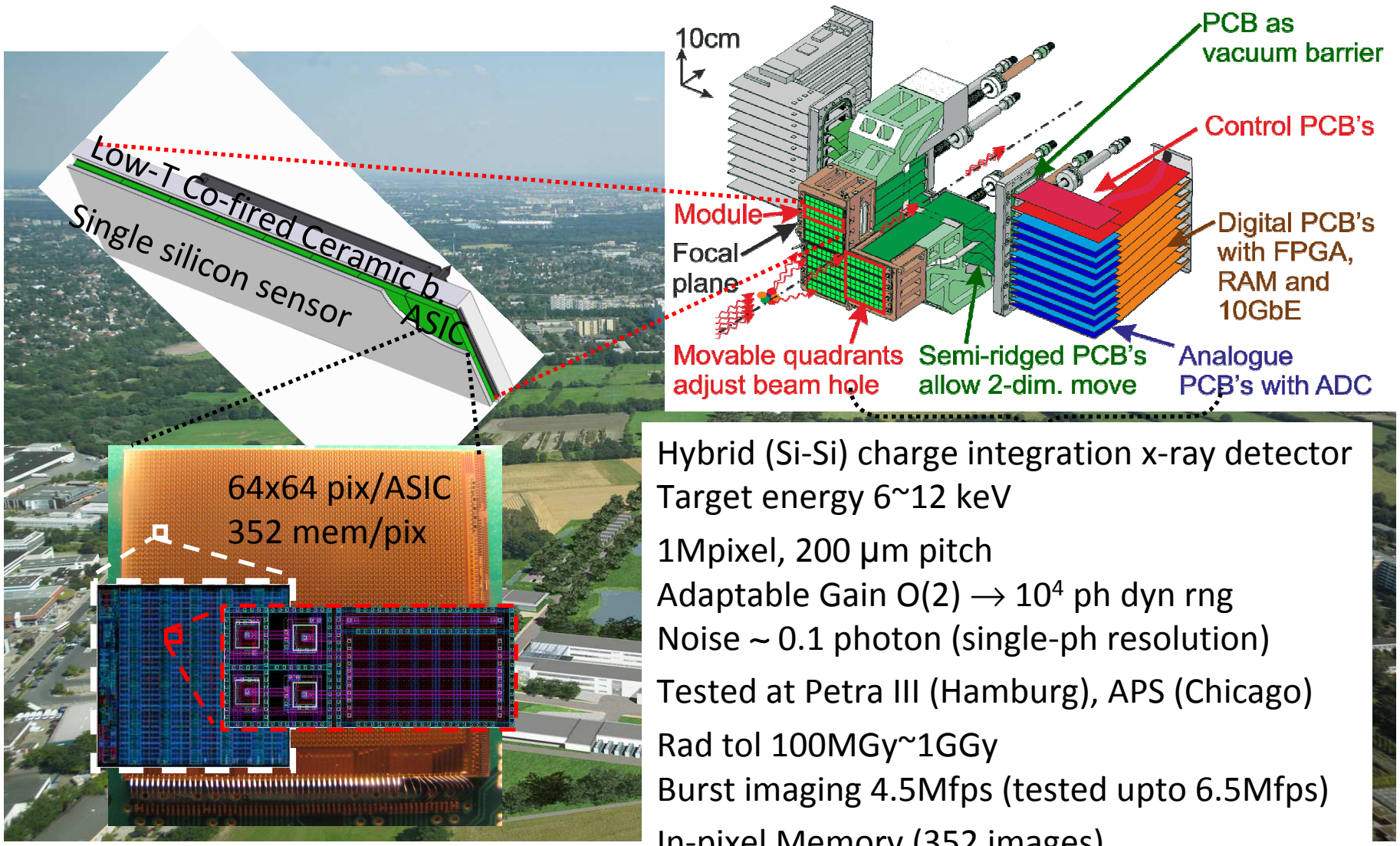
The Motivation

10^{33} ph/(s mm^2 mrad^2 0.1%BW) peak brilliance

- Self-Amplified Spontaneous Emission
- e- accel. up to 17.5 GeV
- to 200m long undulators
- X-ray pulses produced
- Tunnel 3.4 km long, 12-44 m deep



A.G.I.P.D. (2D)



Hybrid (Si-Si) charge integration x-ray detector
Target energy 6~12 keV

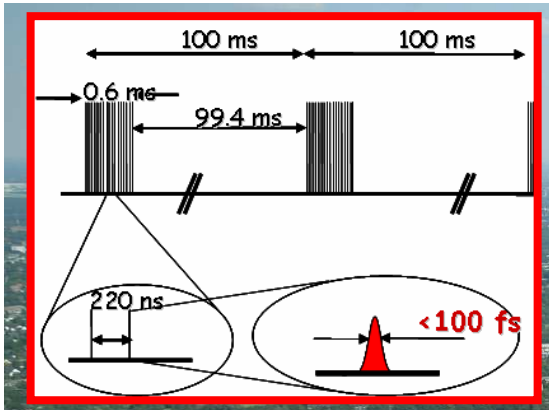
1Mpixel, 200 µm pitch
Adaptable Gain O(2) $\rightarrow 10^4$ ph dyn rng
Noise ~ 0.1 photon (single-ph resolution)

Tested at Petra III (Hamburg), APS (Chicago)

Rad tol 100MGy~1GGy
Burst imaging 4.5Mfps (tested upto 6.5Mfps)

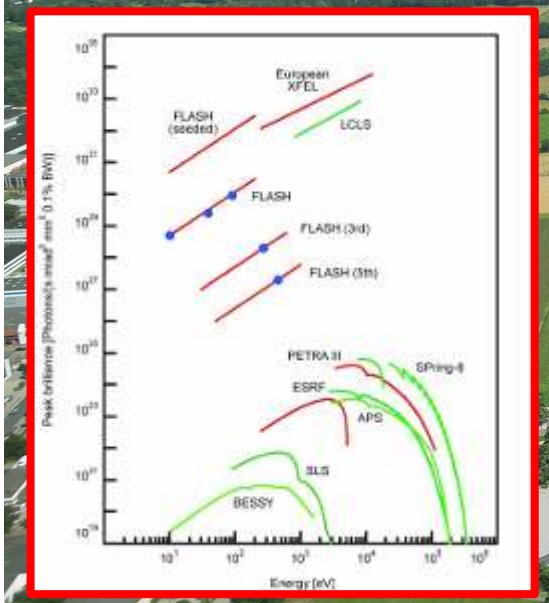
In-pixel Memory (352 images)

but still...



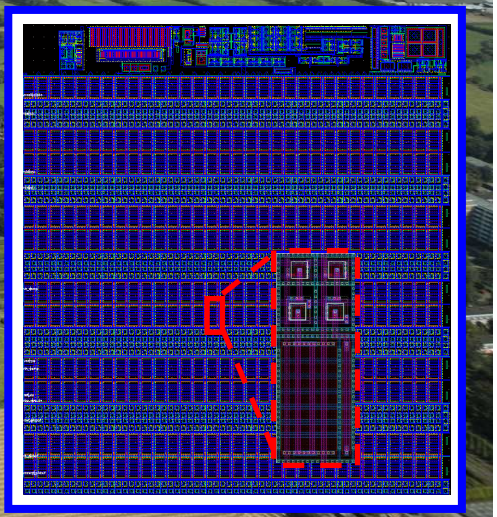
2700 pulses @4.5MHz every 100ms

352 images storing capability



challenging radiation environment

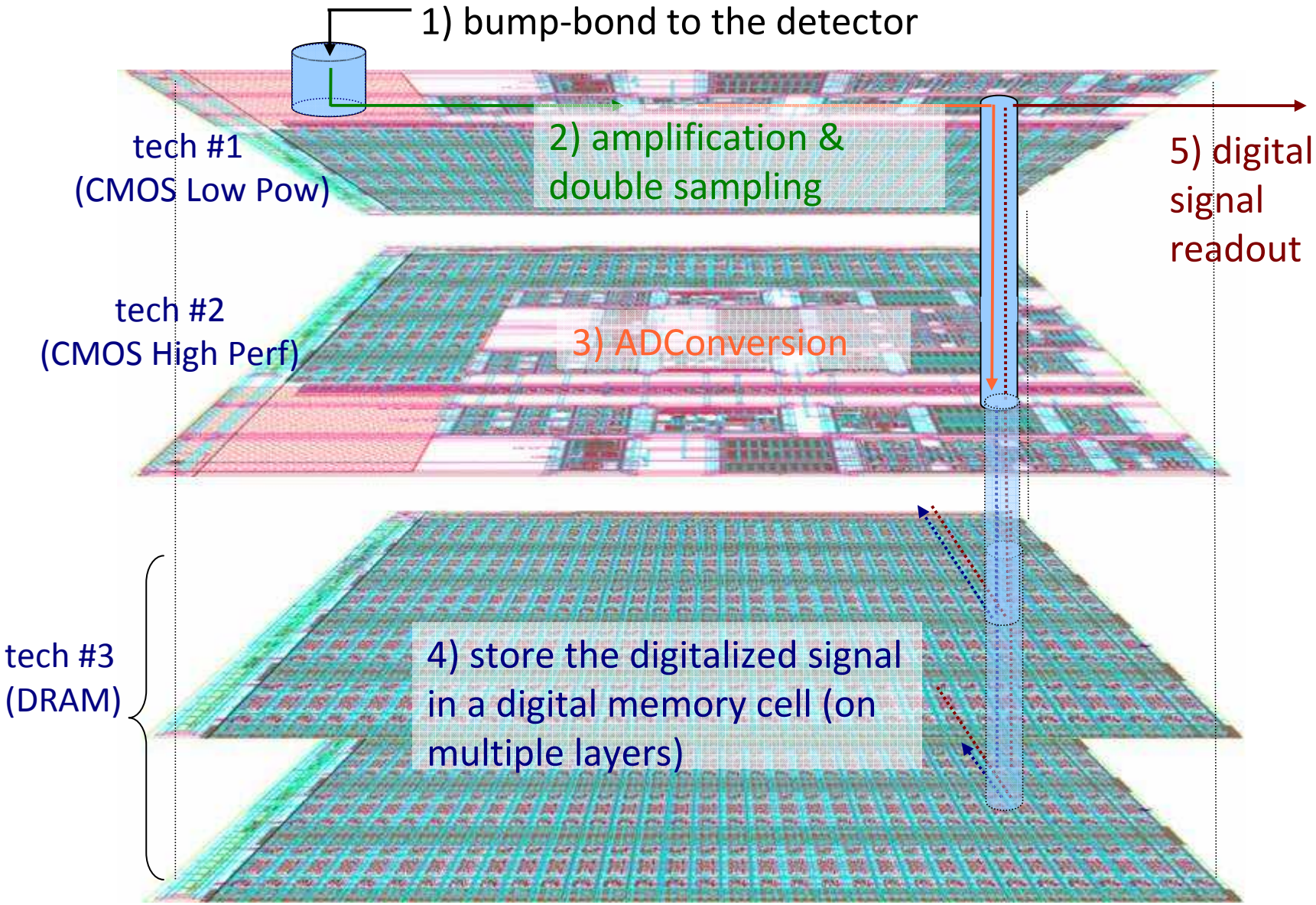
rad tolerant design mandatory



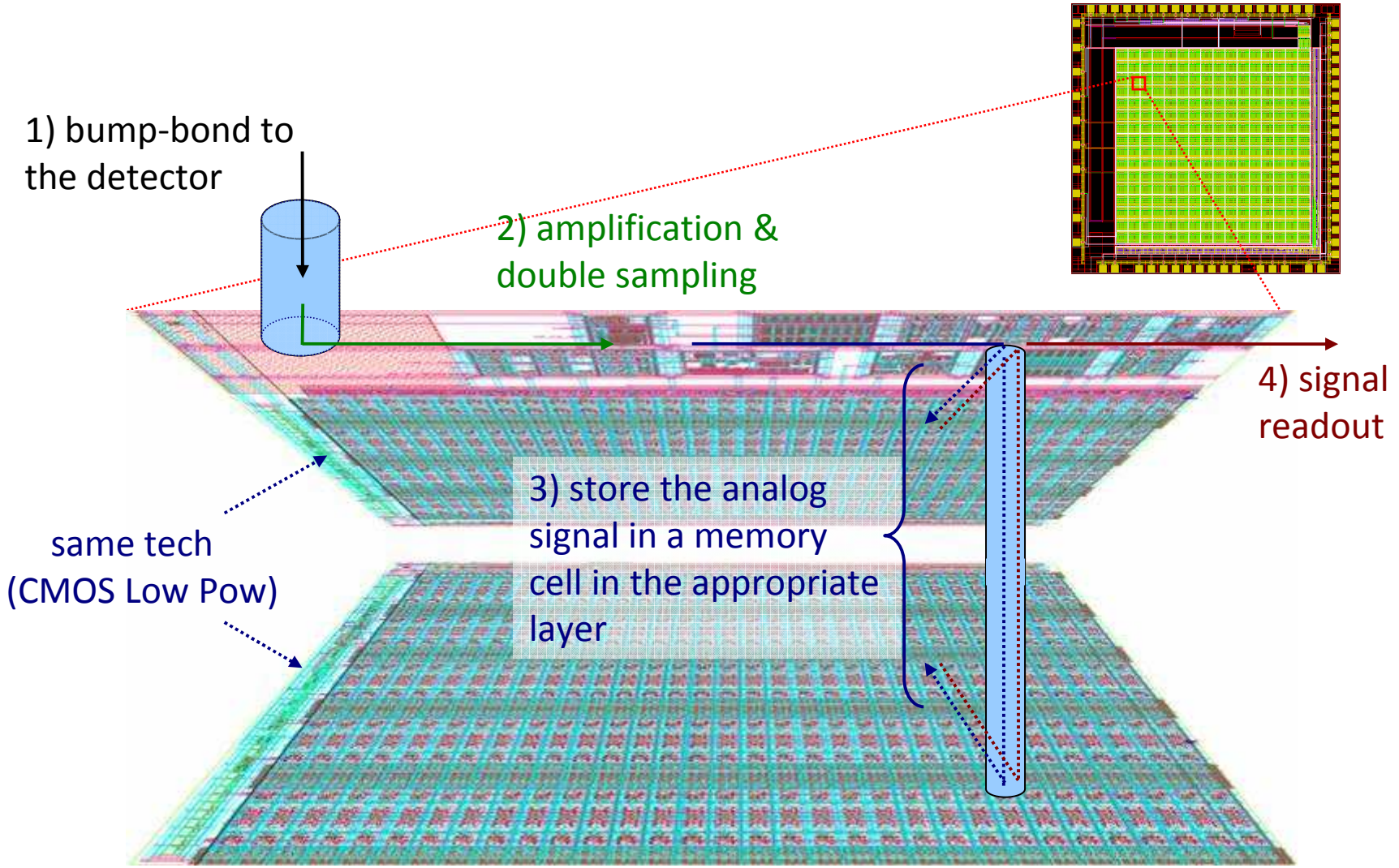
spatial resolution desiderata

200um pitch

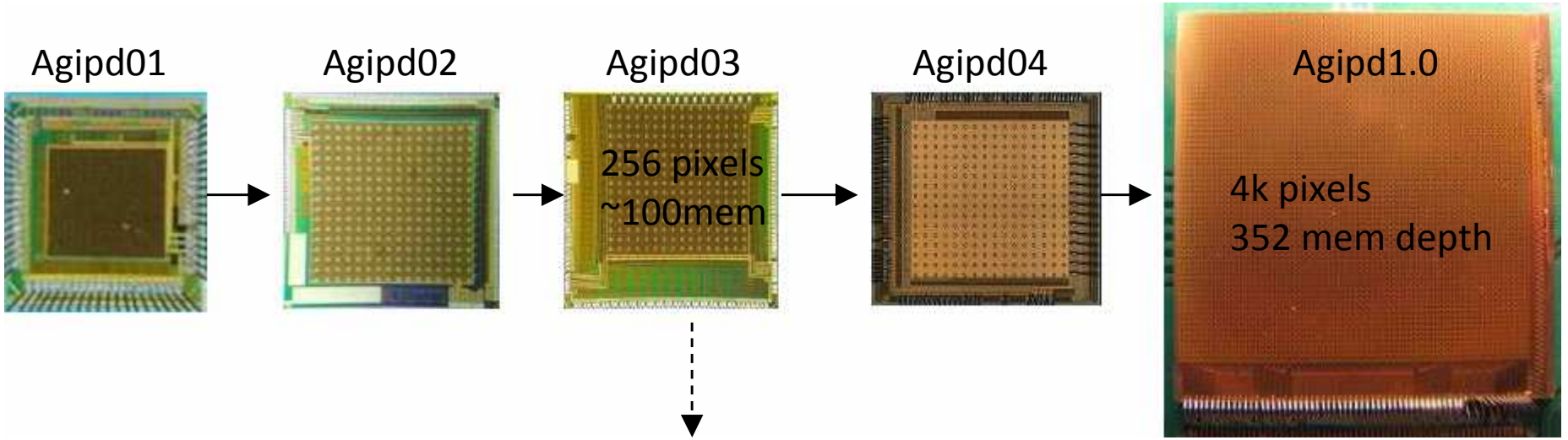
A possible solution (long term goal)



The first step

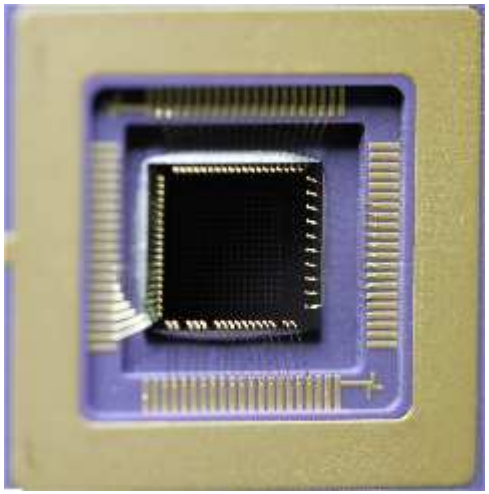


A path toward the solution



GF 130nm CMOS Low Power
ARM SC library
Tezzaron FaStack
double-tier

T13C11 MPWrun, via CMP
submitted 2011
delivered Jan 2014



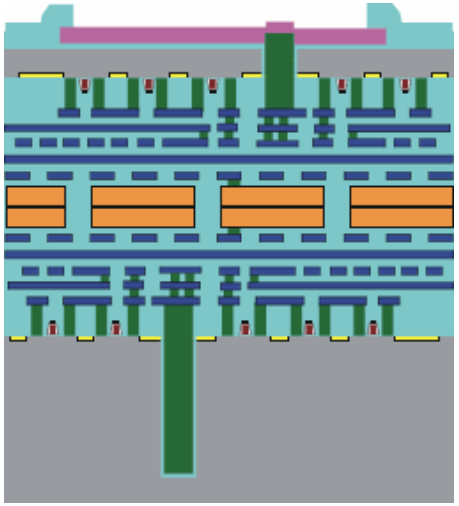
3D-AGIPD0

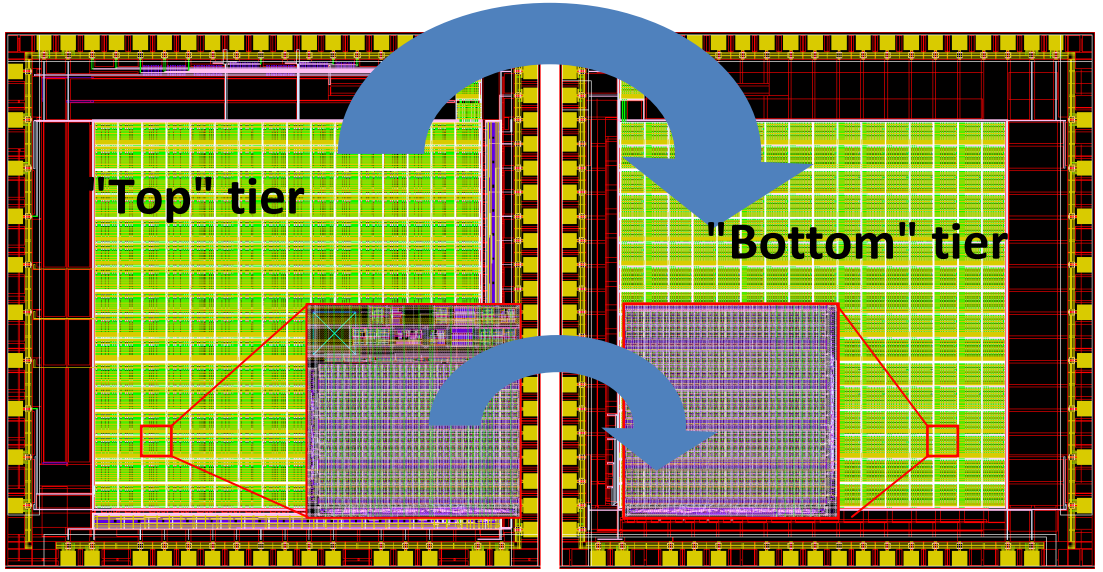
test structures +
256 pixels matrix
200um pitch
544 mem depth

simplified architecture: fixed gain (but reserving the space for multiple-gain circuits; equivalent memcell area)

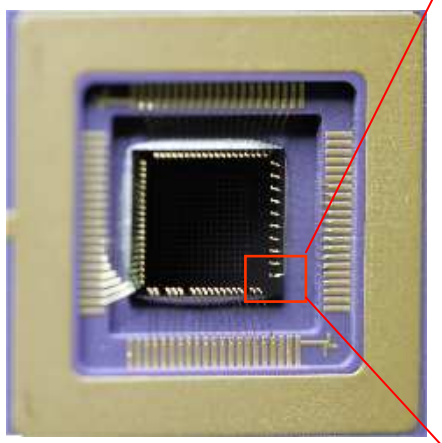
The process at a glance

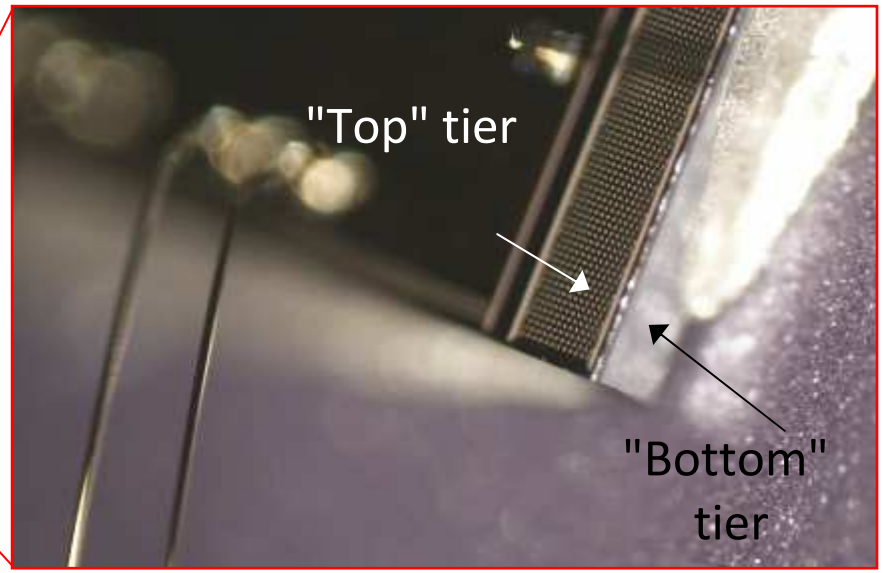
Tezzaron process used



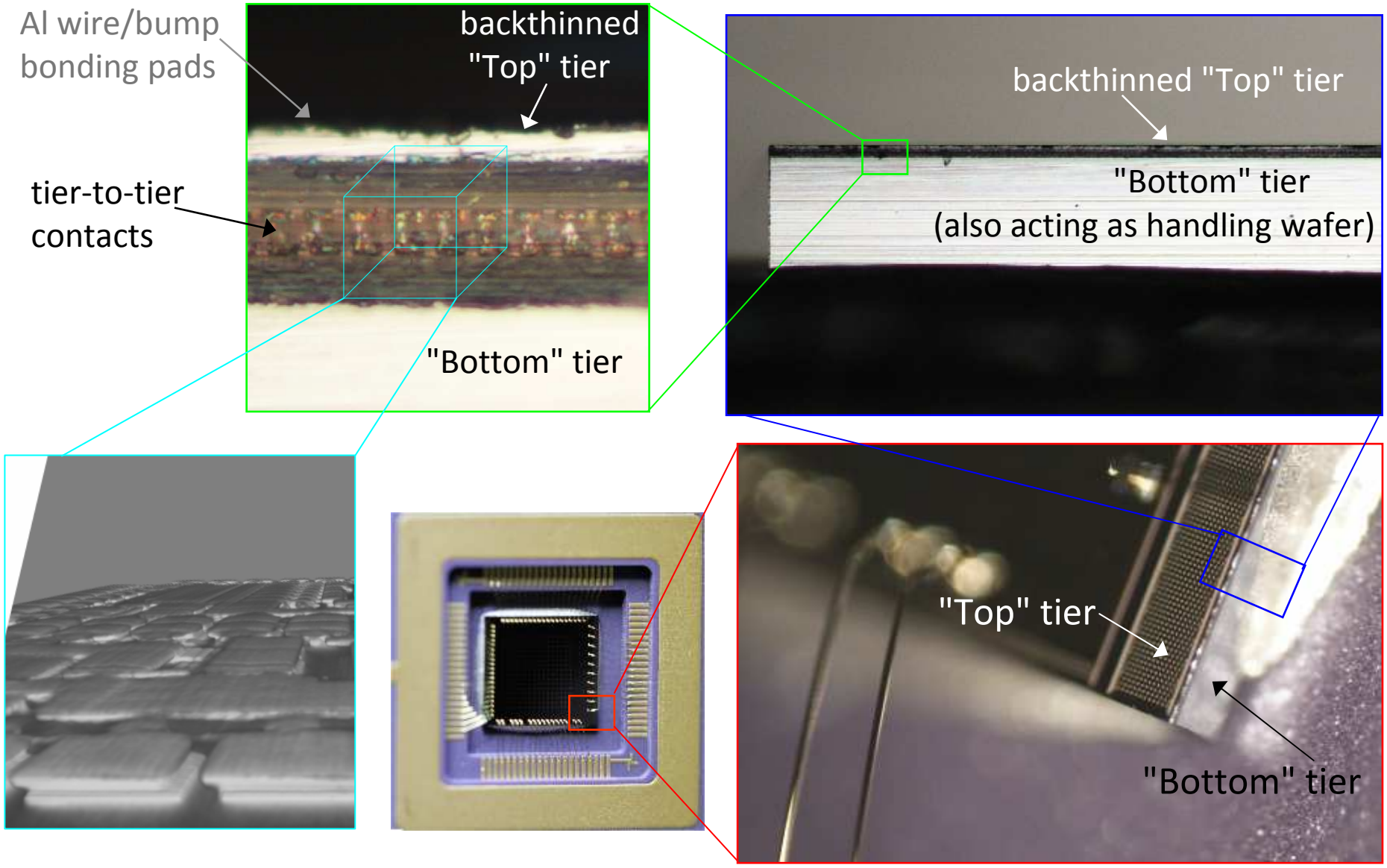


- 2x planar chip manufacture
  - via-middle TSVs
- stacking and face-to-face coupling
- back-grinding of the top tier and exposition of the TSVs
- Pad definition

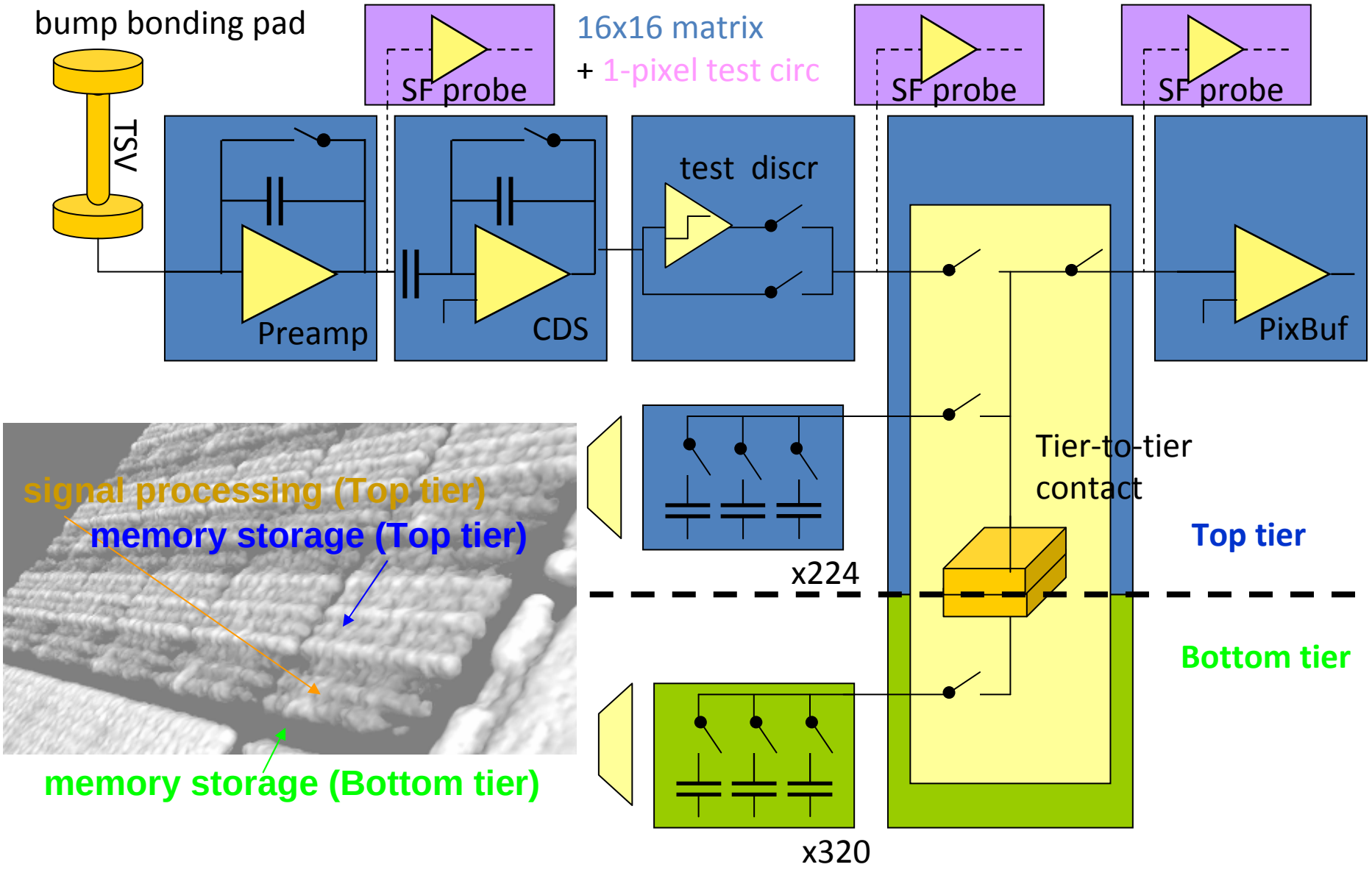




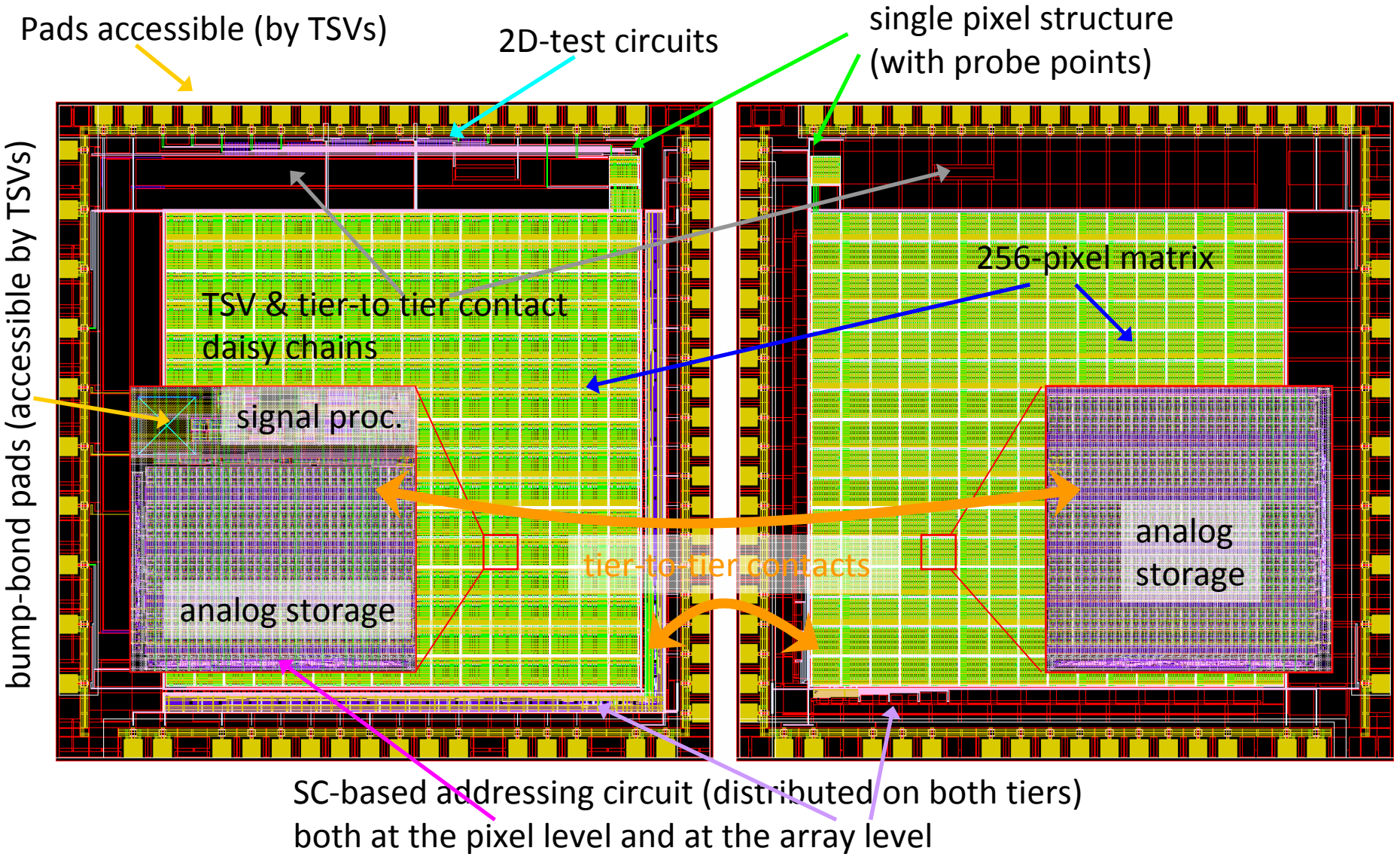
The process at a glance



pixel architecture



chip architecture

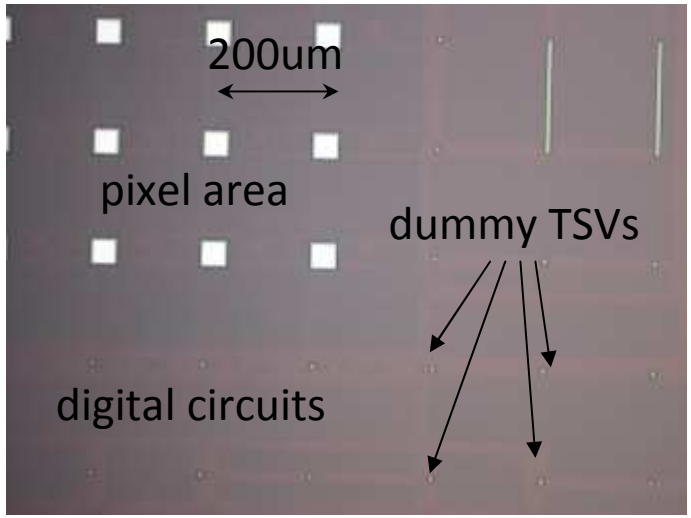


TSV contacts evaluation

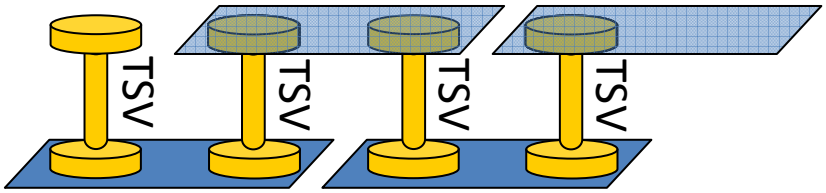
"via middle" TSVs Ø 1.2 um , landing on M1

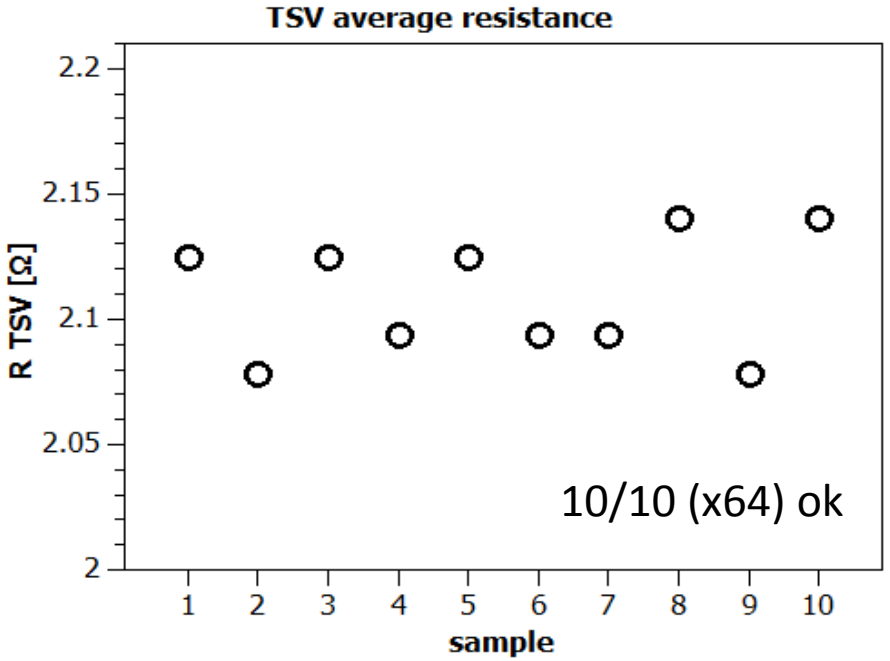
locally: TSV-to-TSV distance down to ~4um
however, globally: "uniform" density of TSVs recommended (→ uniform resistance to grinding)

→ designer constraint: dummy TSVs



10x test structure for TSV evaluation: daisy chain of 64 TSVs, by connected M1/backM.





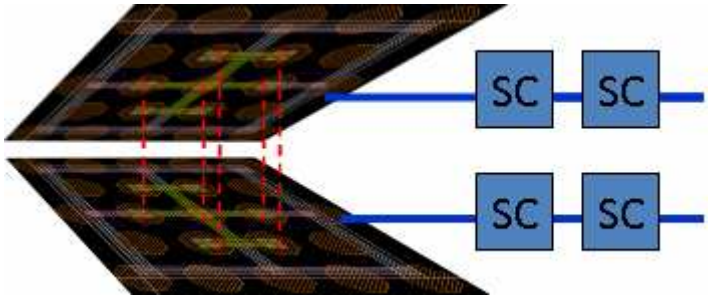
measured on 10 packaged samples
no broken chain, avg R 2.1Ω /TSV

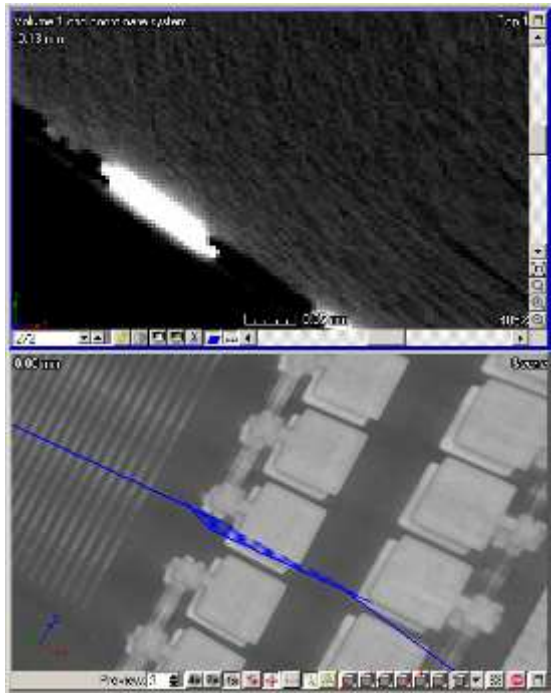
Tier-to-tier contacts

Cu-bondpoints (M6) used for tier-to-tier connectivity

approach adopted

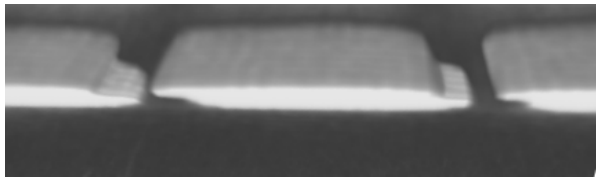
- partition of the behavioural in TOP/BOTTOM
- definition of a "tier-to-tier contact" SC compatible with bondpoint array
- floorplan
- pre-placement of tier-to-tier contact cells
- P&R of regular cells
- ...





M^3APS (courtesy of INFN-Perugia)
submitted end 2009
Tomography by F. Beckmann (DESY)

tier-to-tier contact redundancy was suggested by 2009 MPW experience, to counter eventual tier misalignment

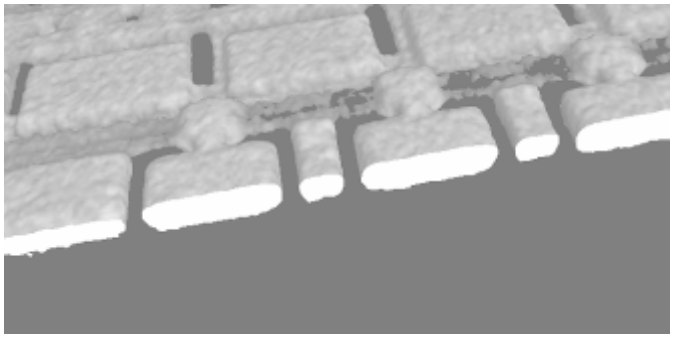


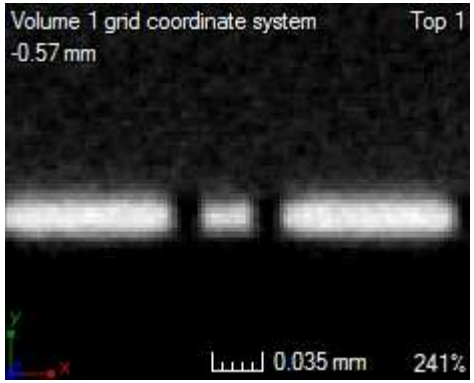
however ...

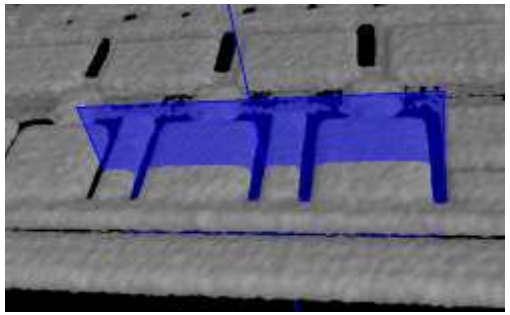
Tier-to-tier contact evaluation

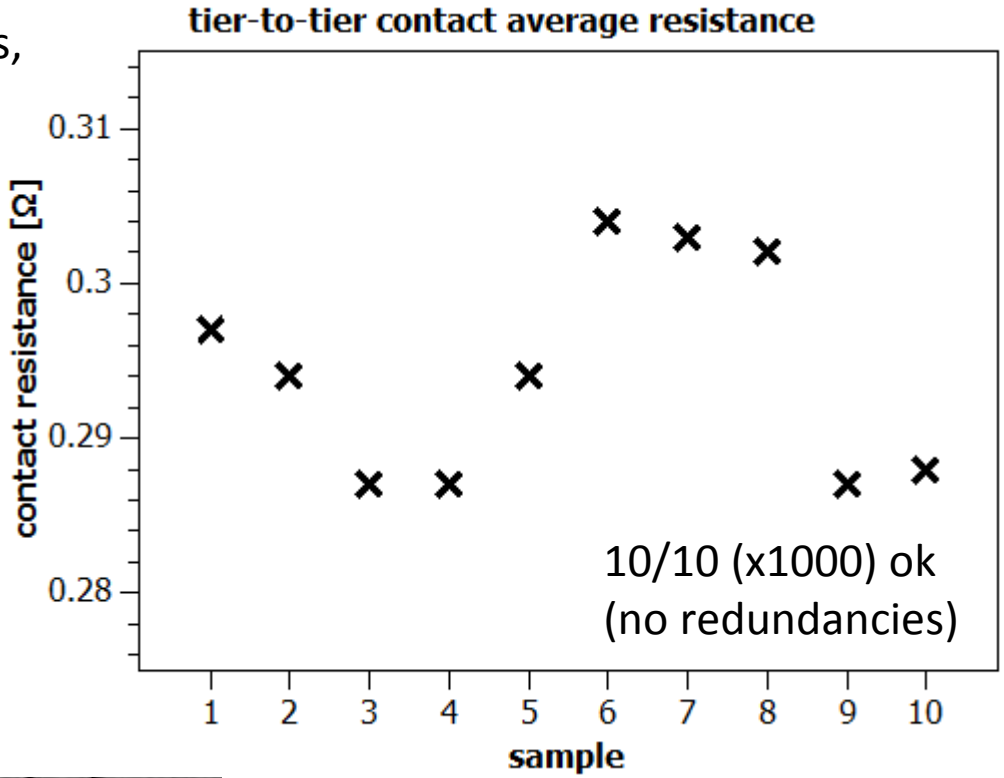
10x test structure for contact evaluation:
daisy chain of 1000 tier-to-tier contacts,
connected in series using M5.

measured independently
on 10 packaged samples
no broken chain



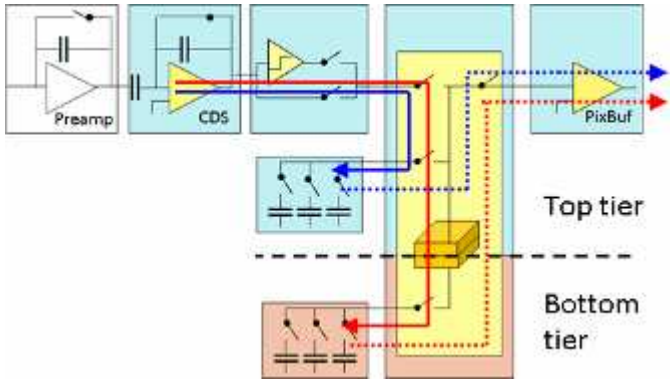






x-ray tomography (F. Beckmann, DESY) also suggest better alignment

Pixel matrix write-read example

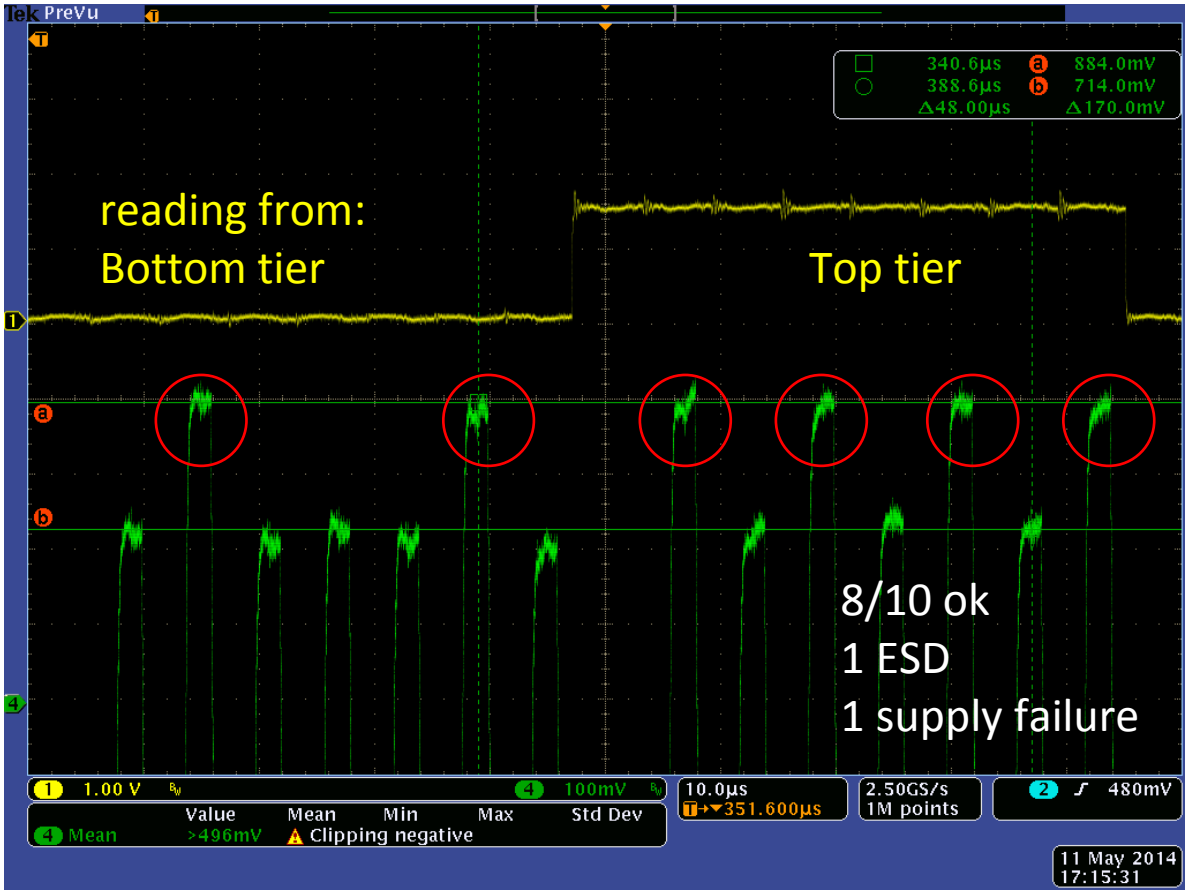


precharge cells

write a (different from precharge) voltage on Bottom tier cells 2,6

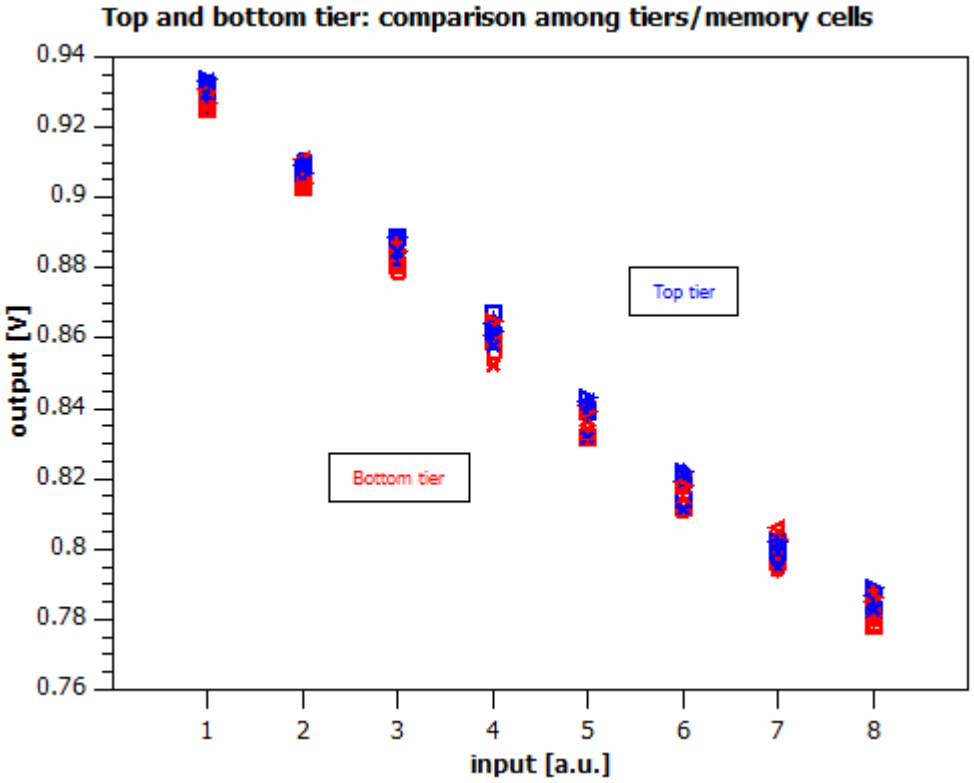
write a (different from precharge) voltage on Top tier cells 1,3,5,7

sequentially read memcells on a sample pixel:

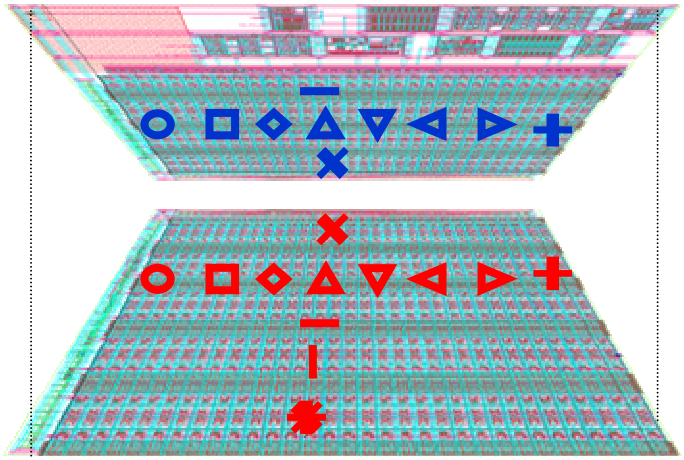


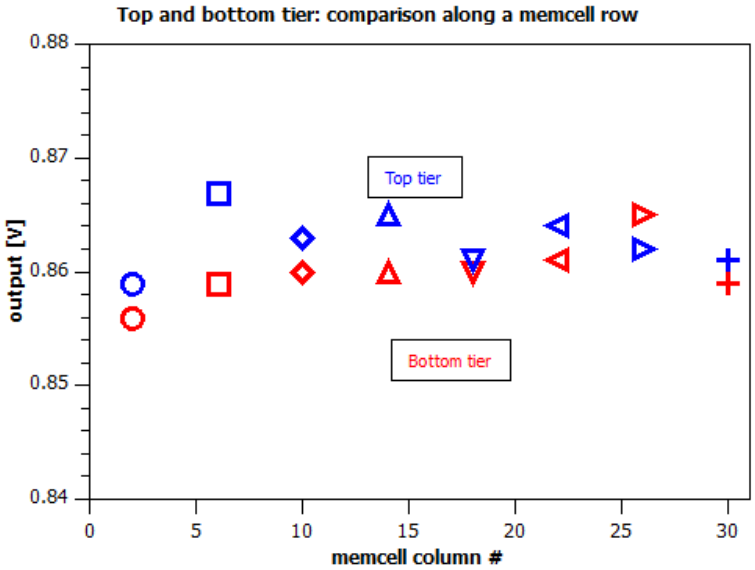
Bottom,1 Bottom,2 Bottom,3 Bottom,4 Bottom,5 Bottom,6 Bottom,7 Top,1 Top,2 Top,3 Top,4 Top,5 Top,6 Top,7

Top/Bottom tier: memory cell-to-memory cell variations



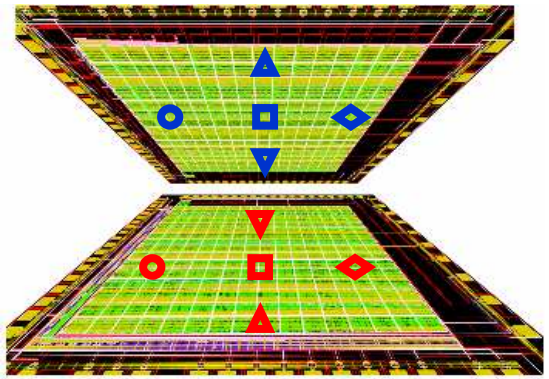
1 pixel in the array



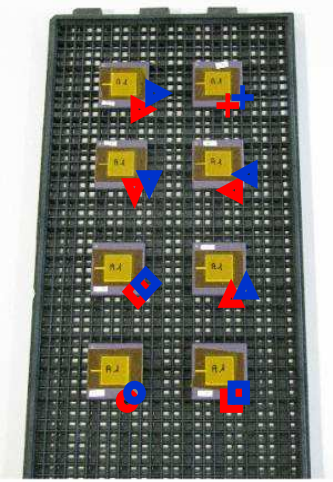


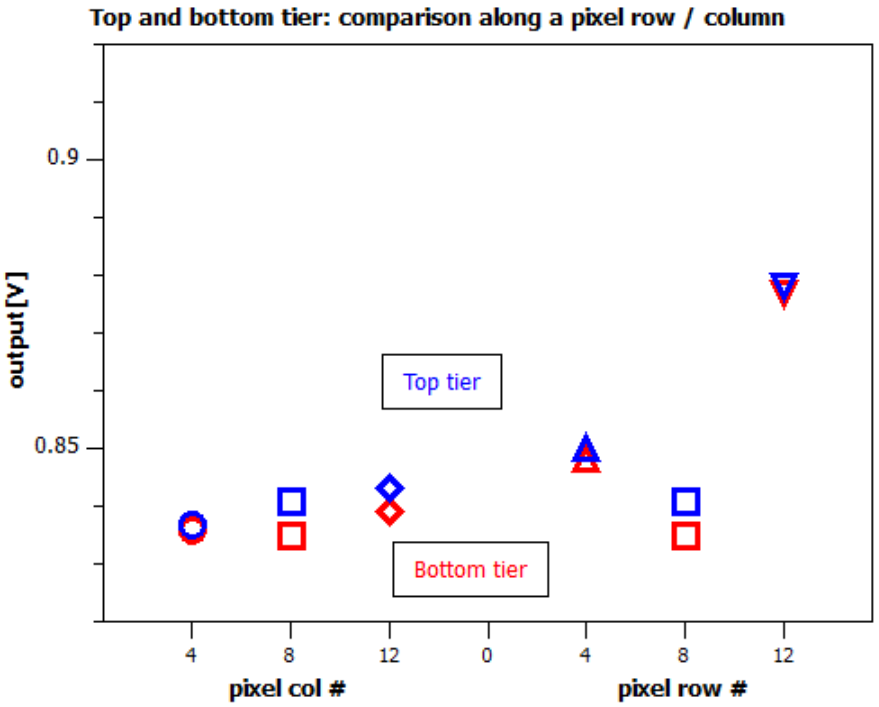
Comparable (linear) detector response
- for charge stored in either in Top/Bottom tier
- for different memory cells in the same pixel,
independently from their location.
Slight pedestal offset, to be investigated further

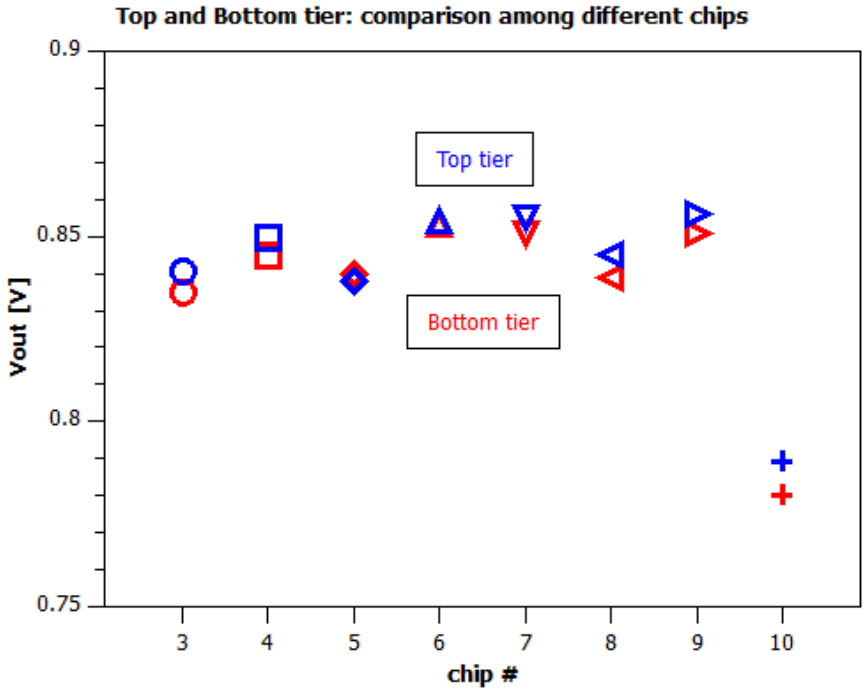
Top/Bottom tier: pixel-to-pixel & chip-to-chip variations



Different pixels/samples: slightly higher variations. However, outputs from memory cells in the Top/Bottom tier of the same pixel remain similar.
Process parameter dispersion in the active pixel circuitry is suspected.
Per-pixel calibration in any case needed.







Conclusions and future work

Extending photon science detectors in the third dimension:

- the 3D-AGIPD case

Prototype produced: T13C11 3DIC MPW run (through CMP)

- GF130nm tech, Tezzaron 3D-process, 2 tiers, face-to-face
- 256 pixel array (200um, 544 images memory depth) + test structures

First evaluations

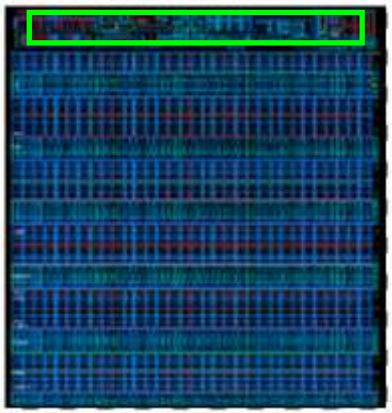
- good TSV, tier-to-tier contact characteristics (10/10)
- 8/10 samples with pixel array working as expected
- able to store/recover info both Top/Bottom tiers

Future work:

- design of improved prototype
- investigation/mitigation of performance dispersion
- investigation of storage cell leakage & rad tolerance of the 3D assembly

Backup

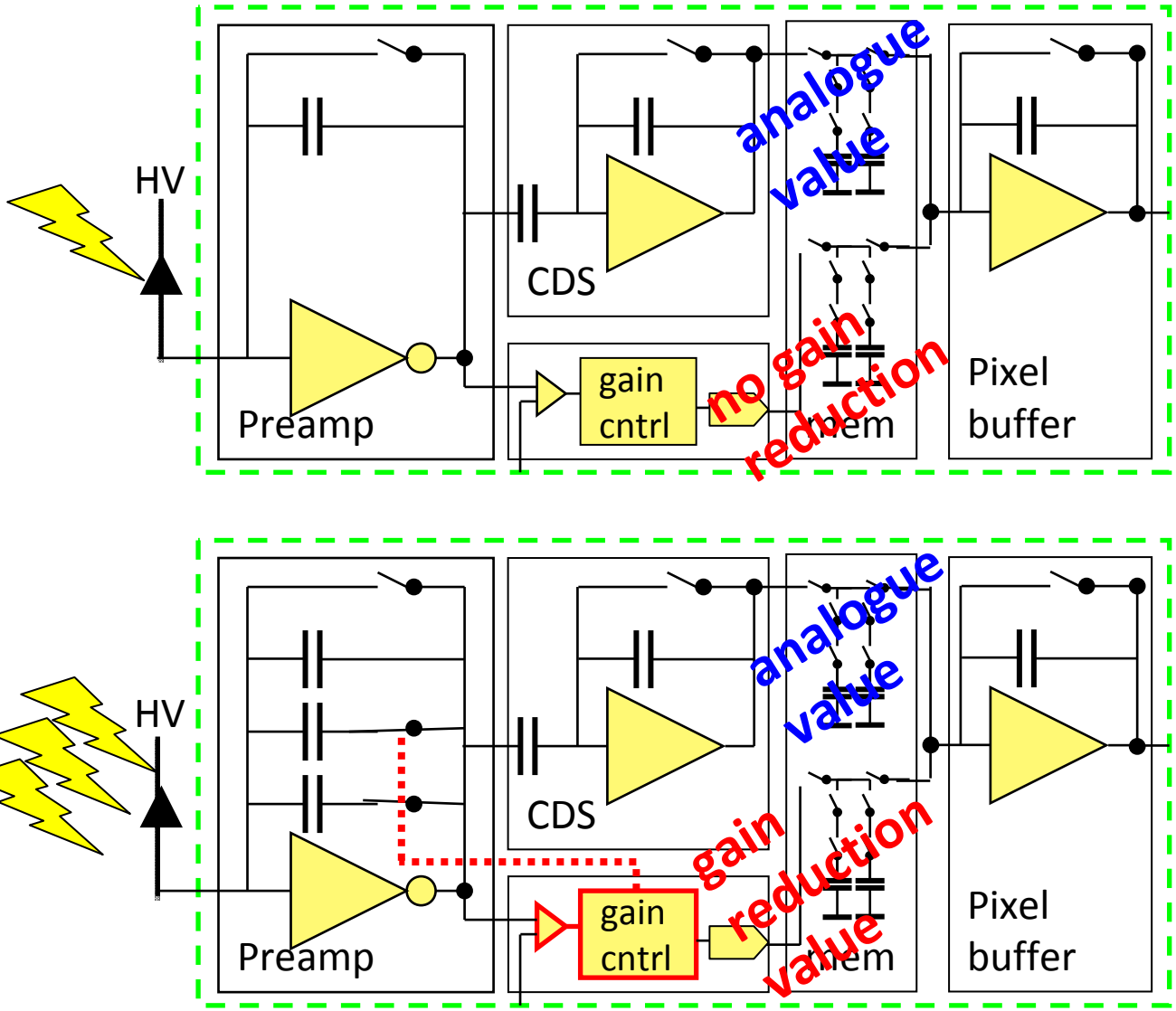
Adaptive Gain Concept



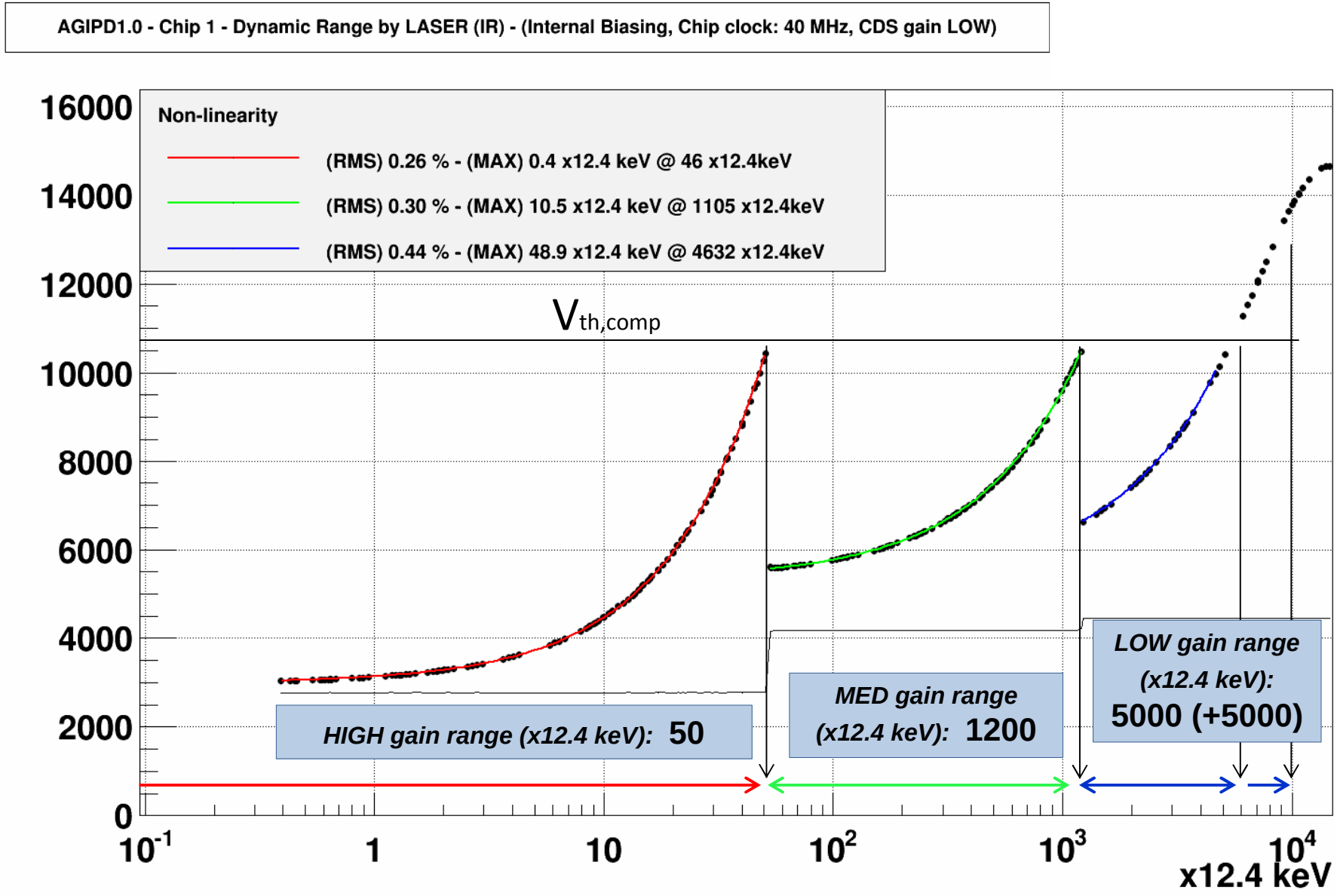
real-time adjustment of the feedback capacitance depending on the photon flux

60fF/3fF/10fF dyn. switching

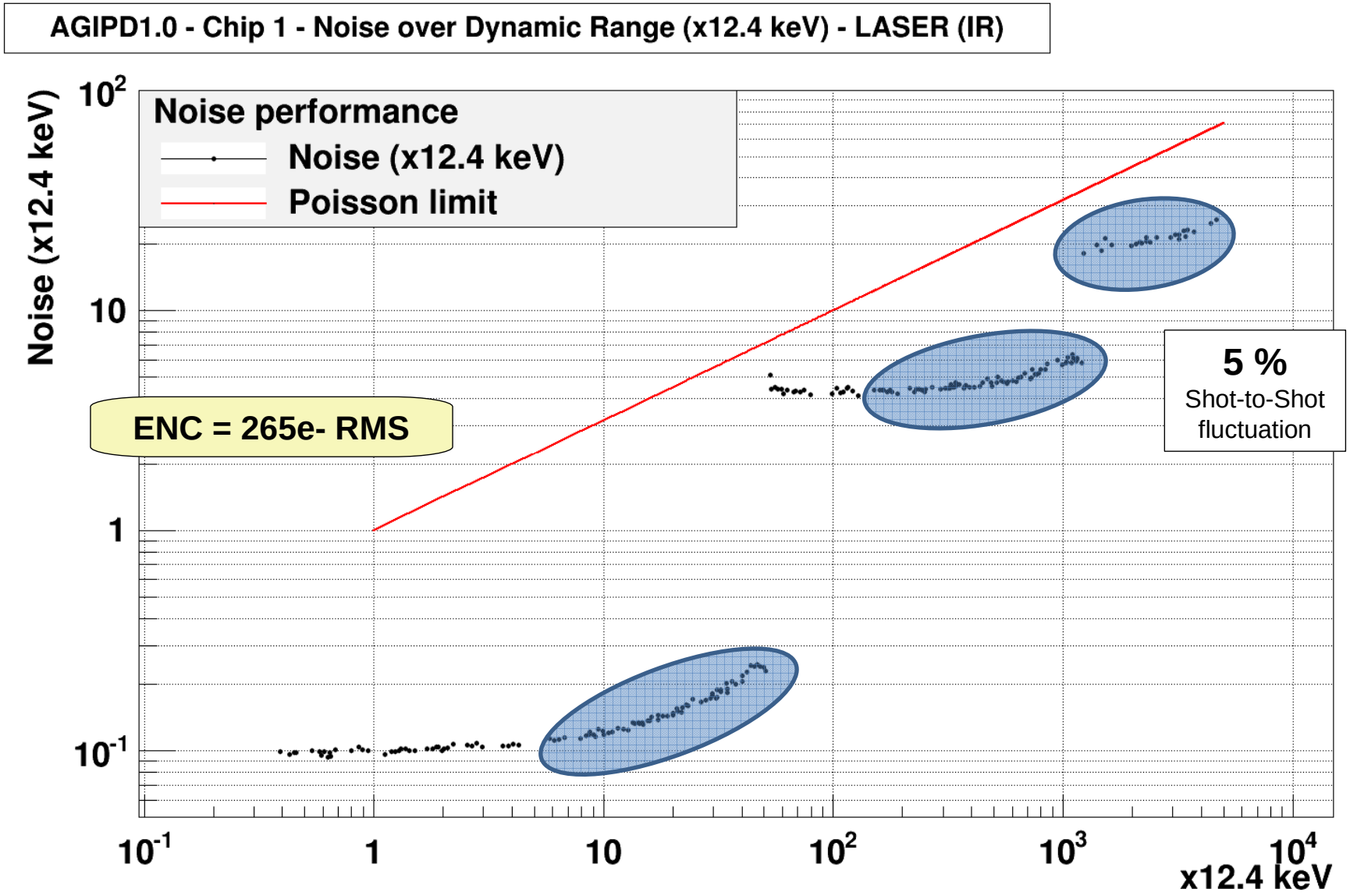
=> adaptable gain O(2)



Multi-Gain Dynamic Range

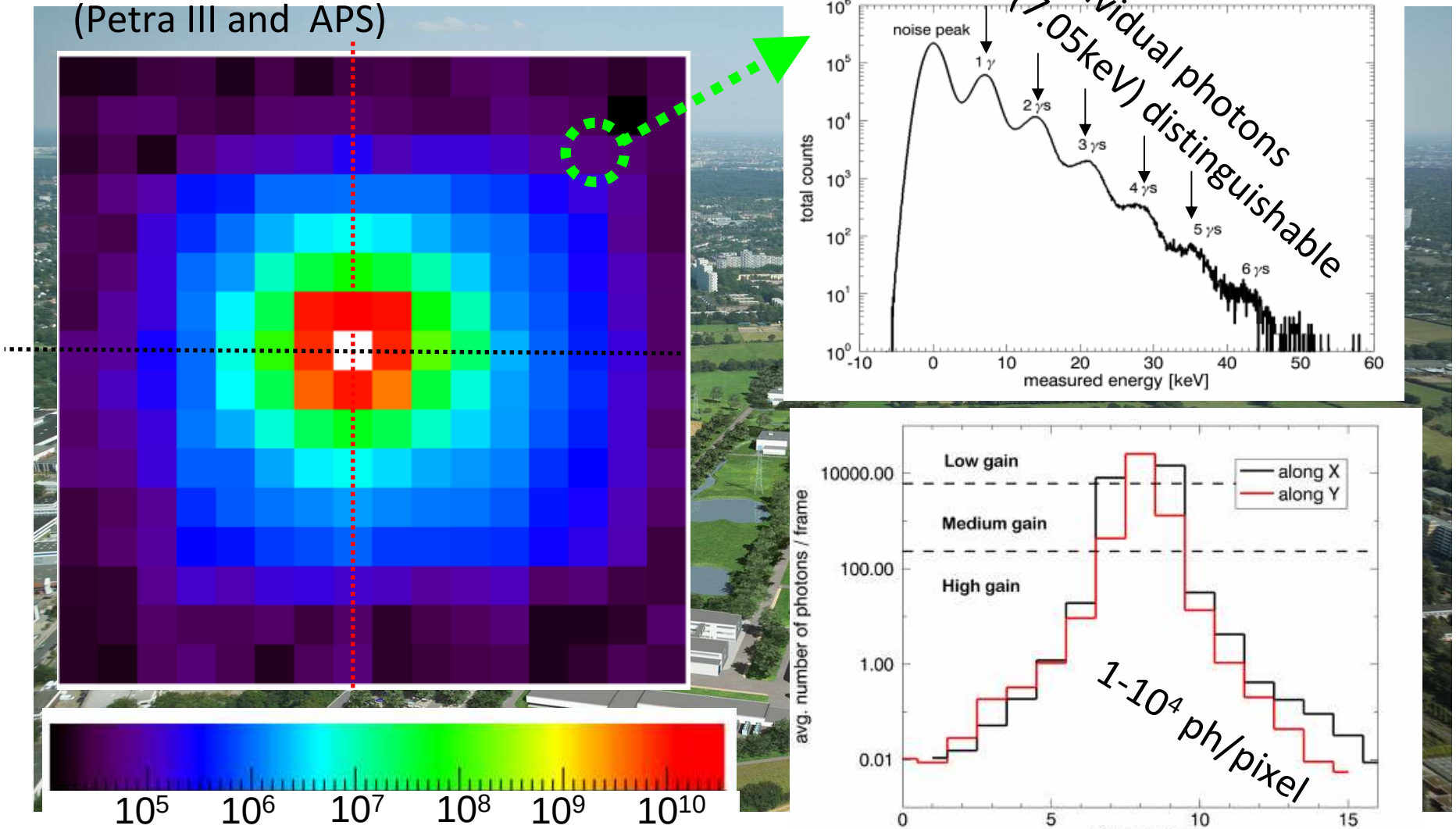


Noise


AGIPD1.0 - Chip 1 - Noise over Dynamic Range (x12.4 keV) - LASER (IR)
Noise performance
Noise (x12.4 keV)
Poisson limit
Noise (x12.4 keV)
ENC = 265e- RMS
5 %
Shot-to-Shot
fluctuation
x12.4 keV

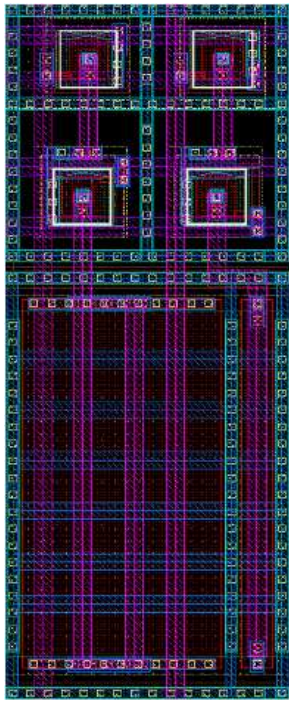
A.G.I.P.D. (2D)

imaging the direct beam of synch rings
(Petra III and APS)

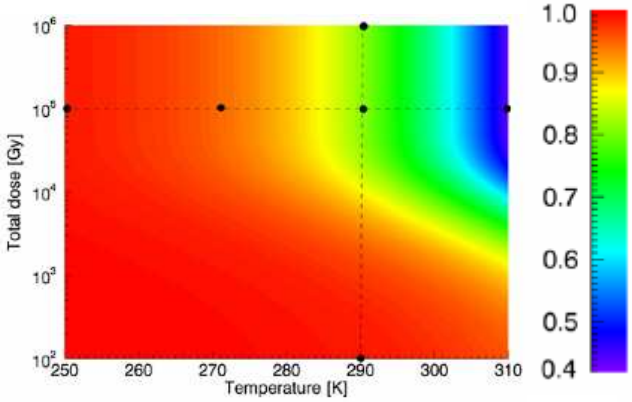


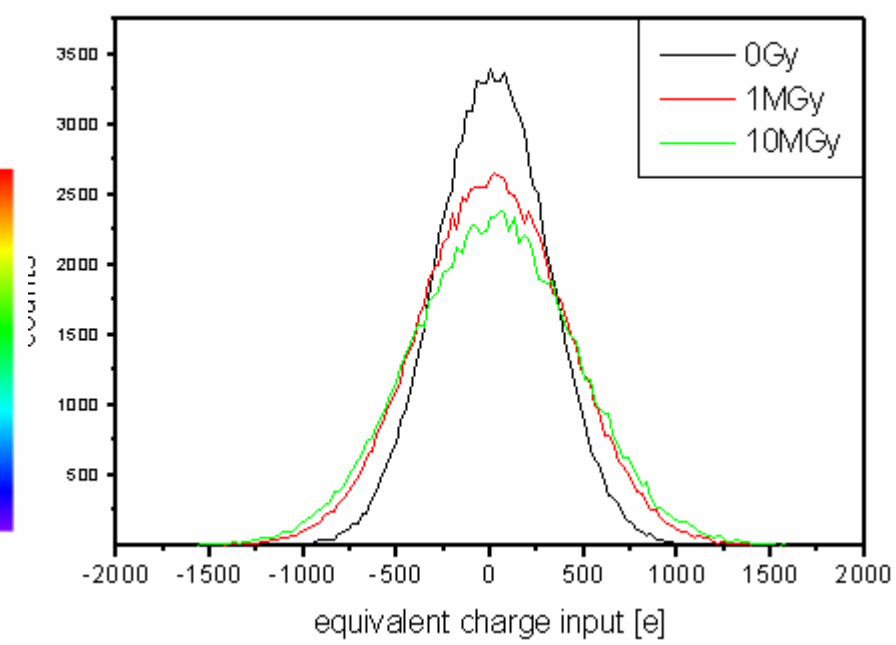
Individual photons
(7.05keV) distinguishable

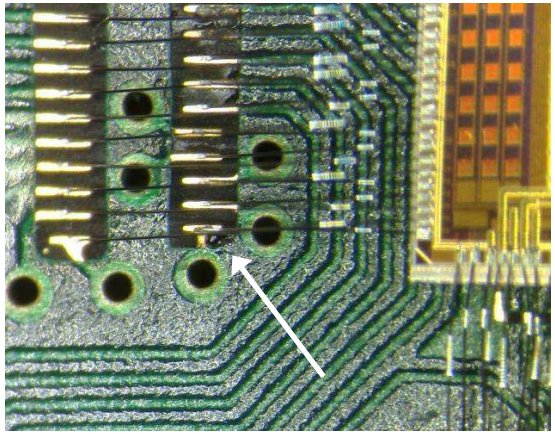
Irradiating AGIPD

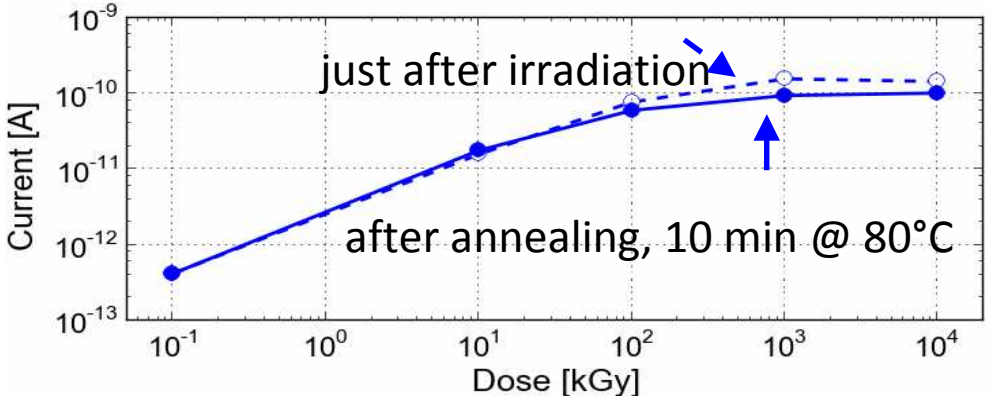


charge left in storage cell

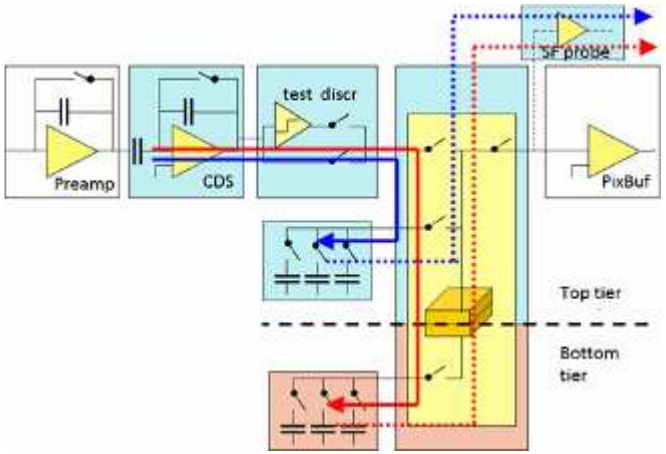








Single pixel write-read example



precharge cells

write a (different from precharge) voltage on Bottom tier cell groups A, C

do the same on Top tier cell group B

connect cell group to memory bus and probe voltage

Bottom tier, cell group A

Bottom tier, cell group B

Bottom tier, cell group C

TOP tier, cell group A

Bottom tier, cell group B

Bottom tier, cell group C

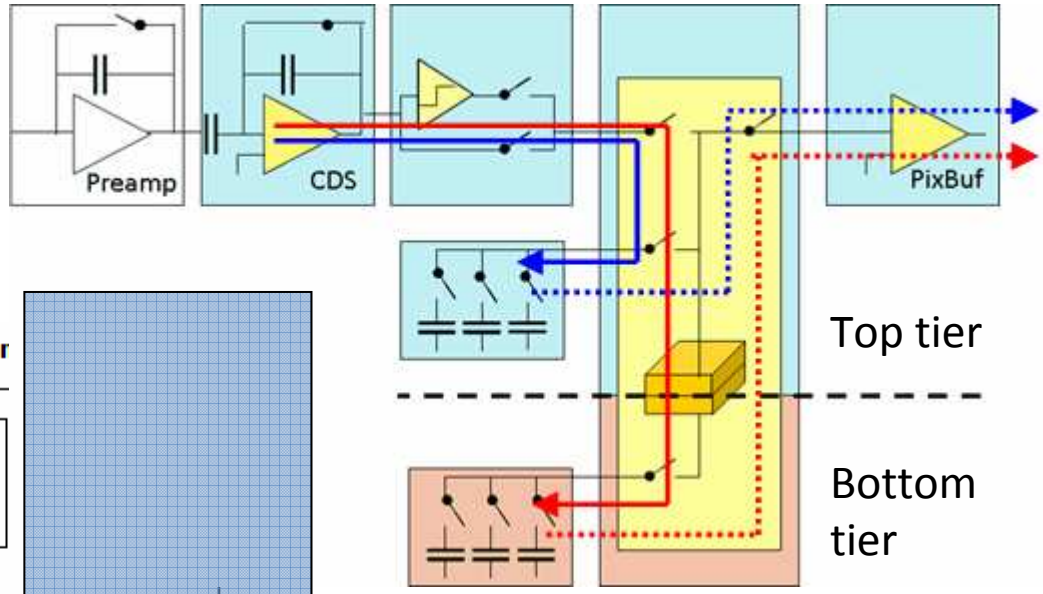
Test summary

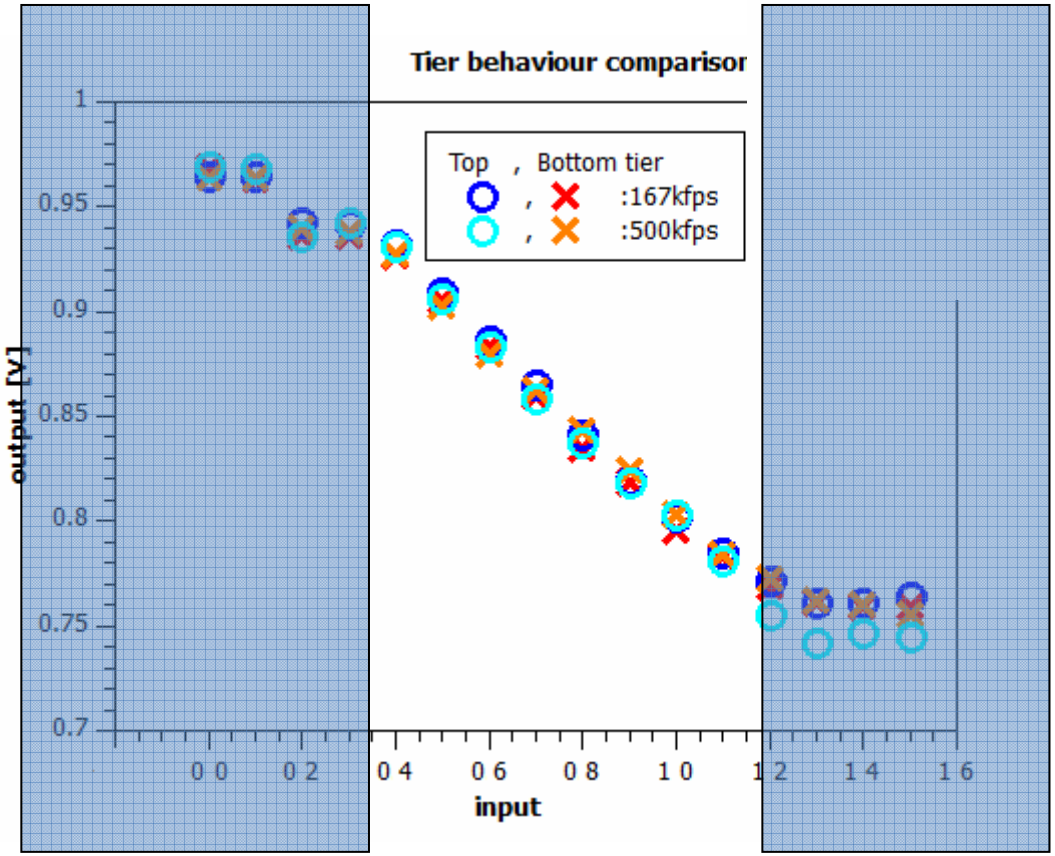
chip #	daisy chains (TSV & tier-to-tier)	2D test circuits	single pixel test struct	16x16 matrix (CDS stage input)	power consumption
	Top&Bottom tier	Top tier	Top&Bottom tier	Top&Bottom tier	
1	unbroken	not responding	not responding	not responding	3.75 mW
2	unbroken	responding	not responding	not responding	24.75 mW
3	unbroken	not responding	responding	responding	31.05 mW
4	unbroken	responding	responding	responding	24.3 mW
5	unbroken	responding	responding	responding	26.25 mW
6	unbroken	responding	responding	responding	30.15 mW
7	unbroken	responding	responding	responding	30.9 mW
8	unbroken	responding	responding	responding	31.2 mW
9	unbroken	responding	responding	responding	26.7 mW
10	unbroken	responding	responding	responding	30.0 mW

as expected	unexpected

Behaviour comparison of Top/Bottom tier storage cells

tested up to 500kfps (limit of current test setup, to be improved for 4.5Mfps test)

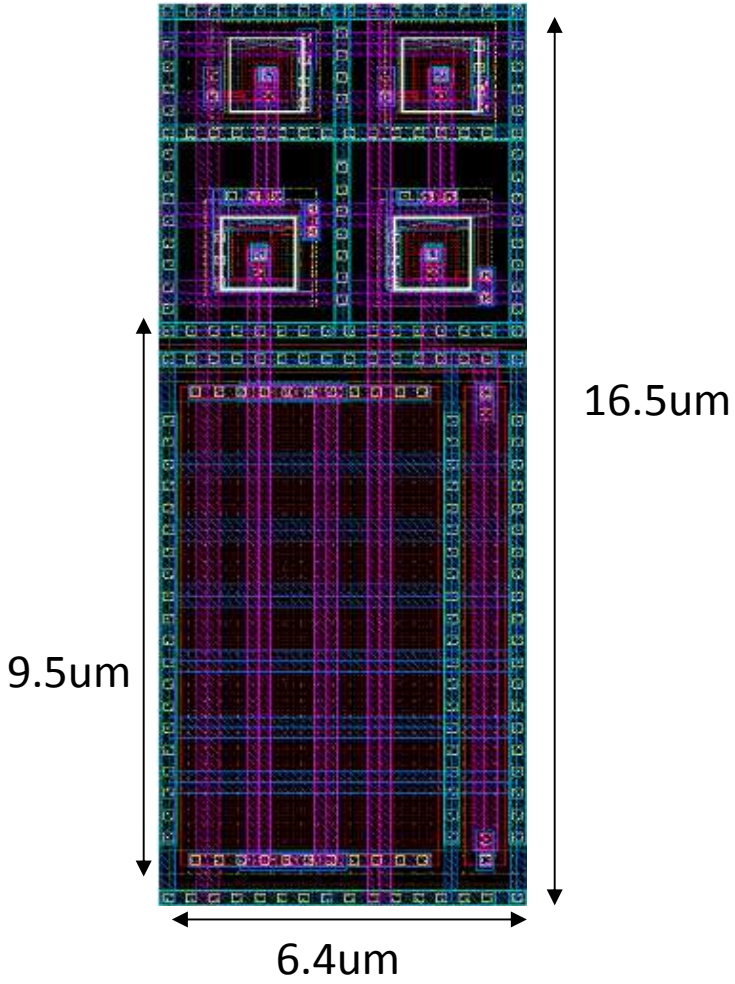




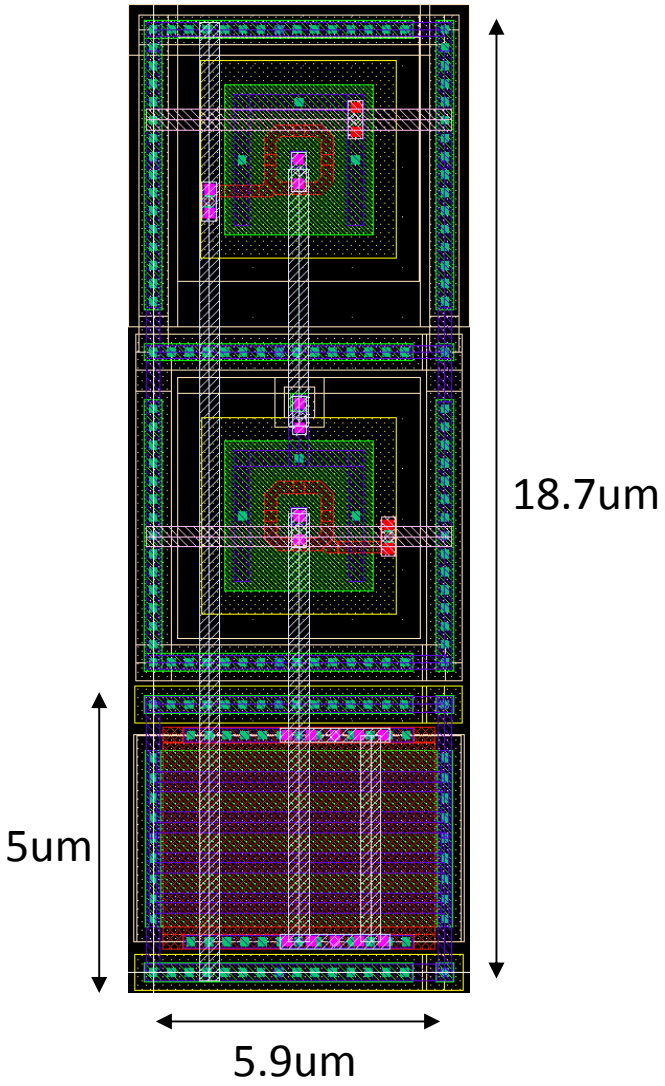
expected operation region of the circuit: comparable (linear) behaviour of the detector output, whether the charge is stored in/read from storage cells located on the Top tier or Bottom tier

memcell comparison

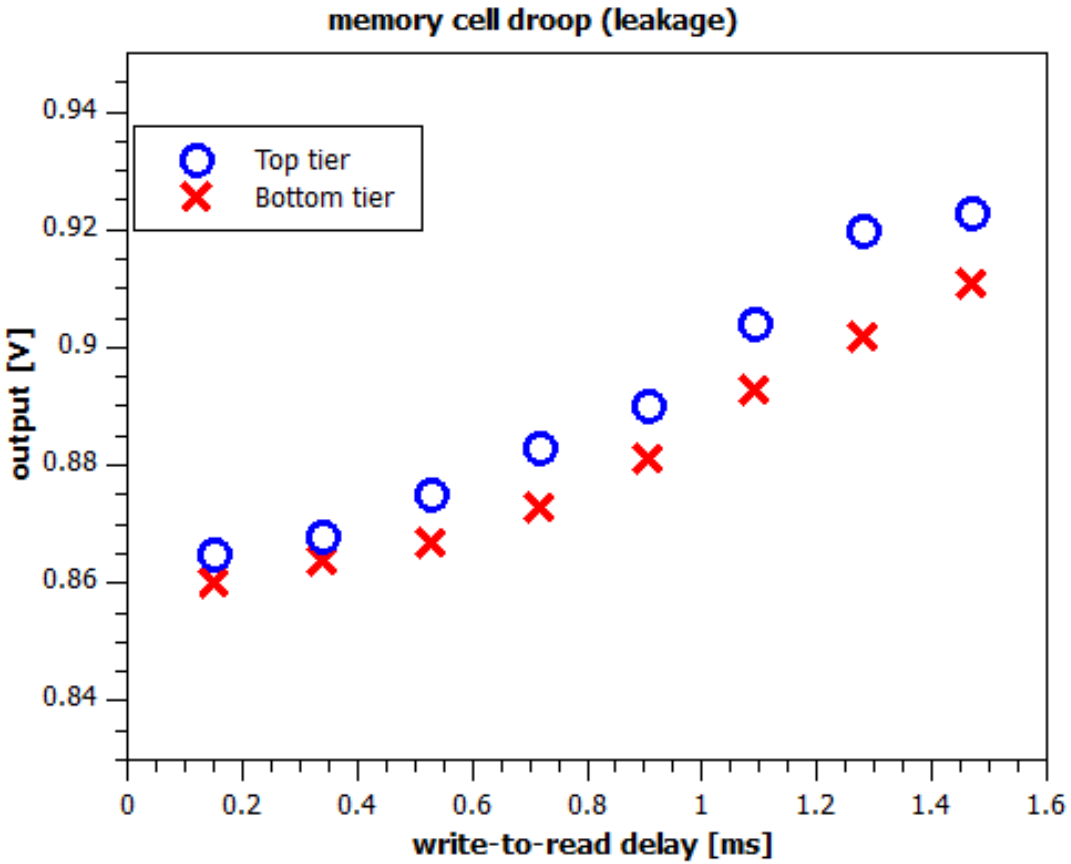
AGIPD1.0 (2D)



3DAGIPD0



Open issue: charge leakage



significant parasitic leakage of charge stored in memory cells

Memory cell layout to be optimized
Temperature dependence to be investigated