AGIPD

AGIPD Meeting: November 2015

A. Allahgholi[2], L.Bianco[2], A. Delfs[2], R. Dinapoli[1], P. Goettlicher[2], M. Gronewald[4], H. Graafsma[2,5], **D. Greiffenberg[1]**, B.H. Henrich[1], H. Hirsemann[2], S. Jack[2], R. Klanner[3], A. Klyuev[2], H. Krueger[4], S. Lange[2], A. Marras[2], **D. Mezza[1]**, A. Mozzanica[1], X. Qingqing[2], B. Schmitt[1], J. Schwandt[3], I. Sheviakov[2], X. Shi[1], U. Trunk[2], J. Zhang[2]

[1]Paul-Scherrer-Institut (PSI), SLS Detector Group, Villigen, Switzerland
[2]DESY, HASYLAB Group, Hamburg, Germany
[3]University of Hamburg, Hamburg, Germany
[4]University of Bonn, Bonn, Germany
[5]Mid Sweden University, Sundsvall, Sweden

OUTLINE

1. GAIN / Noise Map
   - Problem of the gain non uniformity
   - New Measurements
2. DR Scan / Linearity / Noise
3. Burst Mode
   - Settling time of Vrefpxb…
4. Droop
5. Chip Probing/ Bumpbond

1

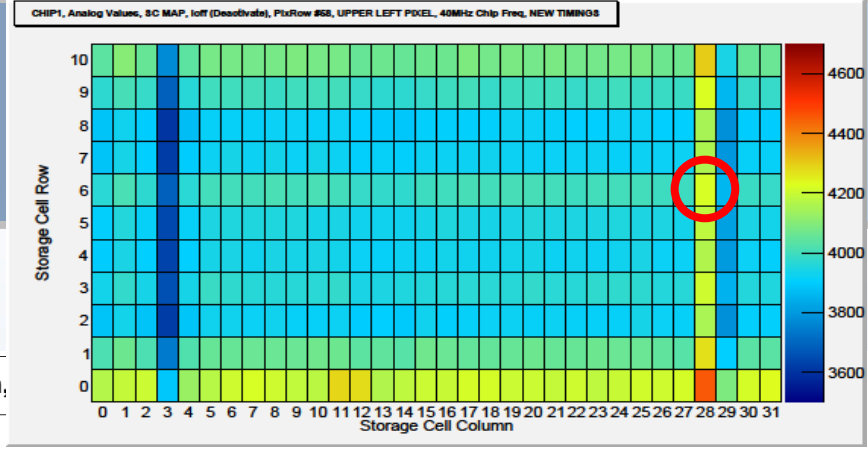
GAIN / Noise Map

GAIN/NOISE/BASELINE MAP

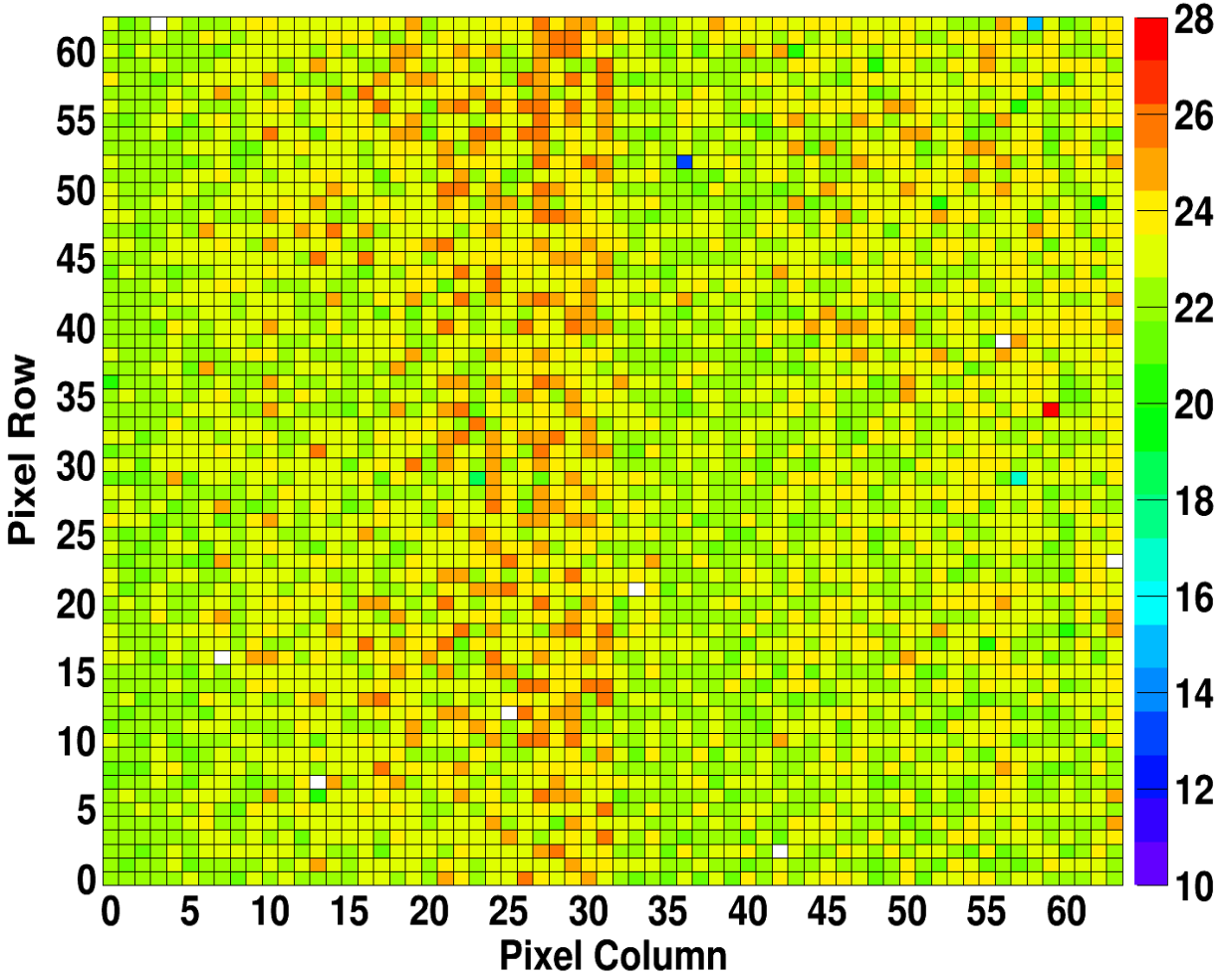
GAIN/NOISE: MEASUREMENT CONDITIONS

- Mo 17keV
- 1 Row of storage cell acquired for Chip 6 + 2 SC for Chip 1 (2 chiptest boxes died during acquisition) -> **No Cooling (Chip Temp ~60/70 °C)**
- Chip Running @40MHz
- Integration Time: 10 µs
- CDS gain HIGH and LOW
- Noise and baseline acquired with 200ns Integration Time
- Depletion Voltage: 250V
- Biasing: **External**

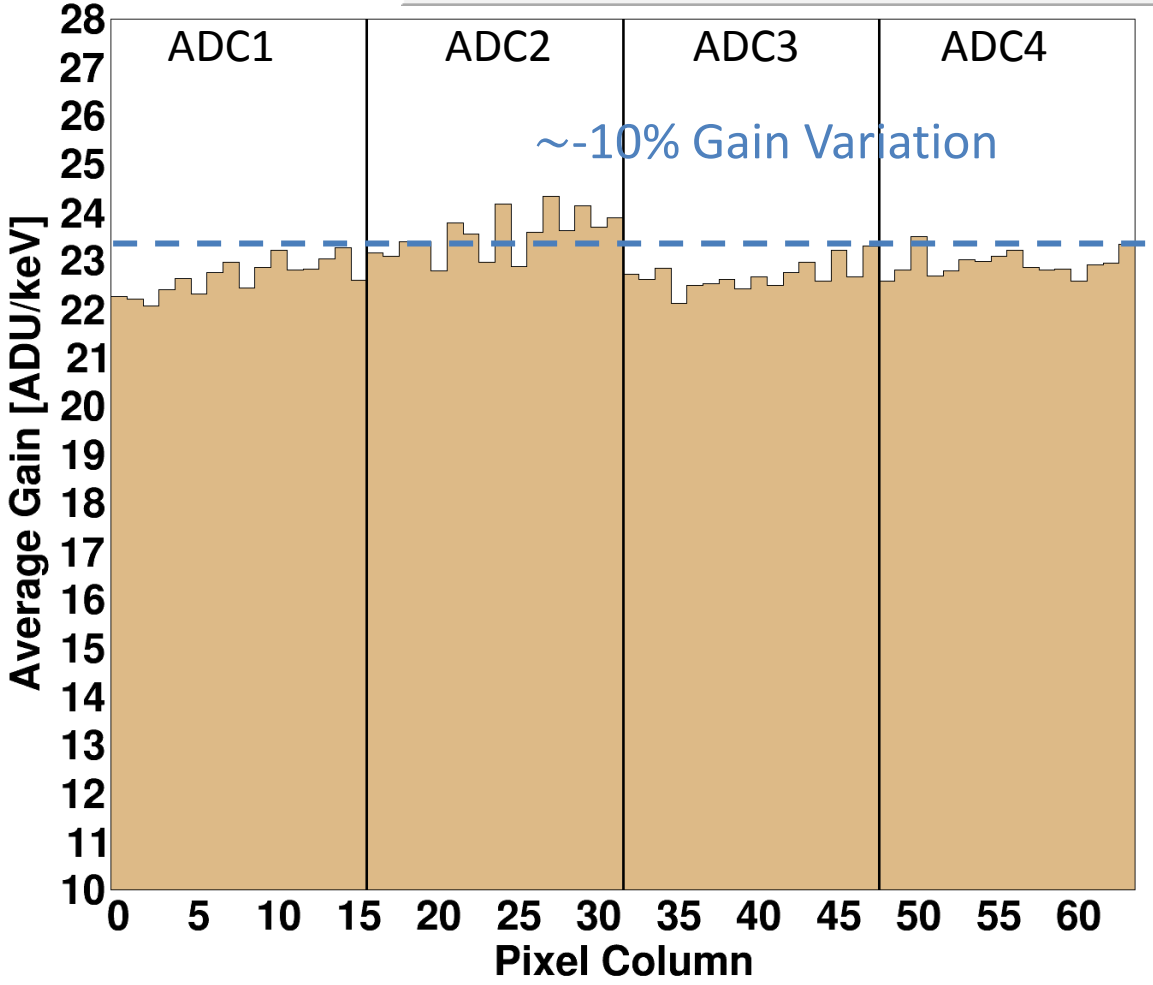
GAIN MAP, Chip 1
SC220, Row6 Col 28



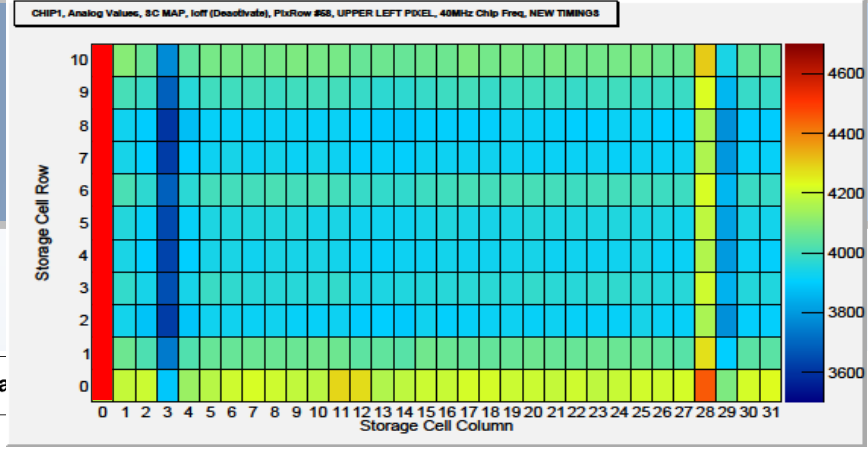
Gain Map, CDS Gain High, 1 Mo Peak, SC 220, CHIP1



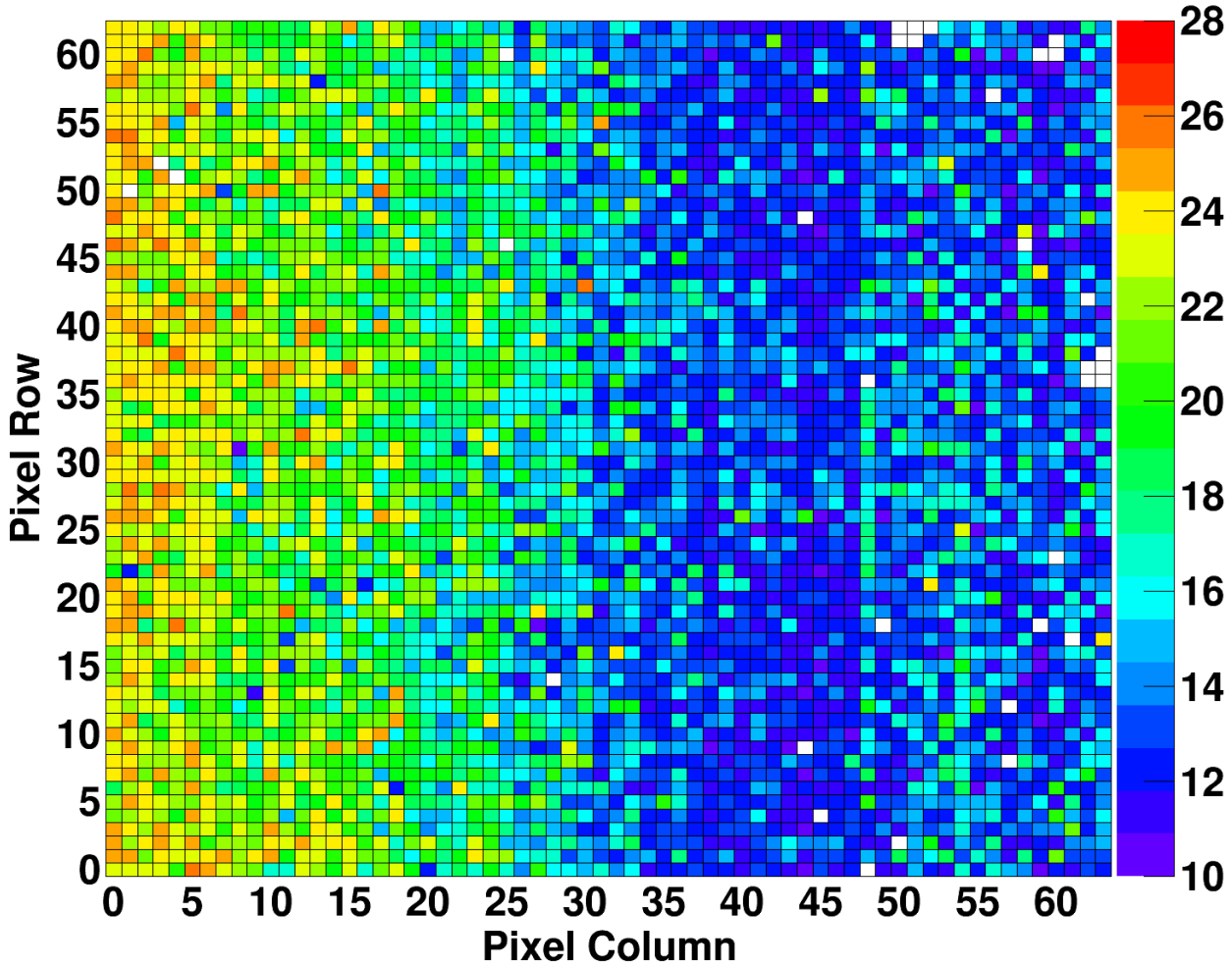
Average Gain, CDS Gain High,



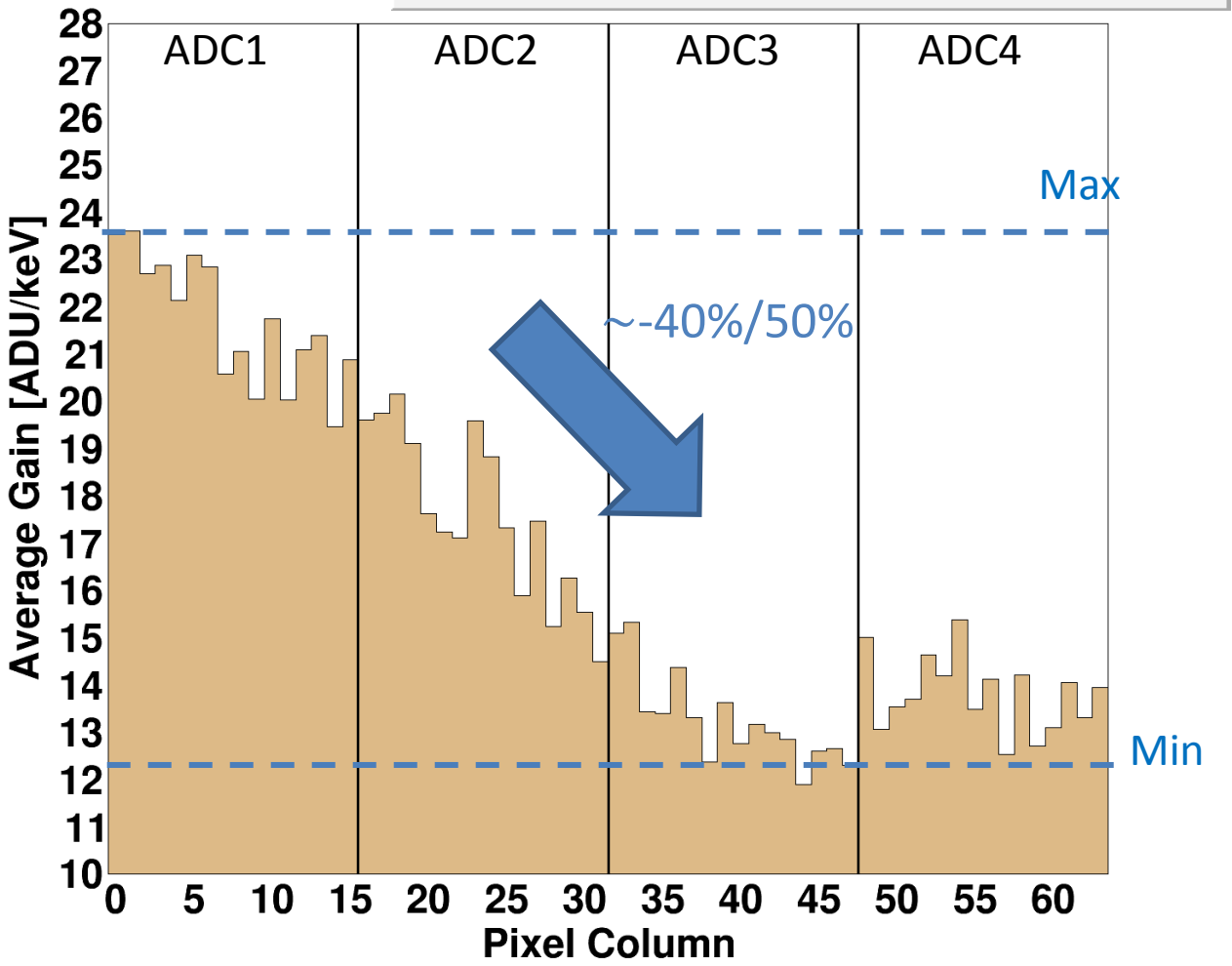
GAIN MAP, Chip 6
SC64, Row2 Col 0



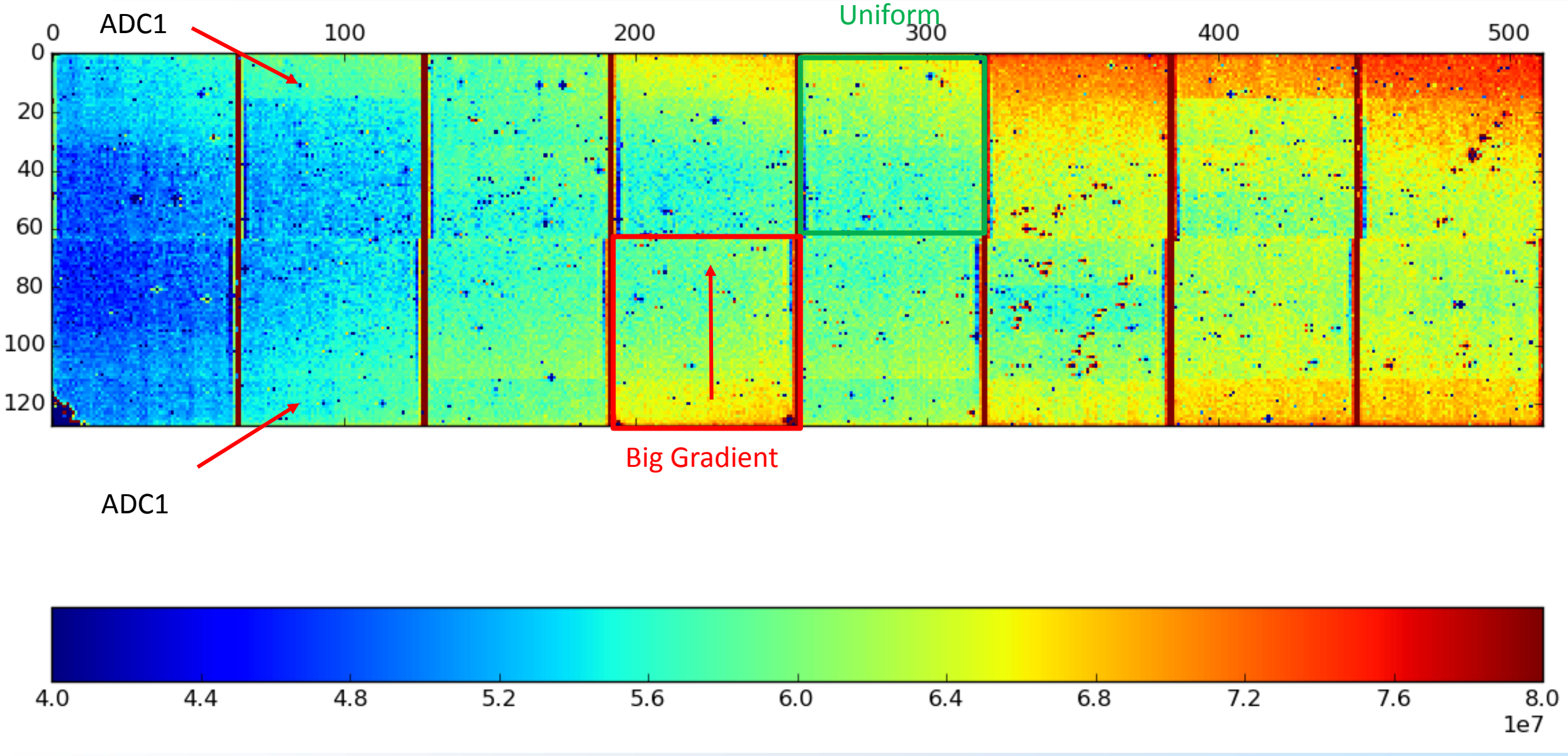
Gain Map, CDS Gain High, Storage Cell Row 2 Column 0, Mo 17.5keV, CHIP6

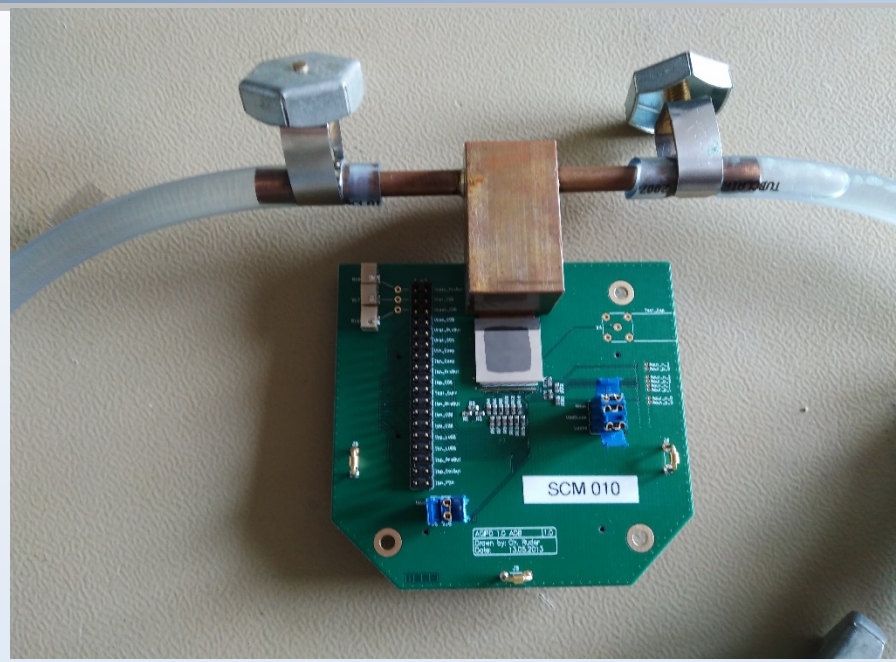


Average Gain, CDS Gain High, Stora



Module Map with Photons



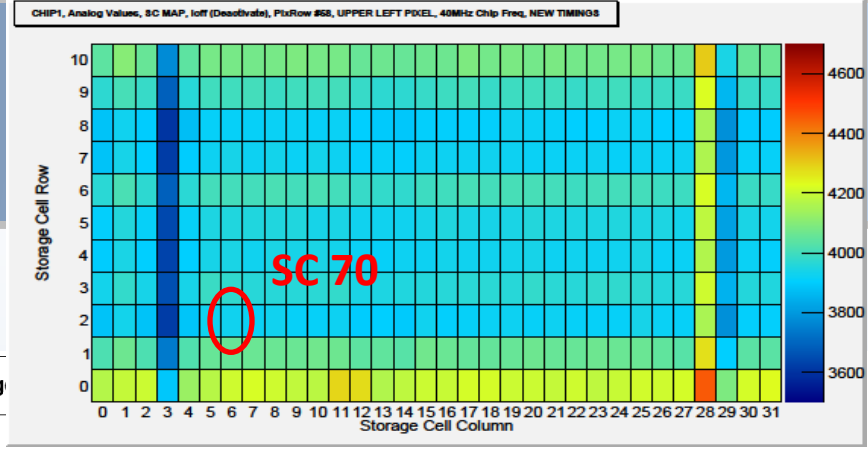


GAIN/NOISE: MEASUREMENT CONDITIONS

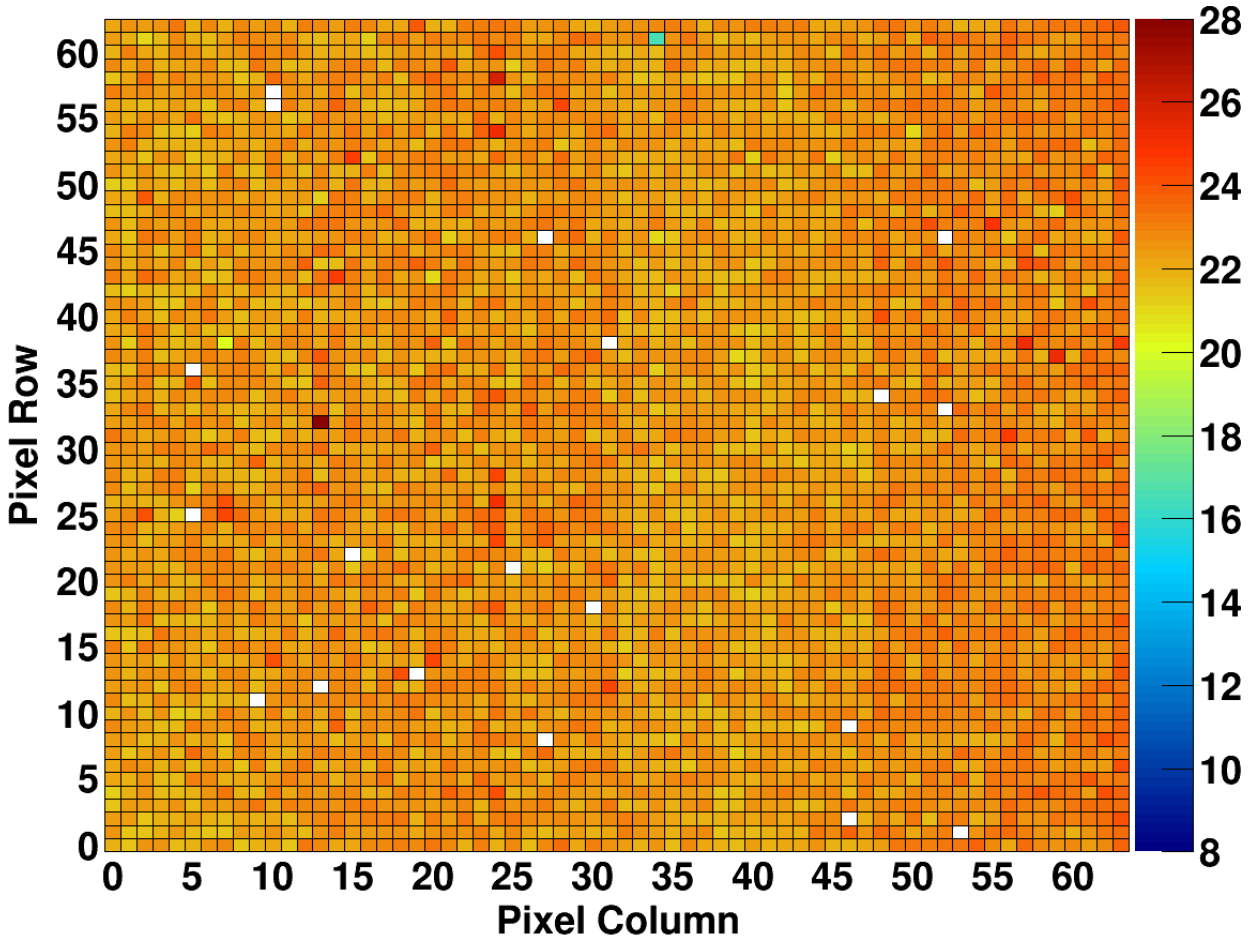
- Mo 17keV
- Chip SCM010 -> **Coolable assembly**
- Temperature: **20°C**
- Chip Running @10MHz for photon measurements (Less Measurement Time)
- Integration Time: 20 µs
- CDS gain HIGH and LOW
- Noise and baseline acquired with 200ns Integration Time (Chip operated @40MHz)
- Depletion Voltage: 250V
- Biasing: **Internal** (results not affected by choosing INT or EXT)

Gain MAP, Chip SCM 010

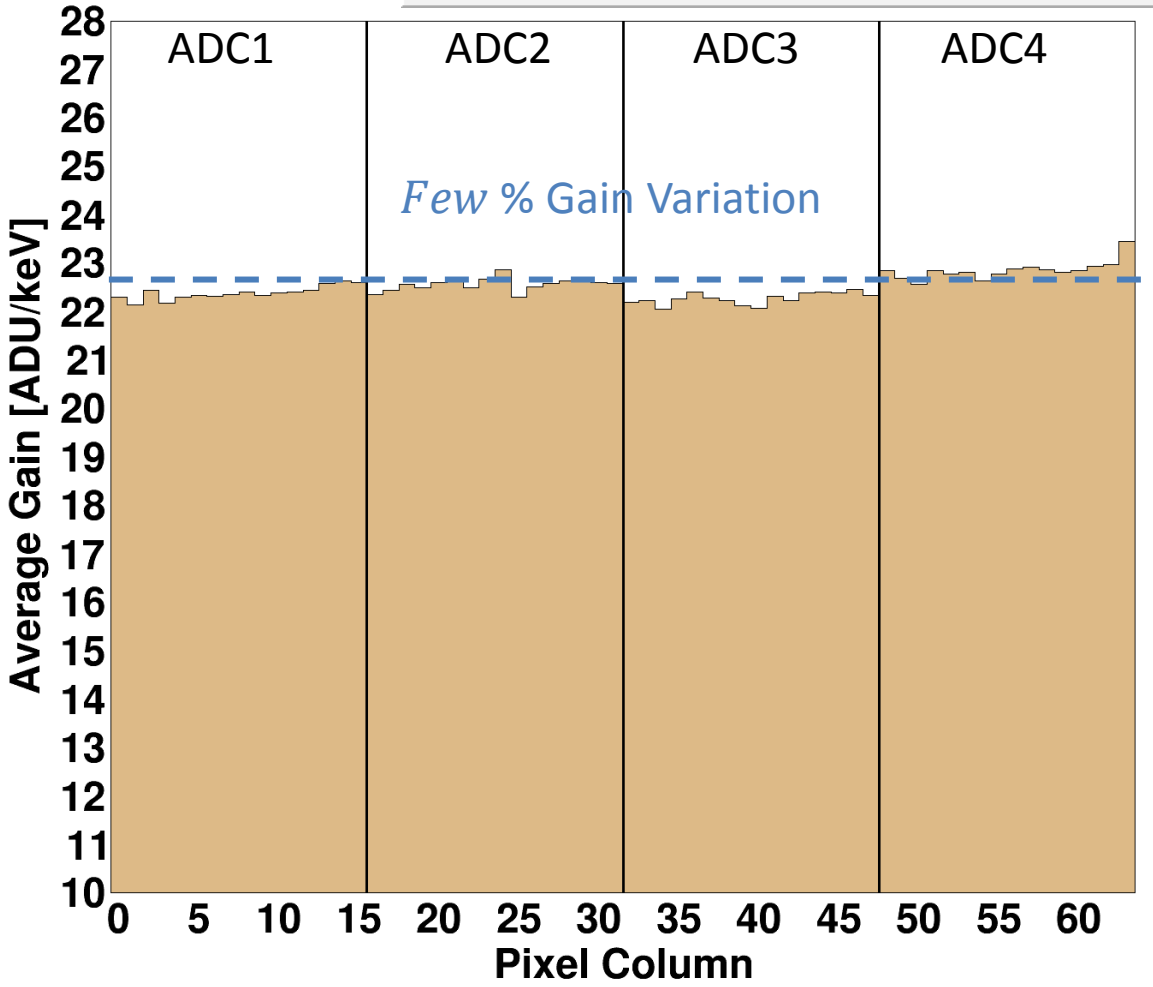
SC70, Vrefcds=650mV, CDS gain HIGH, Int_time = 20us



Gain Map, CDS Gain HIGH, 1 Mo Peak, SC 70, Vrefcds = 650mV, 10 MHz

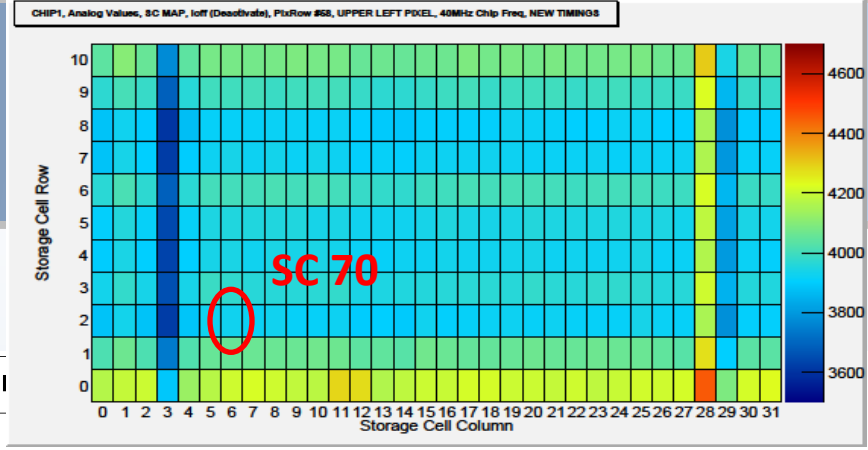


Average Gain, CDS Gain HIGH, Storag

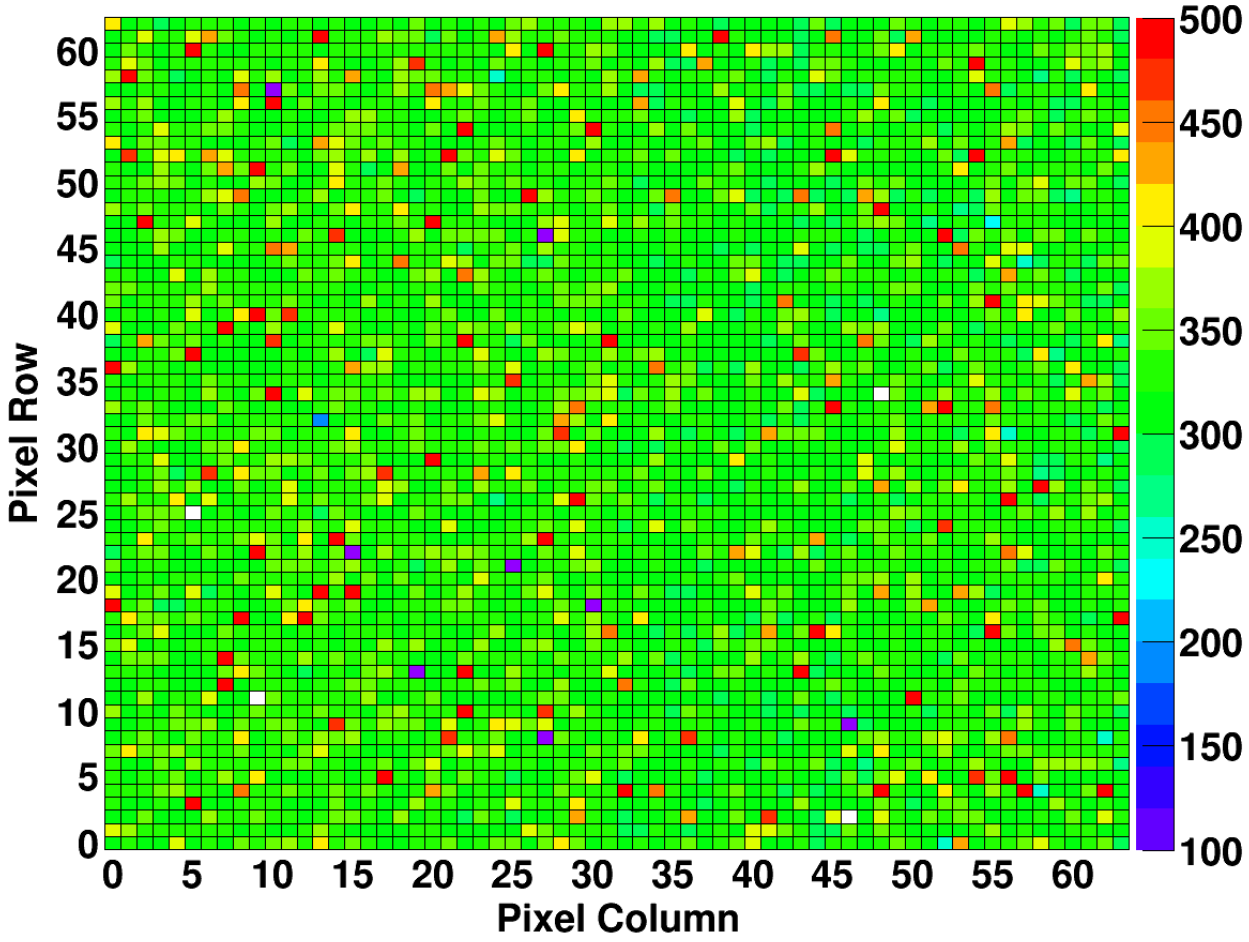


Noise MAP, Chip SCM 010

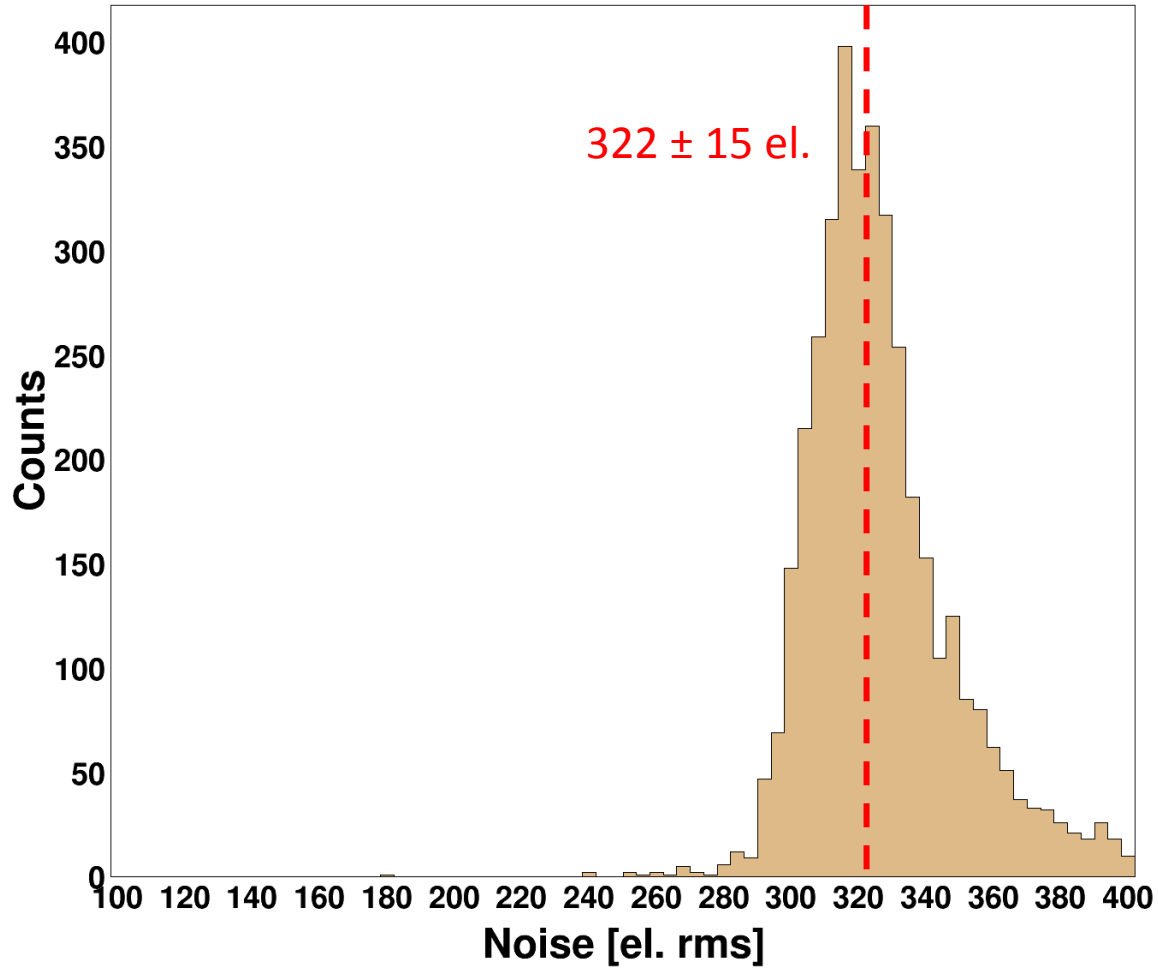
SC70, Vrefcds=650mV, CDS gain LOW, Int_time = 200ns



Noise Map, 200ns, CDS Gain LOW, SC 70, CHIP SCM010



Noise Distribution, CDS Gain LOW, I

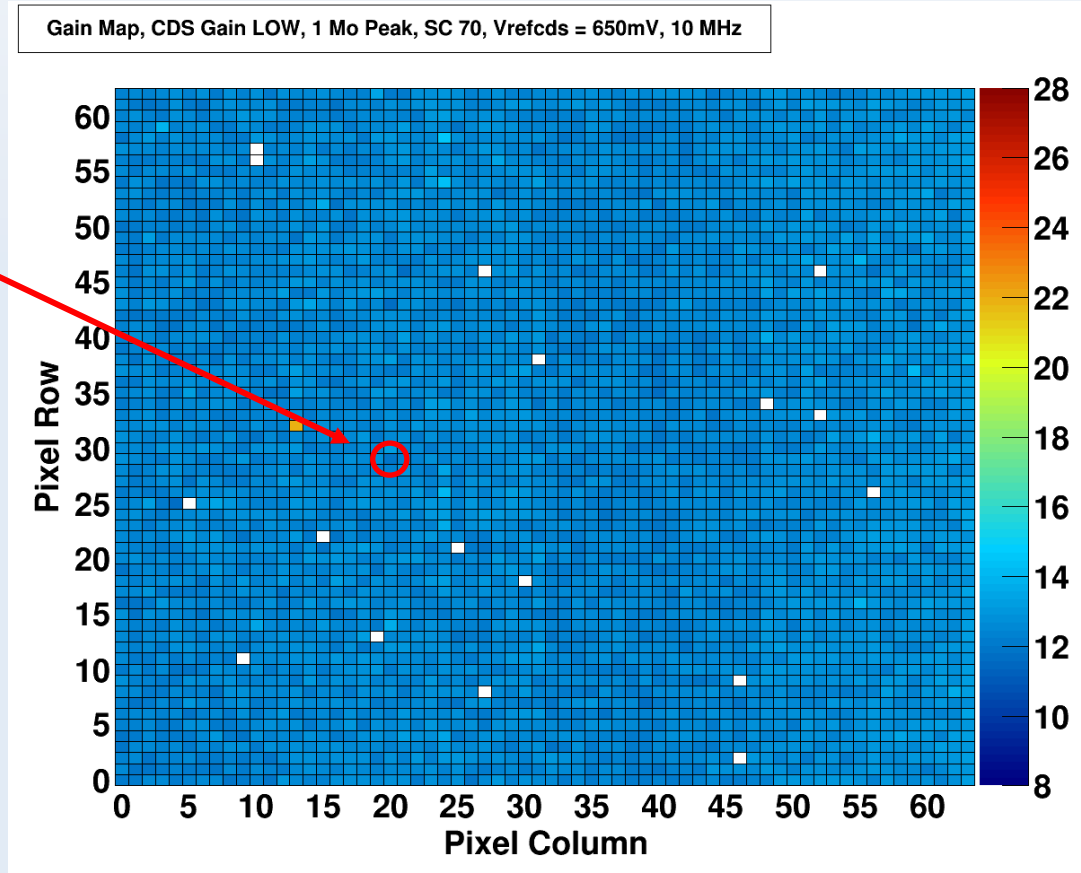


2

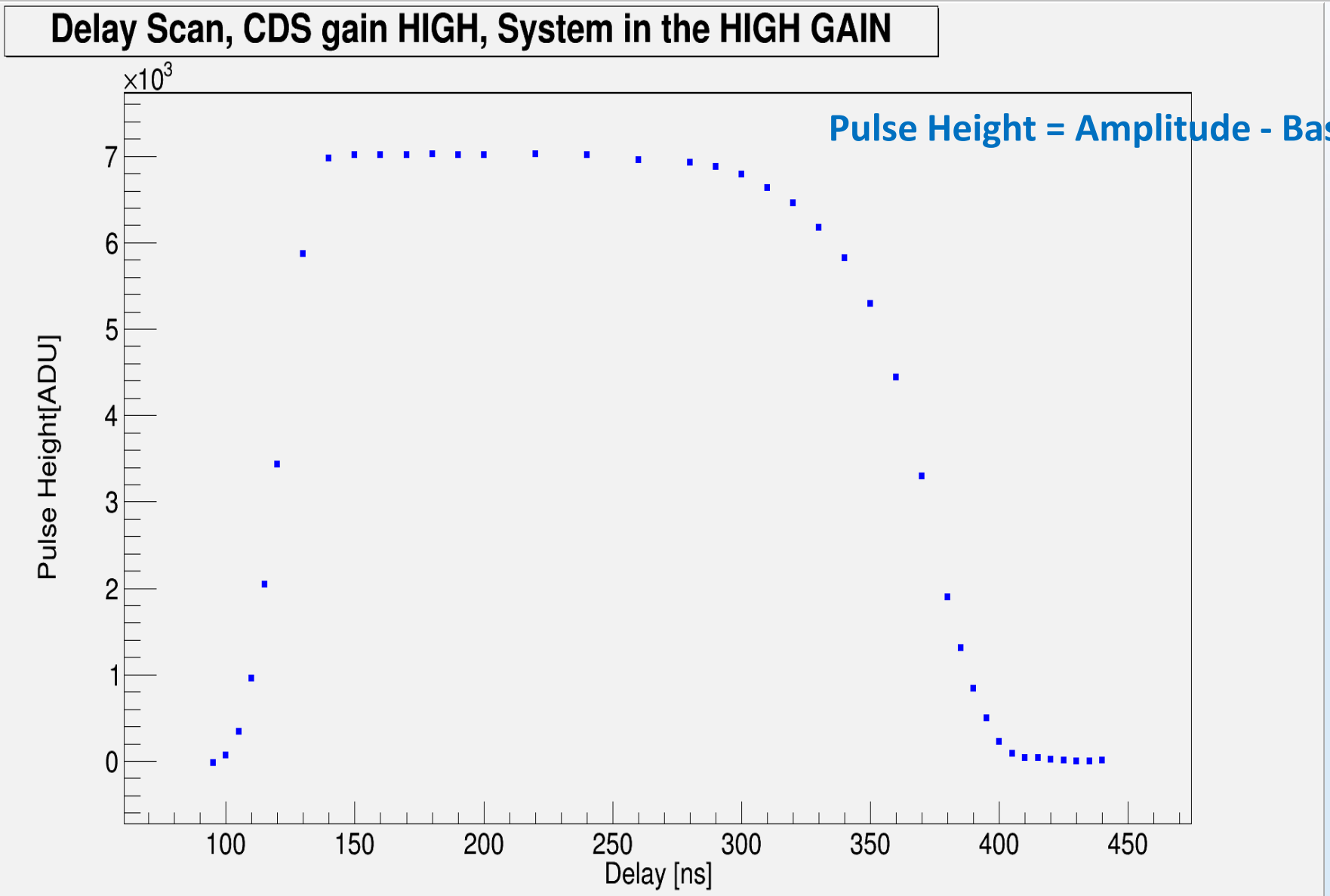
DR Scan / Linearity / Noise

DYNAMIC RANGE: MEASUREMENT CONDITIONS

- Chip SCM010 -> **Coolable assembly**
- Pixel 1565: Row 29, Second ADC from the pads
- SC70
- Infrared Laser: **λ=1030nm**
- Temperature: **20°C**
- Chip Running @40MHz
- CDS gain HIGH and LOW
- Depletion Voltage: 250V
- Each point -> Average over 1000 frames
- Biasing: **Internal**



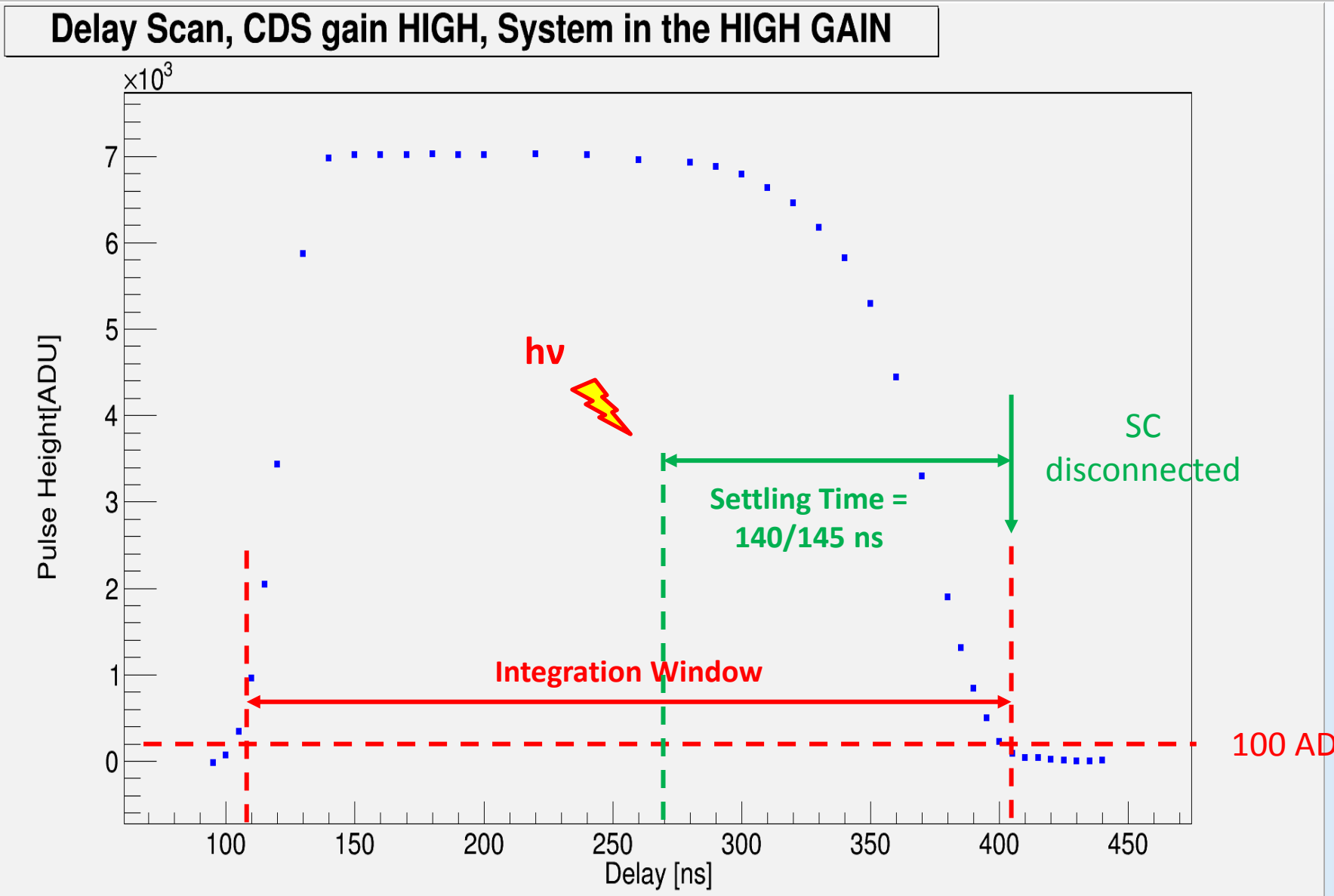
DELAY SCAN



Pulse Height = Amplitude - Baseline

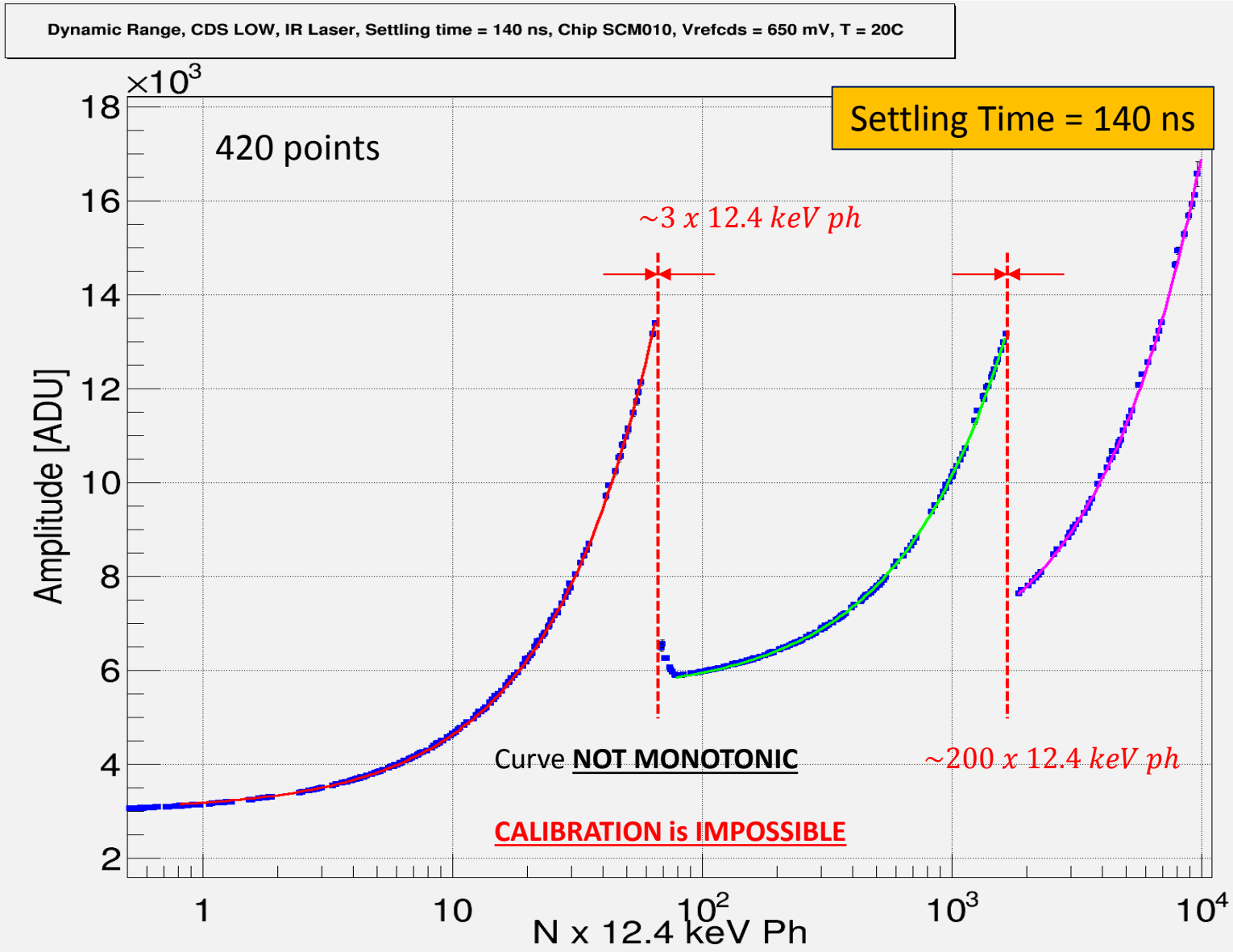
- Determination of the integration window: PH ≤ 100 ADU assumed to be start and stop of the integration window.
- Assuming the last point as the SC disconnection.
- Take 140ns as “safe” settling time.

DELAY SCAN



- Determination of the integration window: PH ≤ 100 ADU assumed to be start and stop of the integration window.
- Assuming the last point as the SC disconnection.
- Take 140ns as “safe” settling time.

DR Scan - CDS gain LOW



Data from analysis

Gain Switching HIGH-MEDIUM: **65.4 x 12.4 keV ph.**
Gap HIGH-MEDIUM: **ca. 3 x 12.4 keV ph.**

Gain Switching Medium-LOW: **ca. 1650 x 12.4 keV ph.**
Gap Medium-LOW: **ca. 200 x 12.4 keV ph.**

Last point in LOW gain: **ca. 9650 x 12.4 keV ph.**

Gains obtained from the fit:

HIGH GAIN = 12.94 ADU/keV
MEDIUM GAIN = 0.375 ADU/keV
LOW GAIN = 0.092 ADU/keV

Theoretical Ratios:

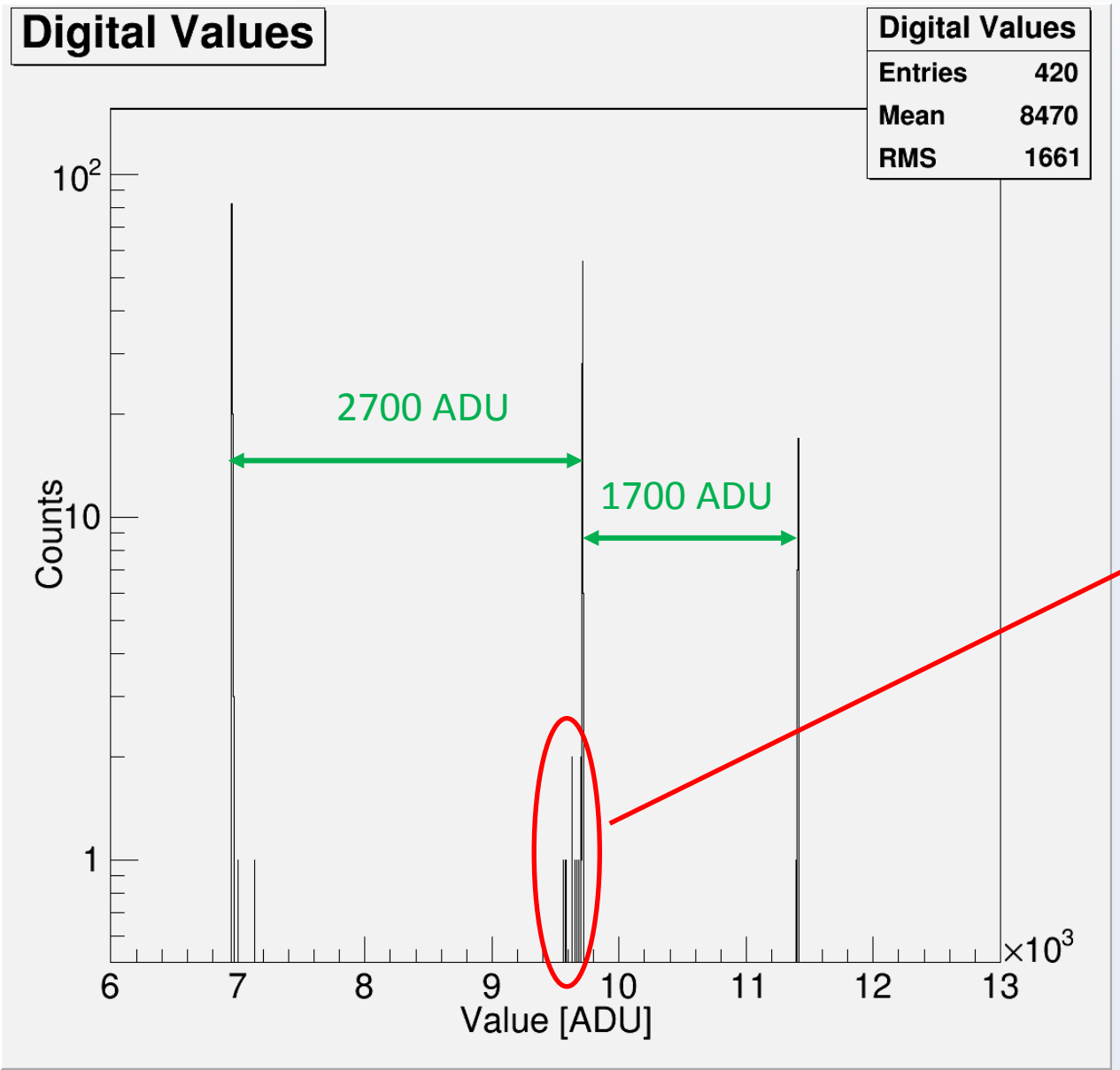
C_{HIGH} = 60fF
C_{MEDIUM} = 3pF
C_{LOW} = 10pF

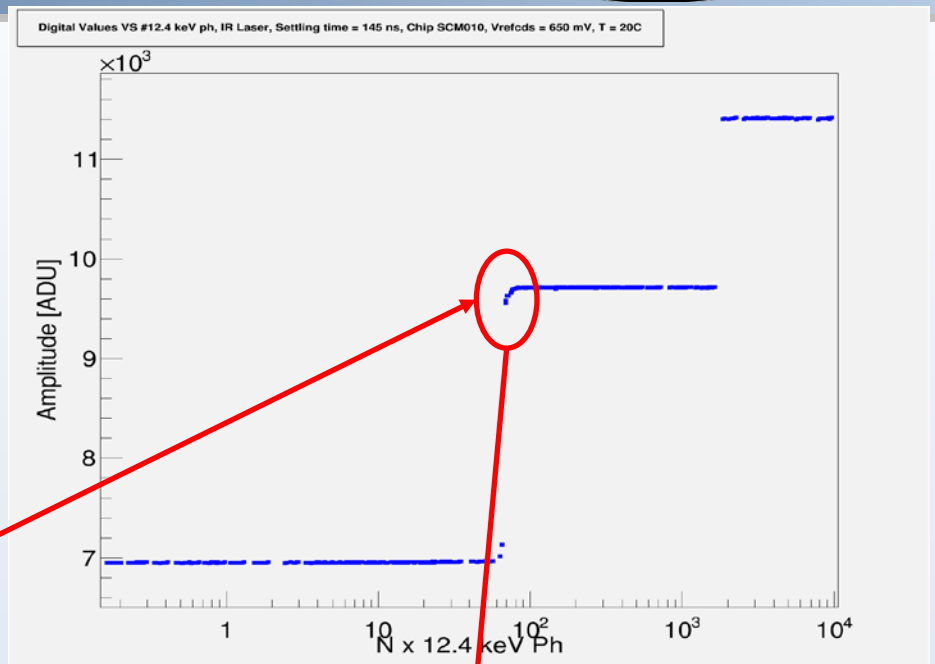
$$\begin{cases} \frac{HG}{MG} = \frac{C_{Medium} + C_{HIGH}}{C_{HIGH}} = 51 \\ \frac{MG}{LG} \cong \frac{C_{Medium} + C_{LOW} + C_{HIGH}}{C_{Medium} + C_{HIGH}} = 4.27 \end{cases}$$

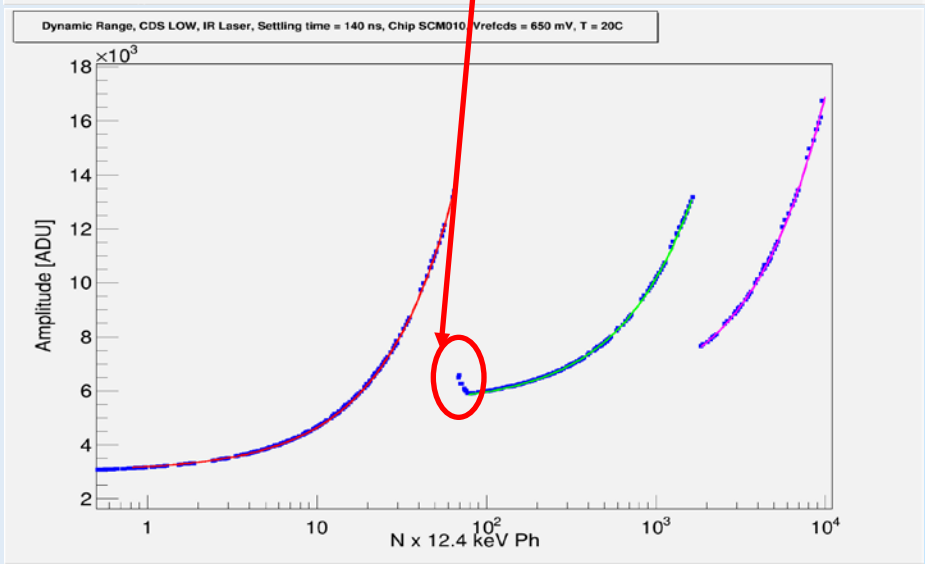
Ratios from fit:

HG/MG = **34.5** (parasitic dominant)
MG/LG = **4.1**

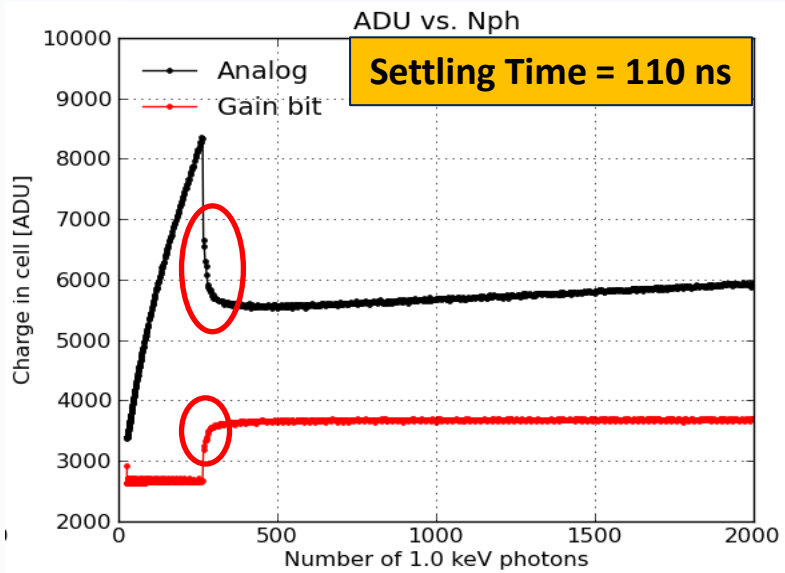
DR Scan - CDS gain LOW - Digital

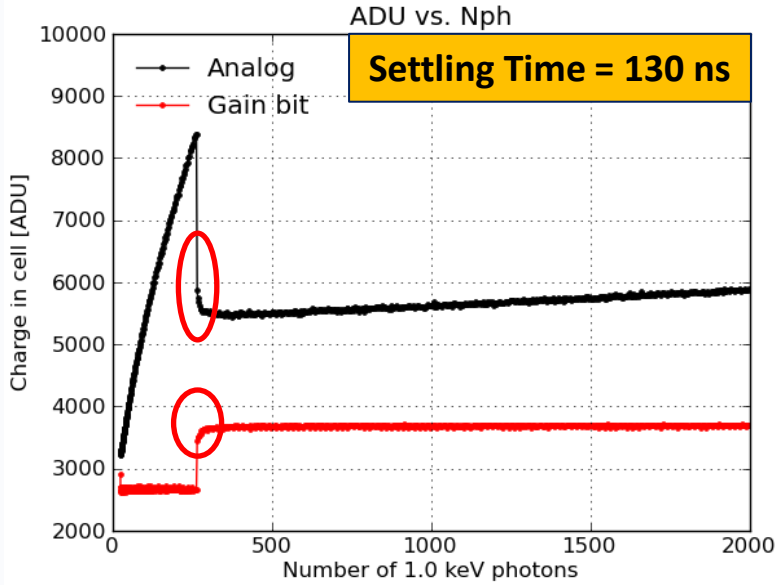


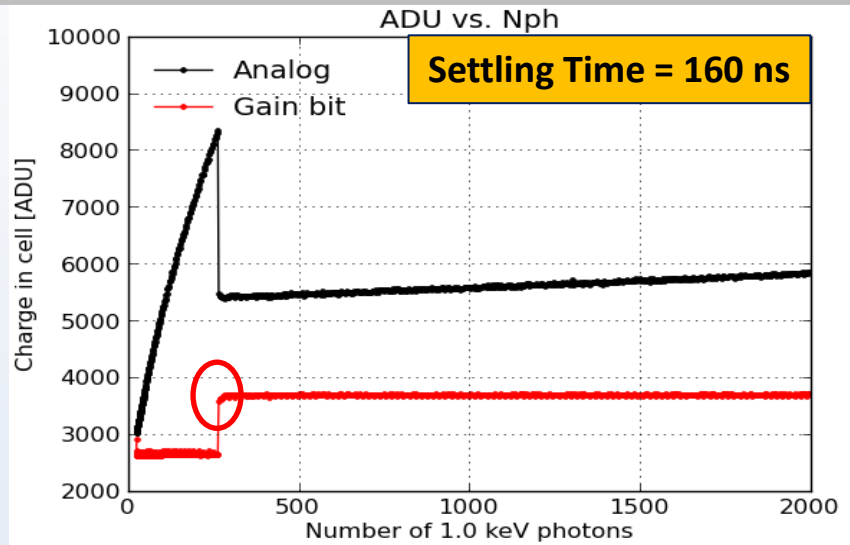


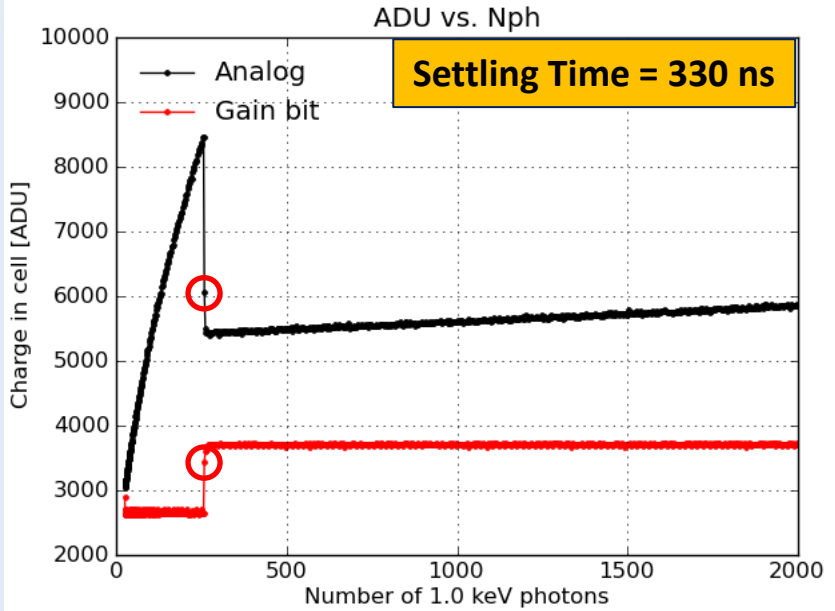


DR Scan – Pulsed Capacitor Module









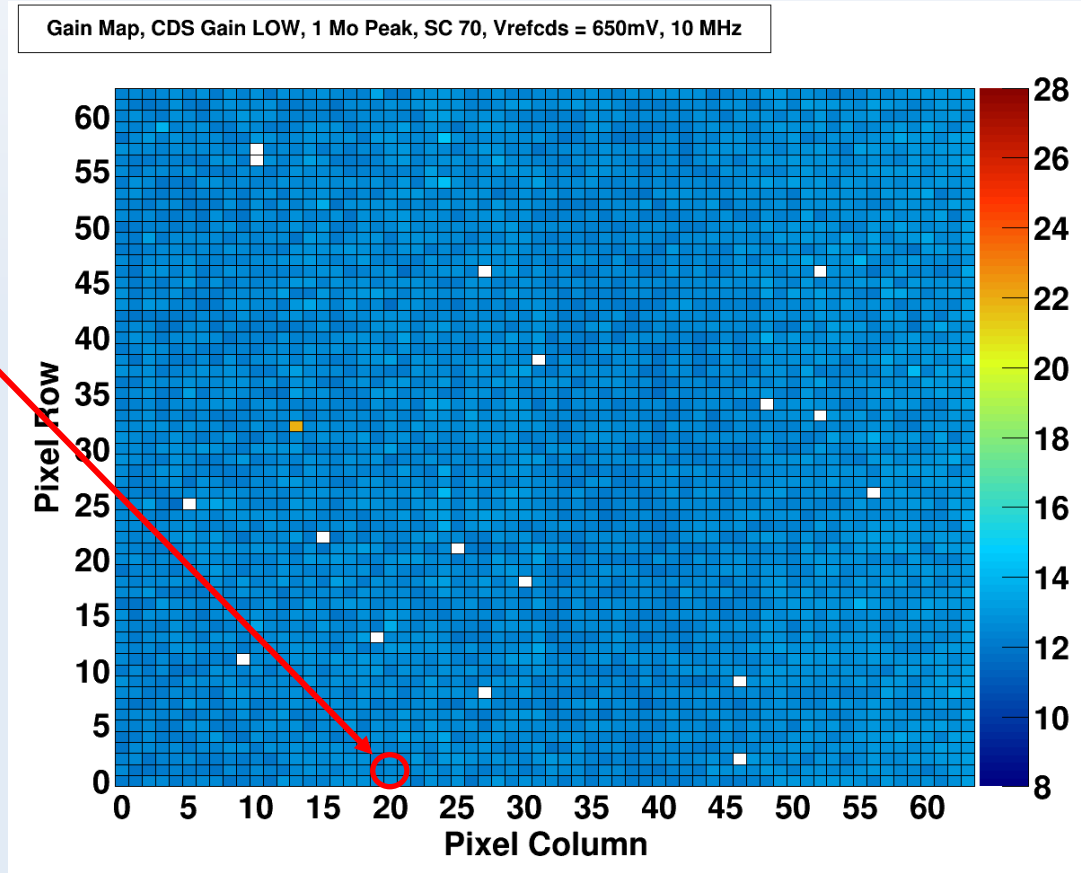
DYNAMIC RANGE: TRIALS…

- **Chip 1** -> No Cooling (Chip Temp ~60/70 °C)
- Pixel Row 2, Second ADC from the pads

- SC 70, SC 100
- CDS gain HIGH and LOW
- Old Readout Scheme
- Different Settling Times
- Different comparator currents

- And so on….

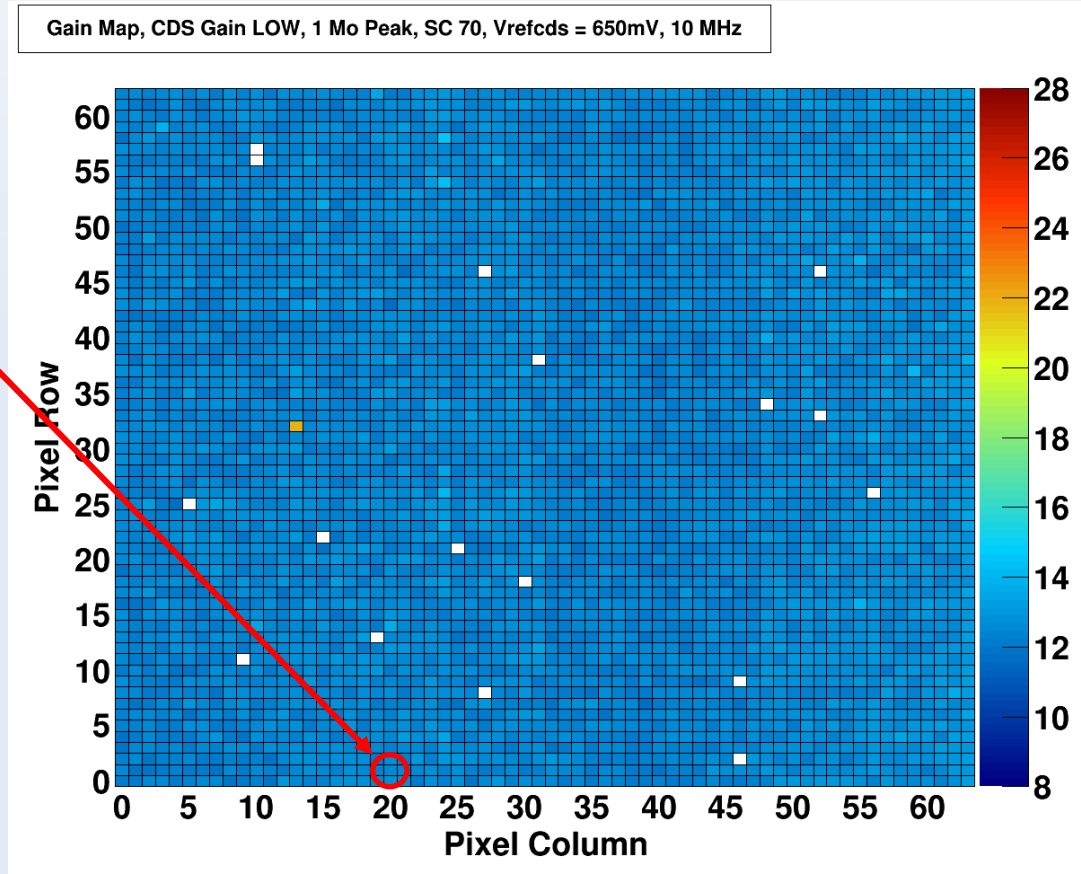
The non linearity problem wasn't solved…



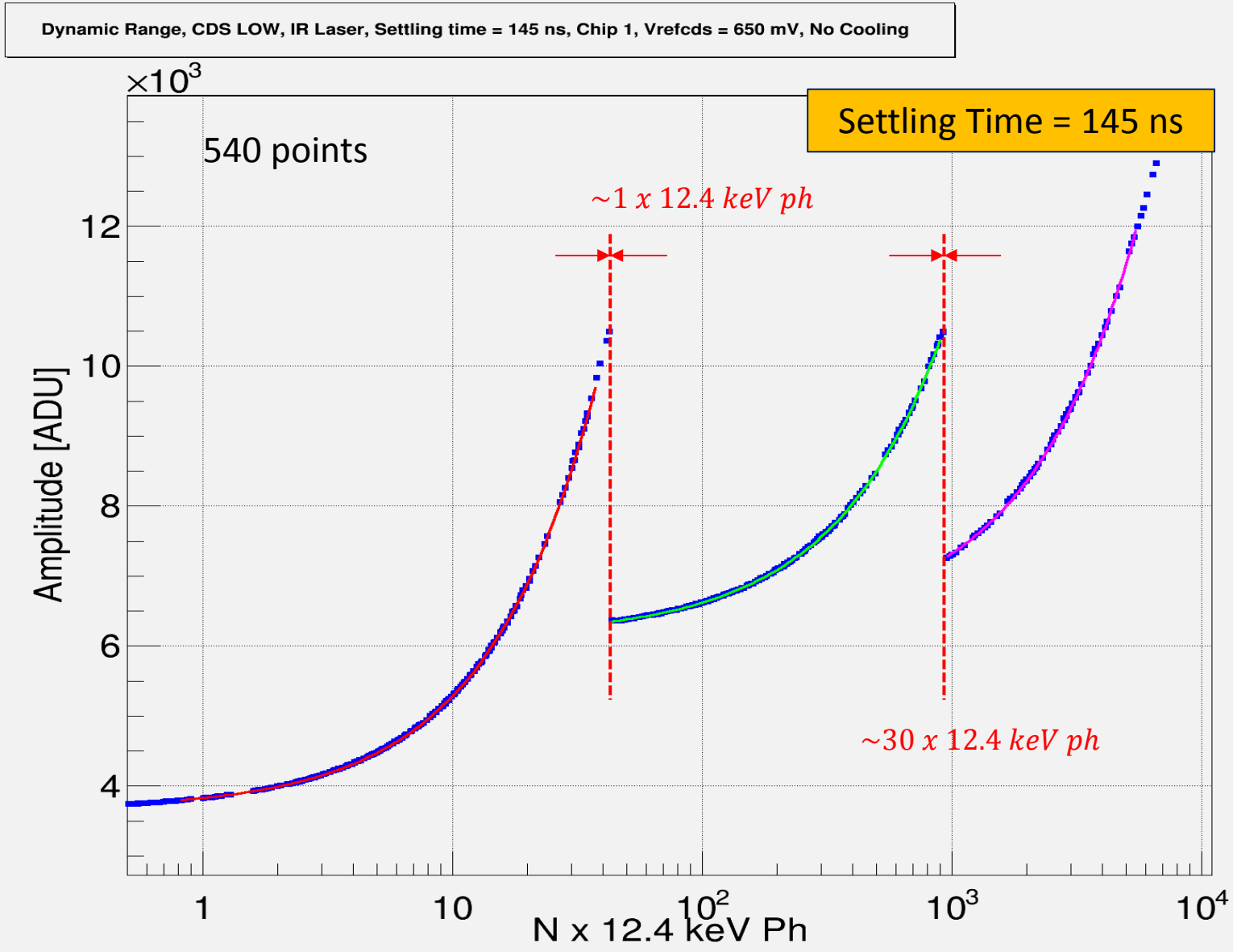
DYNAMIC RANGE: MEASUREMENT CONDITIONS

- **Chip 1** -> **No Cooling (Chip Temp ~60/70 °C)**
- Pixel Row 2, Second ADC from the pads
- SC70
- Infrared Laser: **λ=1030nm**
- Chip Running @40MHz
- CDS gain HIGH and LOW
- Depletion Voltage: 250V
- Each point -> Average over 1000 frames
- Biasing: **Internal**

- **VddPA = VddPix = 1.55 V (+50mV)**
- **Lower Vth,comp**
- **CDS Current from 60uA to 100uA**



DR Scan - CDS gain LOW



Data from analysis

Gain Switching HIGH-MEDIUM: **42.5 x 12.4 keV ph.**
Gap HIGH-MEDIUM: **ca. 1 x 12.4 keV ph.**

Gain Switching Medium-LOW: **ca. 925 x 12.4 keV ph.**
Gap Medium-LOW: **ca. 30 x 12.4 keV ph.**

Last point in LOW gain: **ca. 6600 x 12.4 keV ph.**

Gains obtained from the fit:

HIGH GAIN = 13.02 ADU/keV
MEDIUM GAIN = 0.38 ADU/keV
LOW GAIN = 0.083 ADU/keV

Theoretical Ratios:

C_{HIGH} = 60fF
C_{MEDIUM} = 3pF
C_{LOW} = 10pF

$$\begin{cases} \frac{HG}{MG} = \frac{C_{Medium} + C_{HIGH}}{C_{HIGH}} = 51 \\ \frac{MG}{LG} \cong \frac{C_{Medium} + C_{LOW} + C_{HIGH}}{C_{Medium} + C_{HIGH}} = 4.27 \end{cases}$$

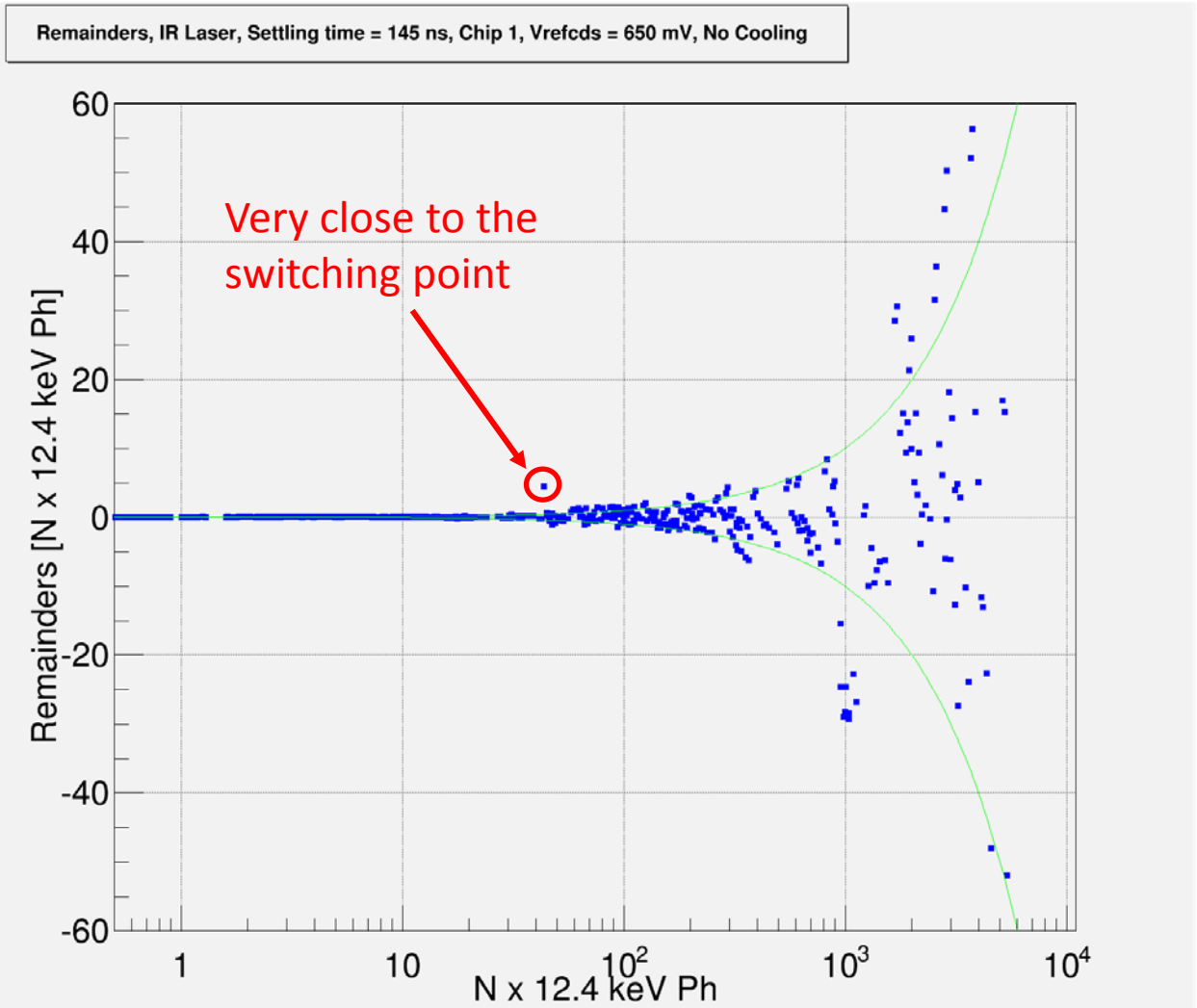
Ratios from fit:

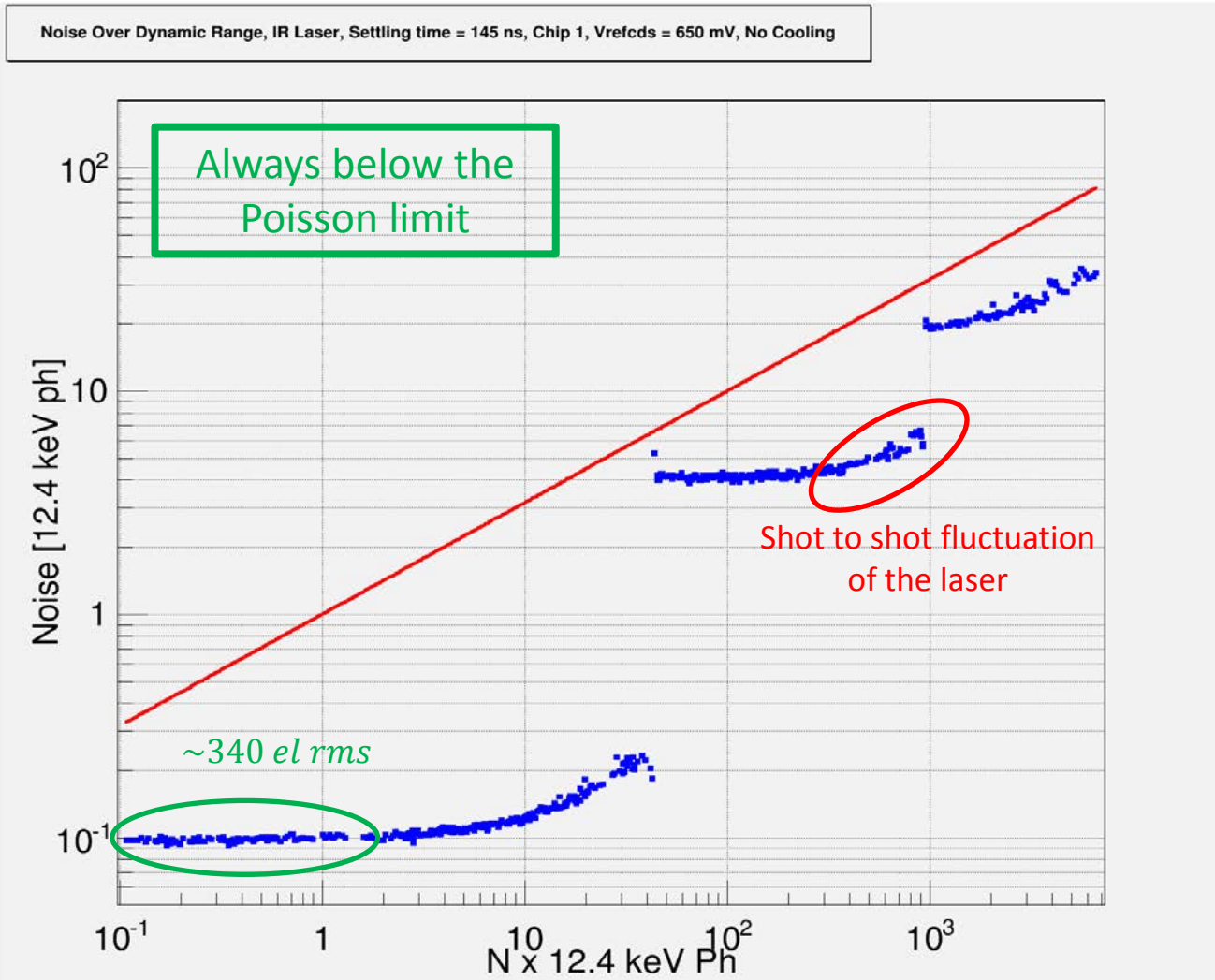
HG/MG = **34.26** (parasitic dominant)
MG/LG = **4.55**

Linearity & Noise over DR - CDS gain LOW

±1%

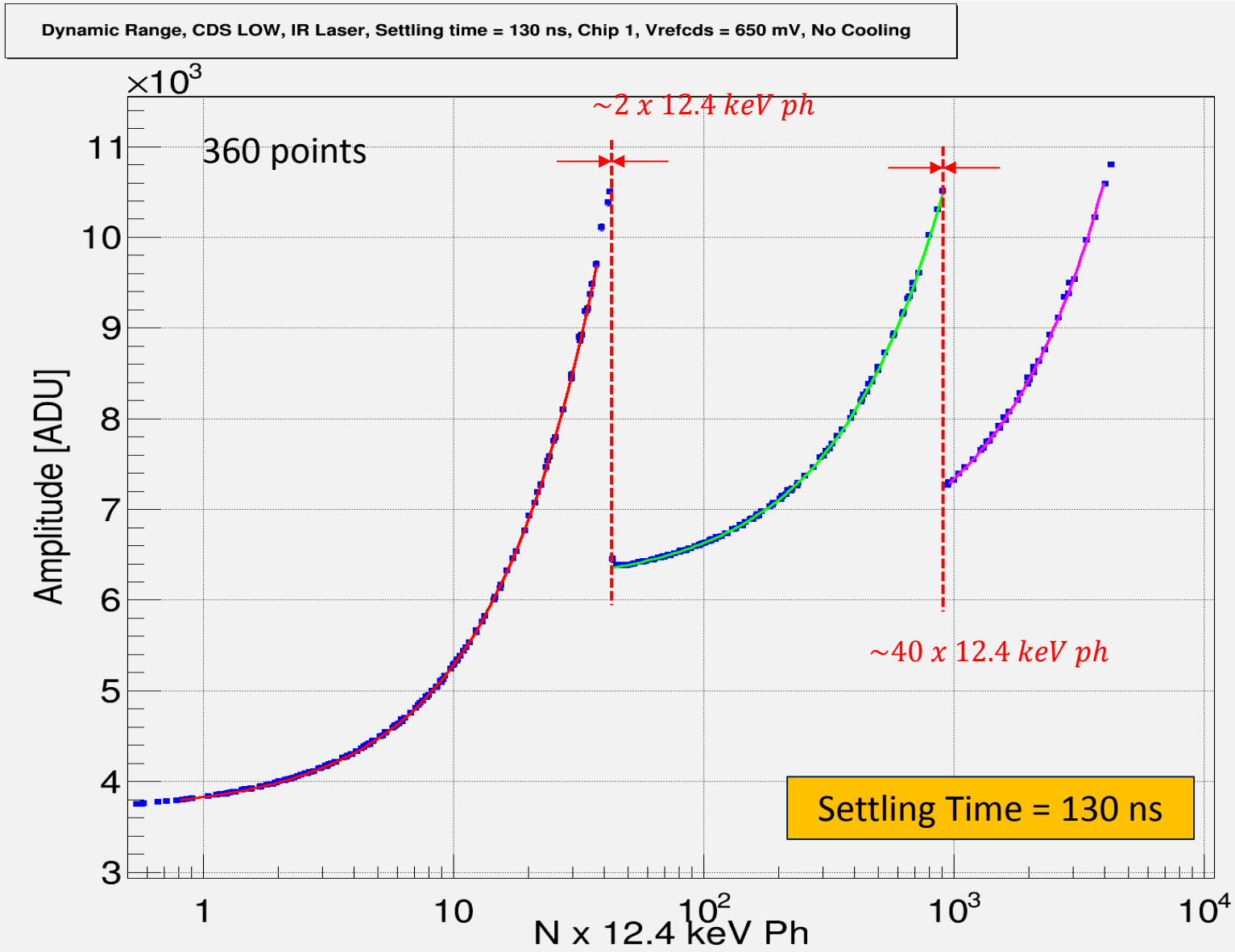
Poisson Limit





Going back from this point to
Settling Time 130 ns …..

DR Scan - CDS gain LOW



Data from analysis

Gain Switching HIGH-MEDIUM: **x 12.4 keV ph.**
Gap HIGH-MEDIUM: **ca. 1 x 12.4 keV ph.**

Gain Switching Medium-LOW: **ca. 900 x 12.4 keV ph.**
Gap Medium-LOW: **ca. 40 x 12.4 keV ph.**

Last point in LOW gain: **ca. 4250 x 12.4 keV ph.**

Gains obtained from the fit:

HIGH GAIN = 13.1 ADU/keV
MEDIUM GAIN = 0.38 ADU/keV
LOW GAIN = 0.09 ADU/keV

Theoretical Ratios:

C_{HIGH} = 60fF
C_{MEDIUM} = 3pF
C_{LOW} = 10pF

$$\begin{cases} \frac{HG}{MG} = \frac{C_{Medium} + C_{HIGH}}{C_{HIGH}} = \mathbf{51} \\ \frac{MG}{LG} \cong \frac{C_{Medium} + C_{LOW} + C_{HIGH}}{C_{Medium} + C_{HIGH}} = \mathbf{4.27} \end{cases}$$

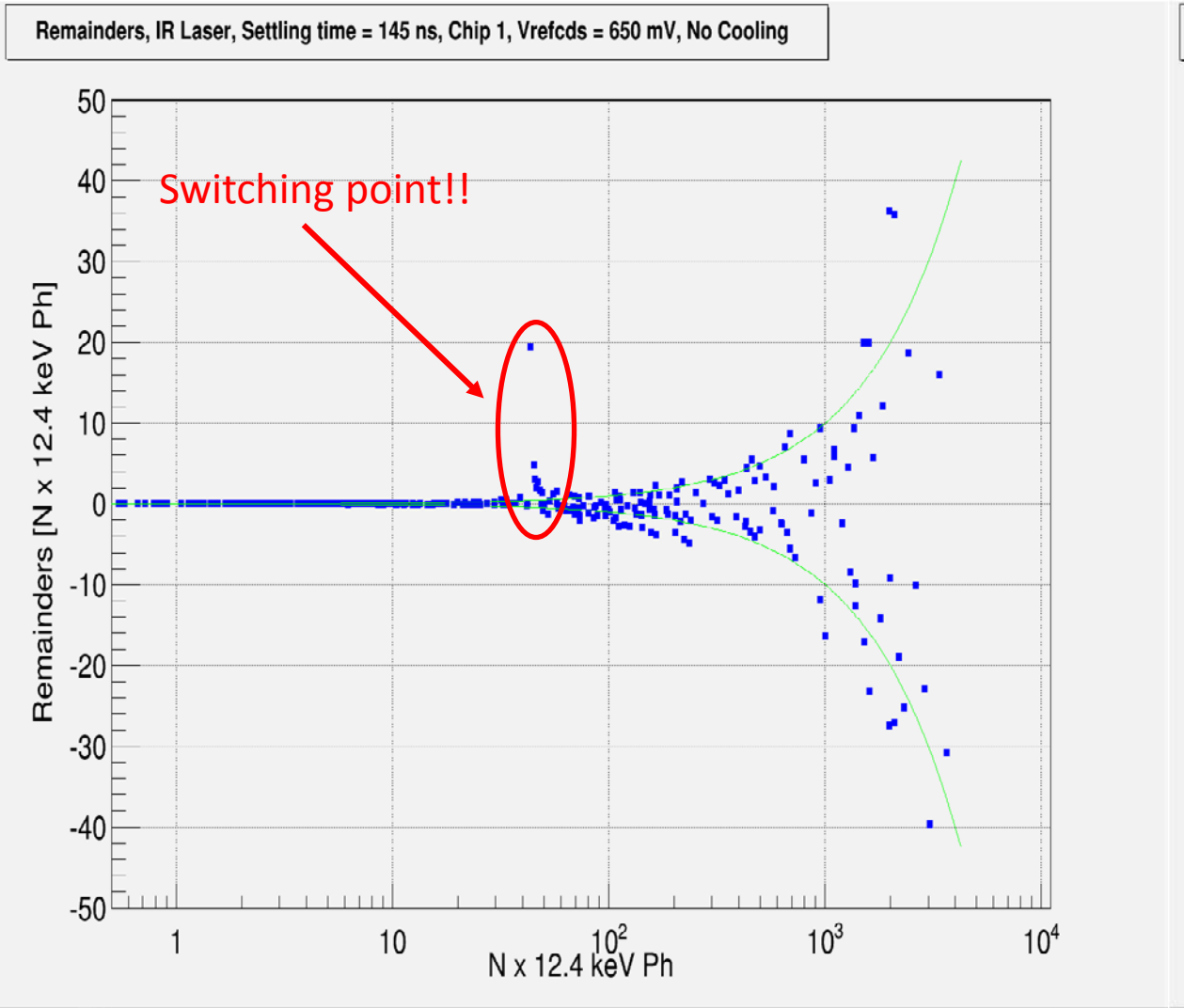
Ratios from fit:

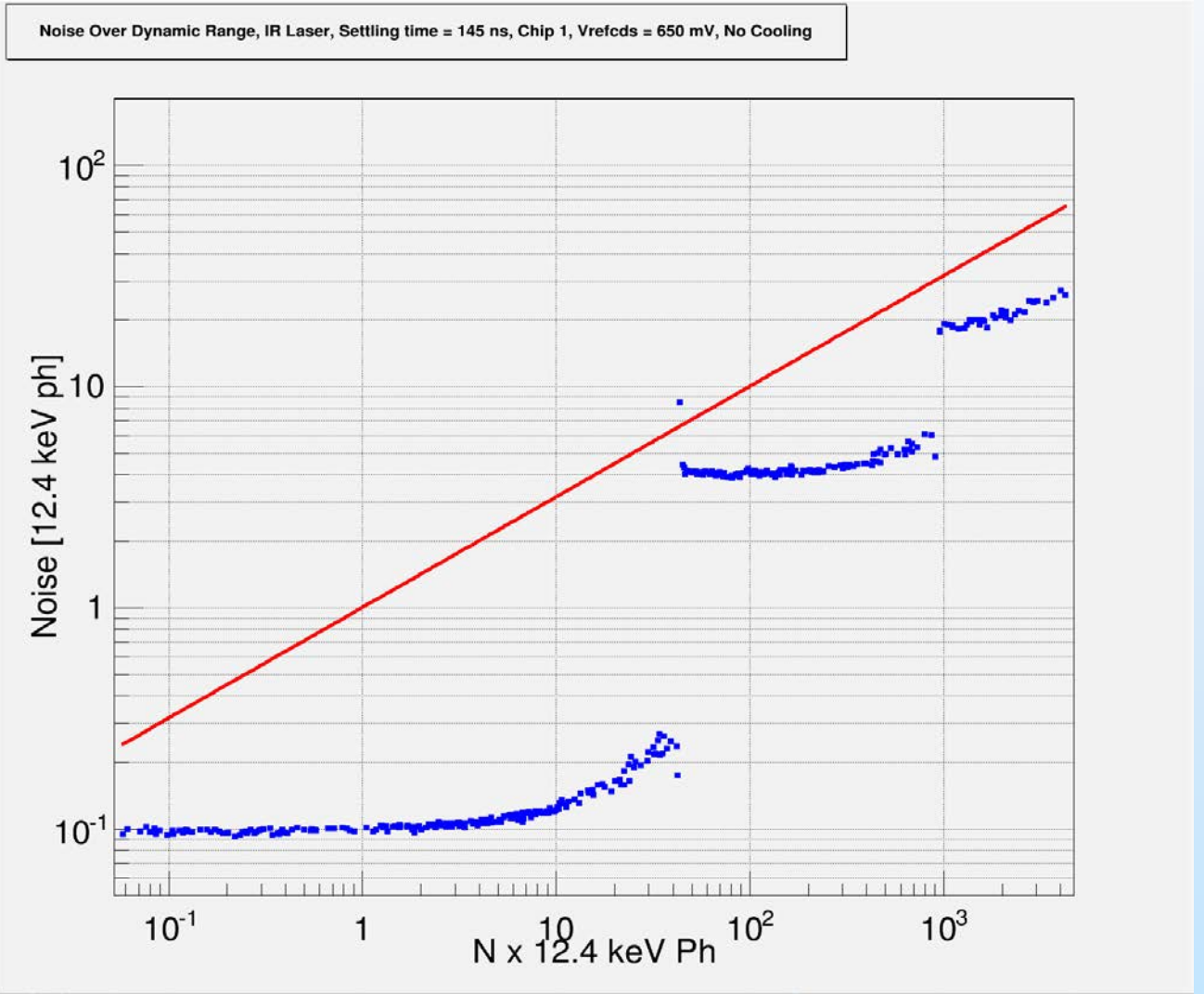
HG/MG = **33.6** (parasitic dominant)
MG/LG = **4.38**

Linearity & Noise over DR - CDS gain LOW

±1%

Poisson Limit

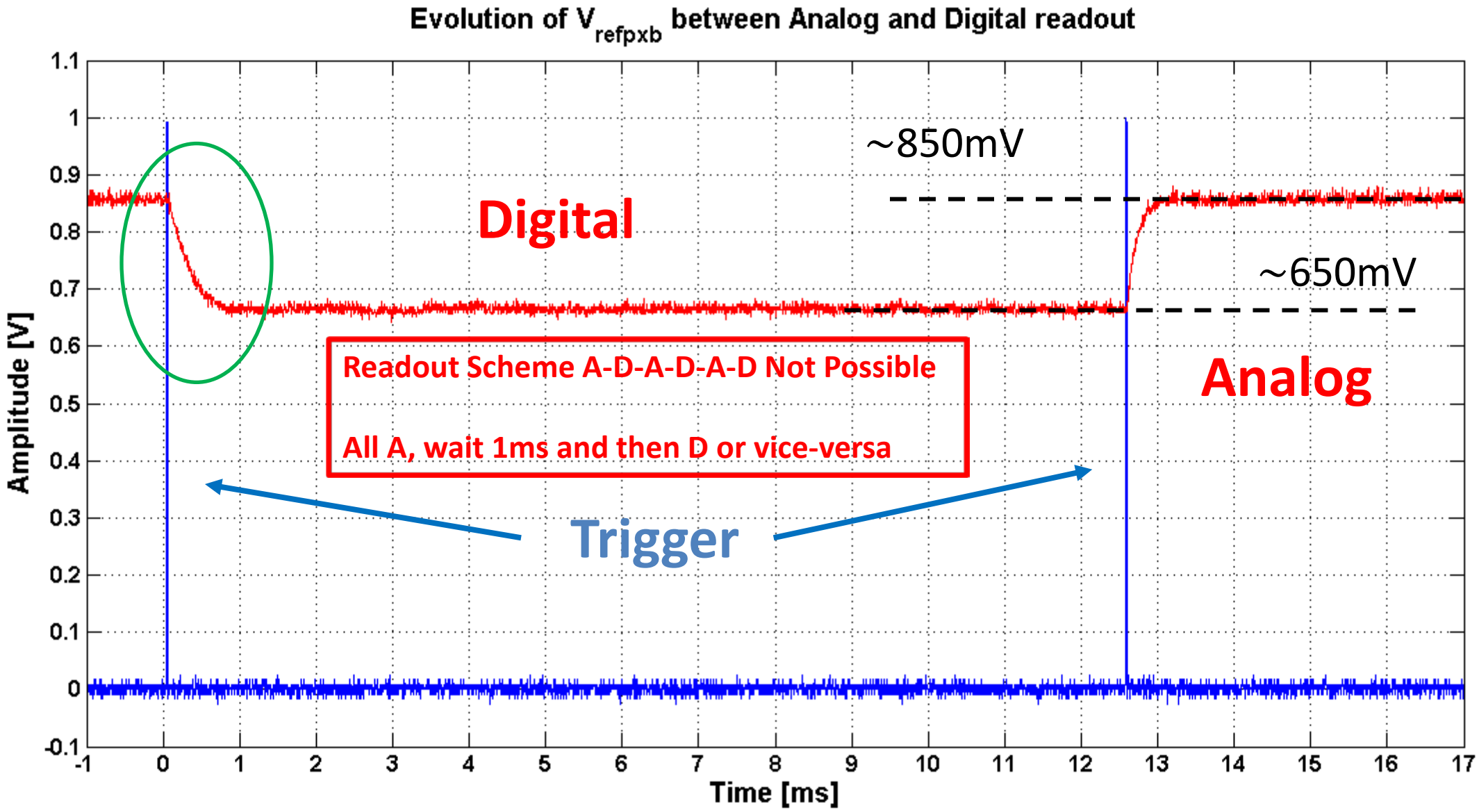




3

Burst Mode – Problem of Vrefpxb speed…

Oscilloscope



4

Droop

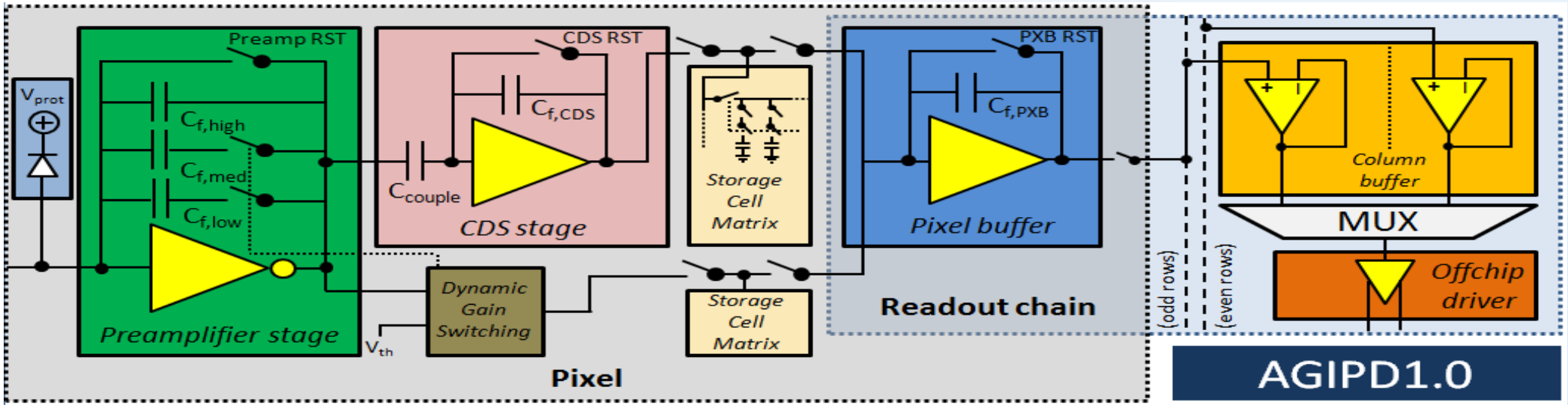
Chip- / Module Probing

Measurement

- After having changed the readout scheme, the ‚precharging' of the bus between Storage Cell and PXB is performed by the front end:

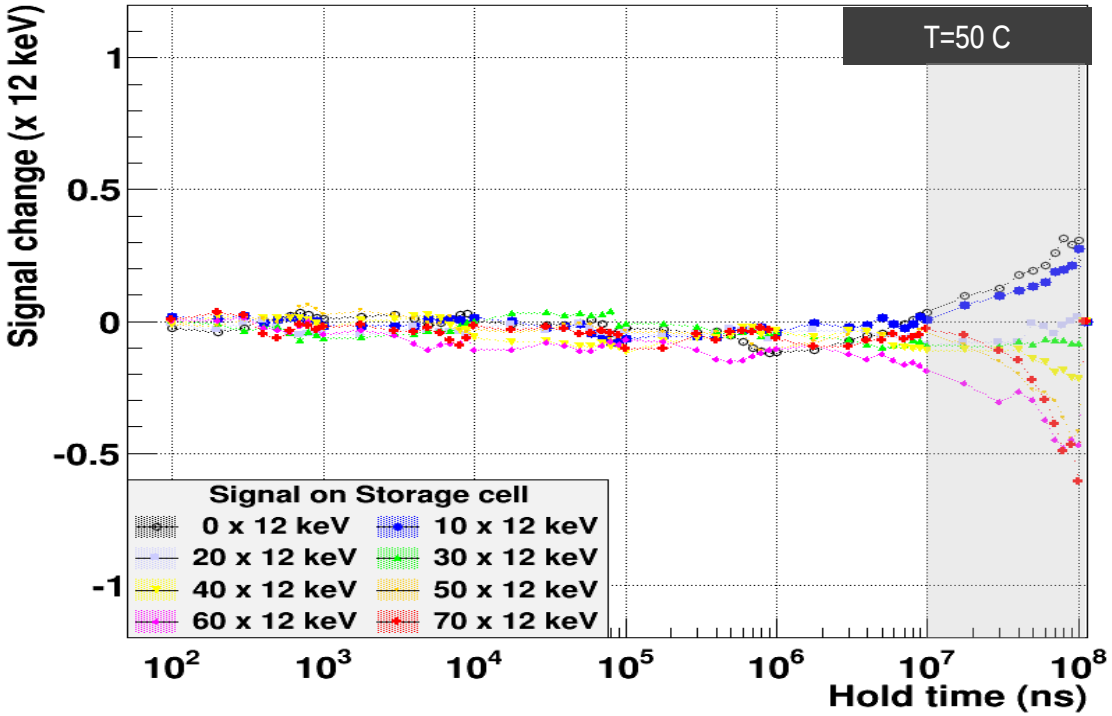
→ Analog Storage Cell Matrix: $V_{ref,CDS}$
→ Digital Storage Cell Matrix: Voltage from voltage divider

- Writing a virtual signal onto storage cell by increasing $V_{ref,CDS}$ and putting CDS buffer in reset
- Setting $V_{ref,CDS}$ back to baseline
- Putting chip into precharge mode (SETMEM)
- Waiting (up to 100 ms – EuXFEL cycle)
- Reading out
- Comparing value after waiting to value without additional hold time

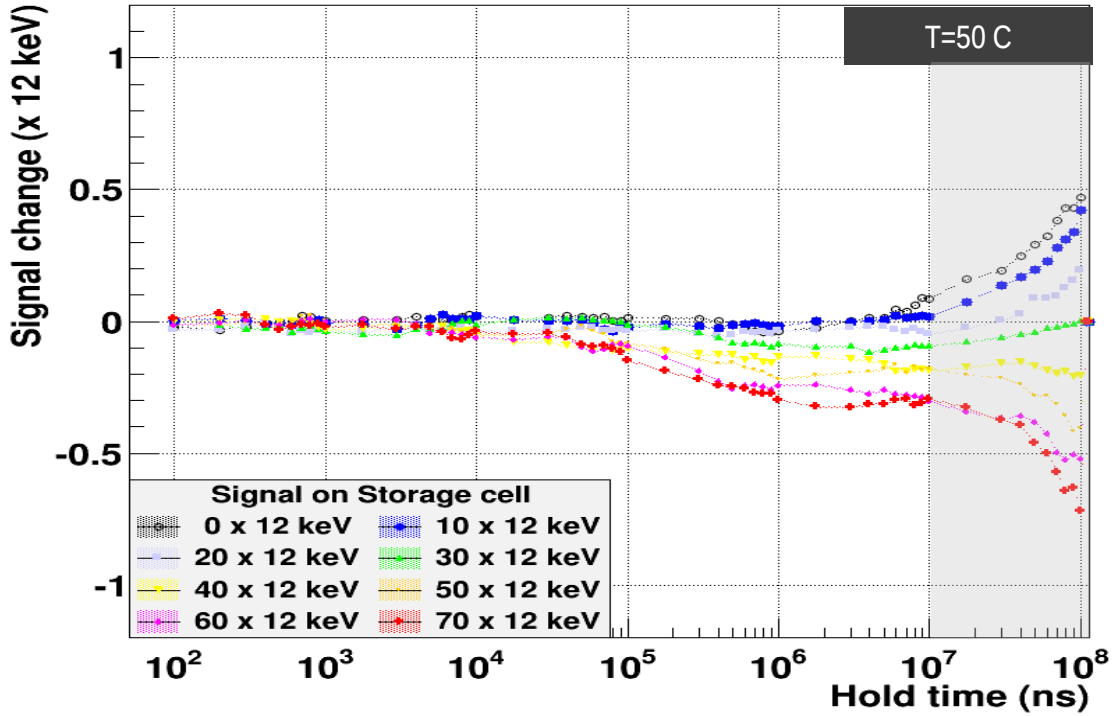


Droop of the analog Storage Cells (T=50 C)

Pixel 325 – Storage Cell 66 - Droop (x12 keV, CDS gain HIGH)



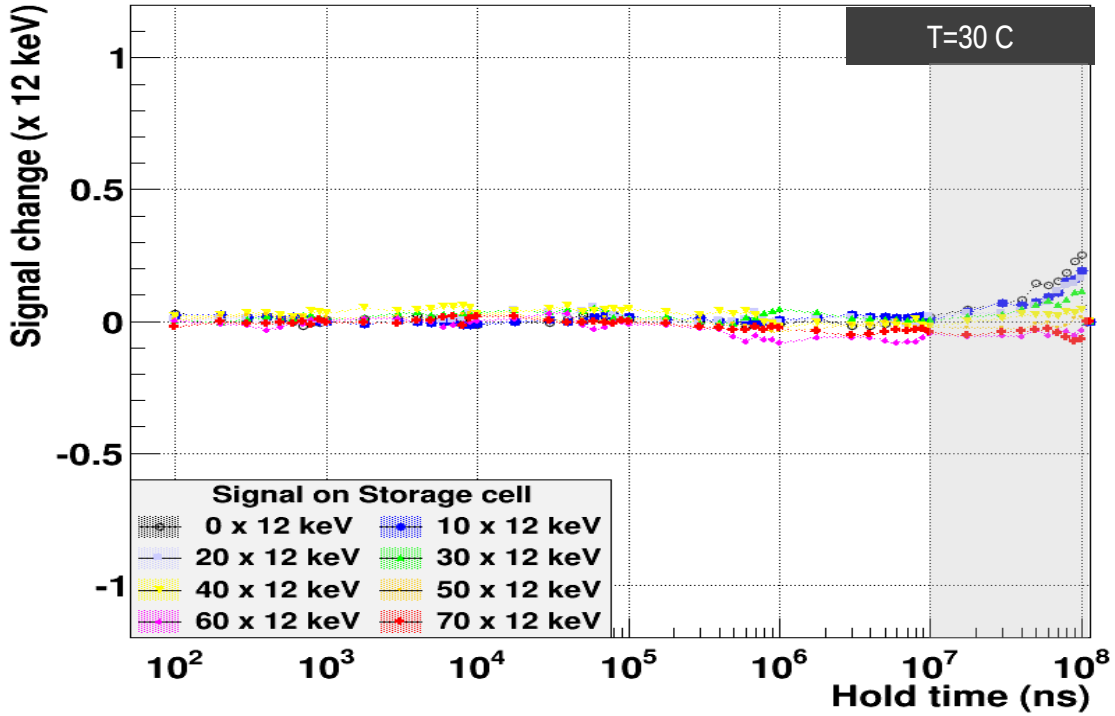
Pixel 1825 – Storage Cell 66 - Droop (x12 keV, CDS gain HIGH)



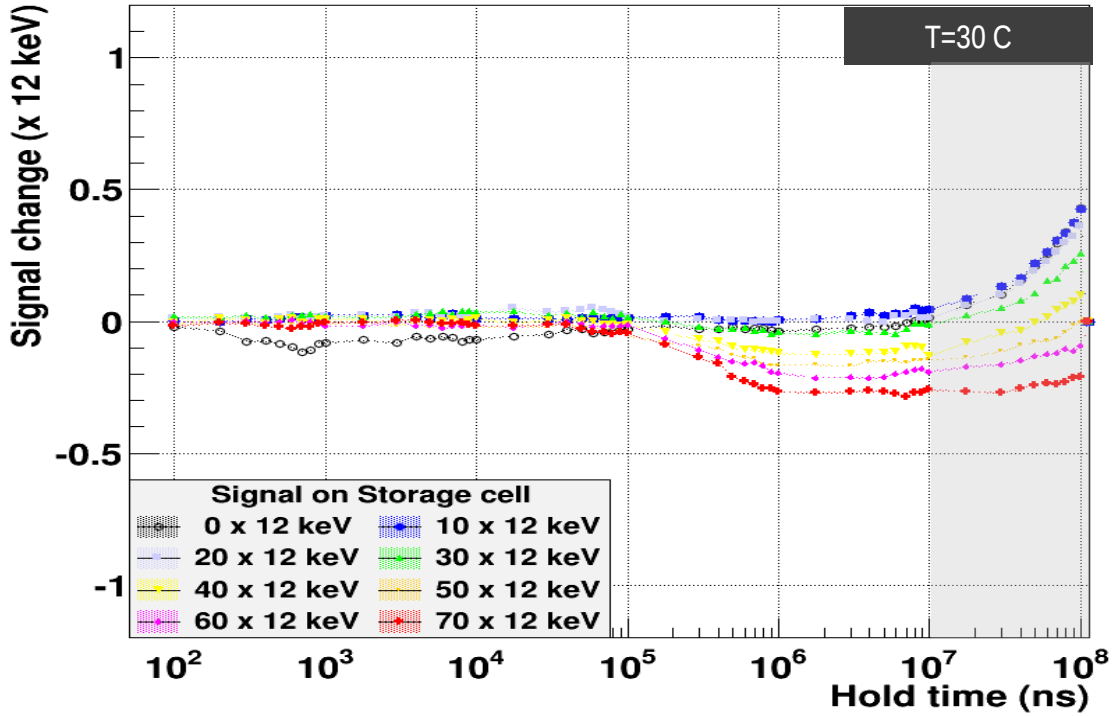
- Typical Hold Time on Storage Cell: 10 – 100 ms (Depending on readout speed
- Two random pixels
- Temperature: 50 C
- Analog signal droops between (-0.6 .. +0.5) x12 keV photons

Droop of the analog Storage Cells (T=30 C)

Pixel 325 – Storage Cell 66 - Droop (x12 keV, CDS gain HIGH)



Pixel 1825 – Storage Cell 66 - Droop (x12 keV, CDS gain HIGH)



- Typical Hold Time on Storage Cell: 10 – 100 ms (Depending on readout speed
- Two random pixels
- Temperature: 30 C
- Analog signal droops between (-0.2 .. +0.4) x12 keV photons

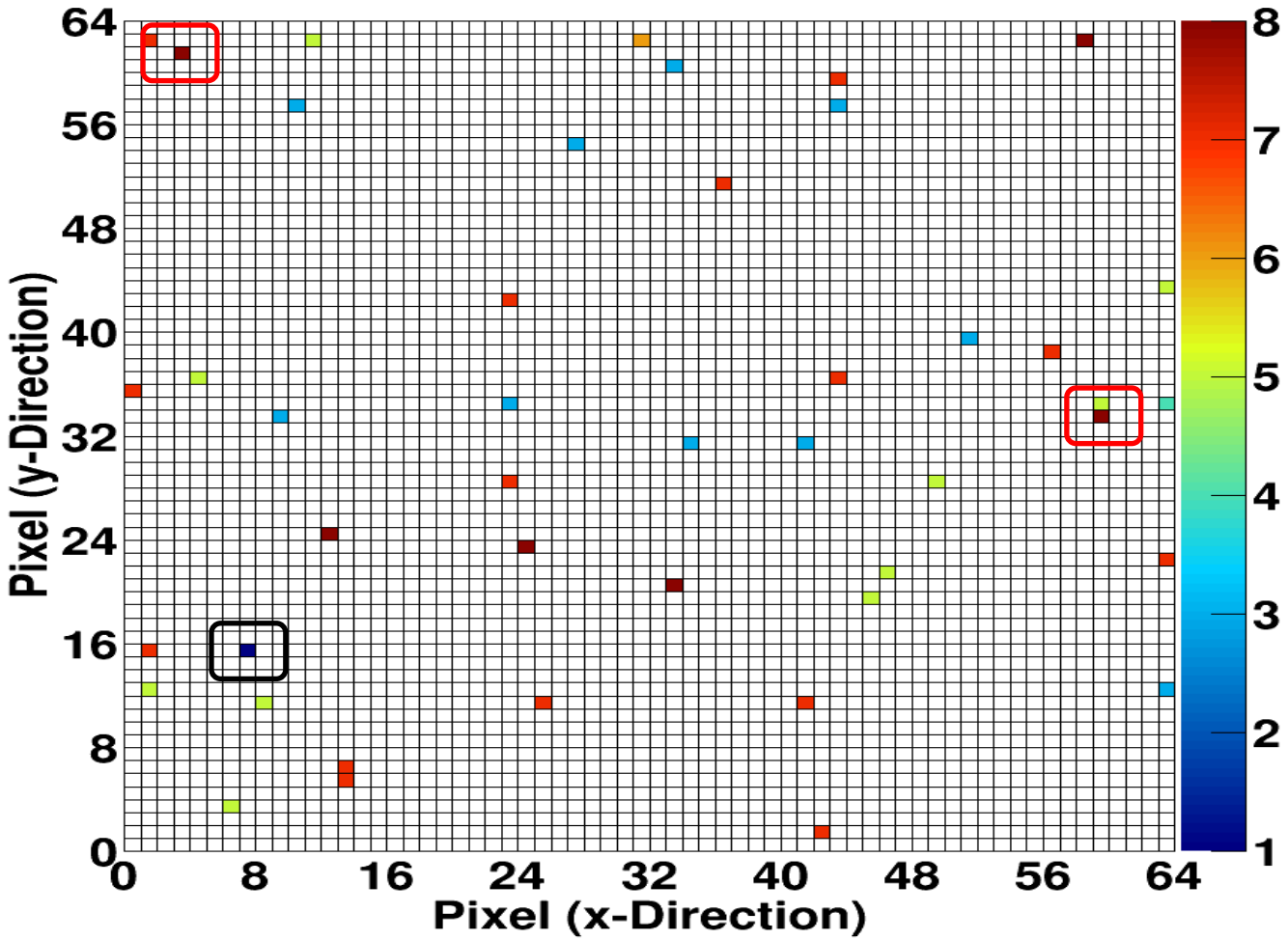
→ Cooling helps dramatically

5

Chip Probing / Bumpbond

Chip- / Module Probing: X-Rays (Mo 17.5 keV)

AGIPD1.0 – Chip001 – Pixel Failure Map

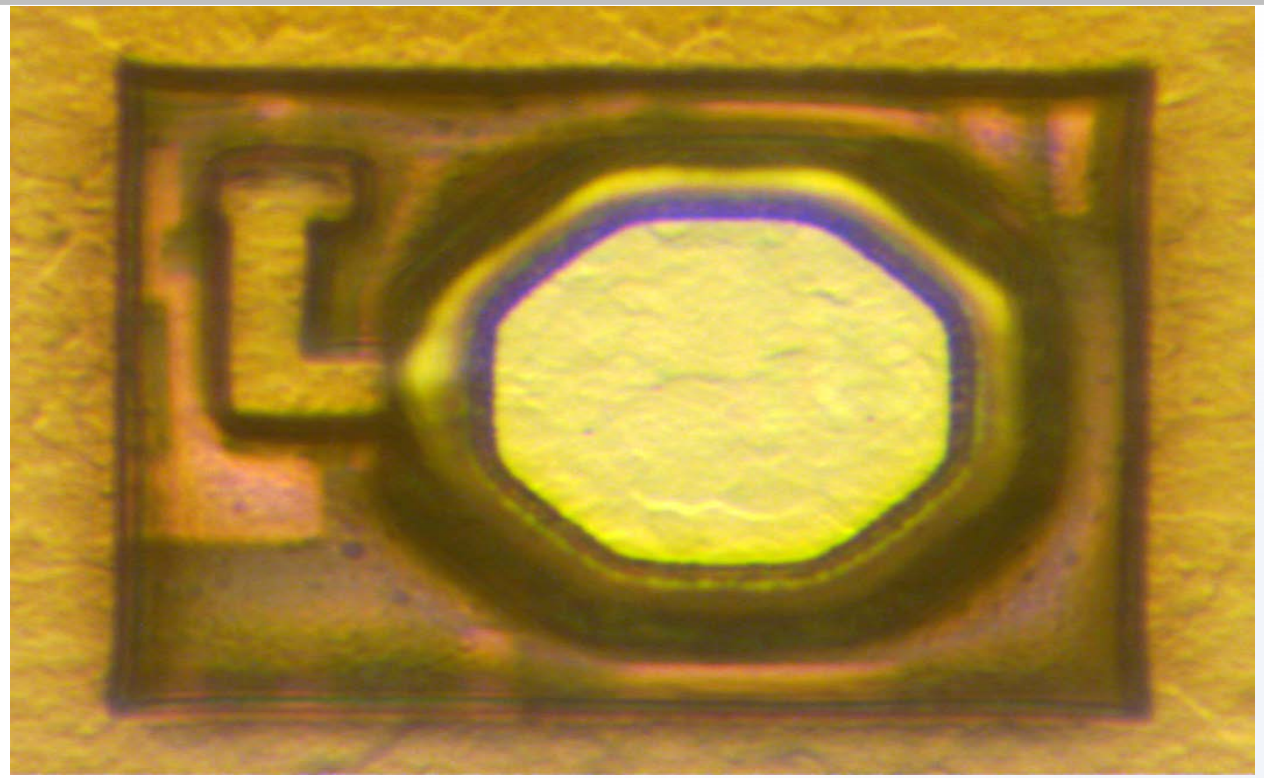


Failure codes:

- Electronically dead
- Testpulse capacitors broken
- Current source (mainly whole SC Rows, potentially crosstalk)
- Storage Cell Row: Failed
- Single Storage Cells: Failed
- Low X-Ray Gain, but working
- ‚No Photon Peak' (e.g. Sensor processing) but baseline off
- Bumpbonding Issue

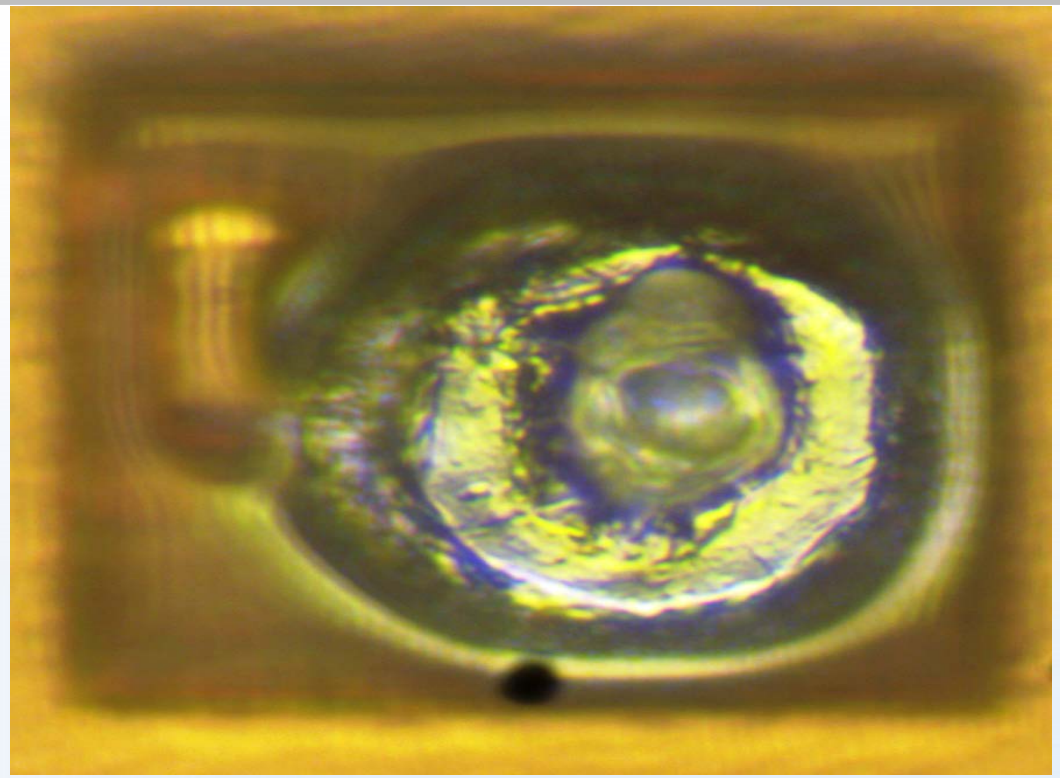
→ 41 Pixels fail due to various reasons
→ 38 Pixel fail the tests with X-Rays, but only 2 of these pixels fail due to bumpbonding
→ Bumpbond Yield: 99.95 %

Chip- / Module Probing: Ripped off module



Processed ASIC – UBM visible

→ No indium on the ASIC side

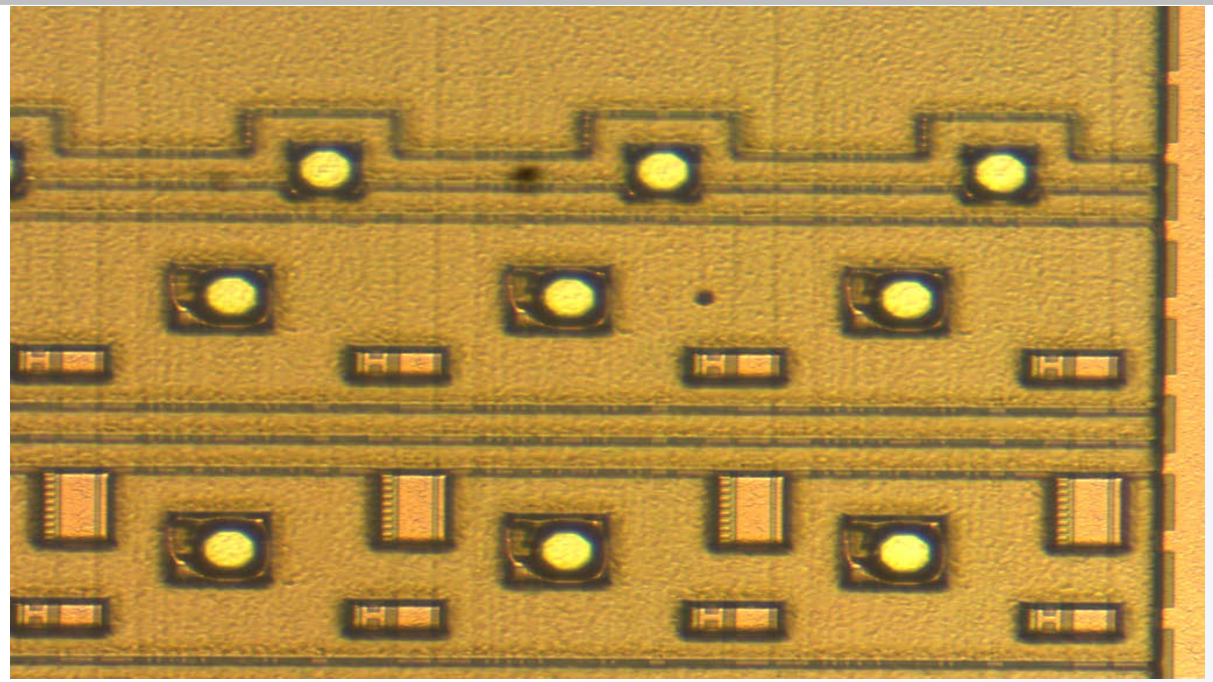


Ripped of ASIC – Indium residuals

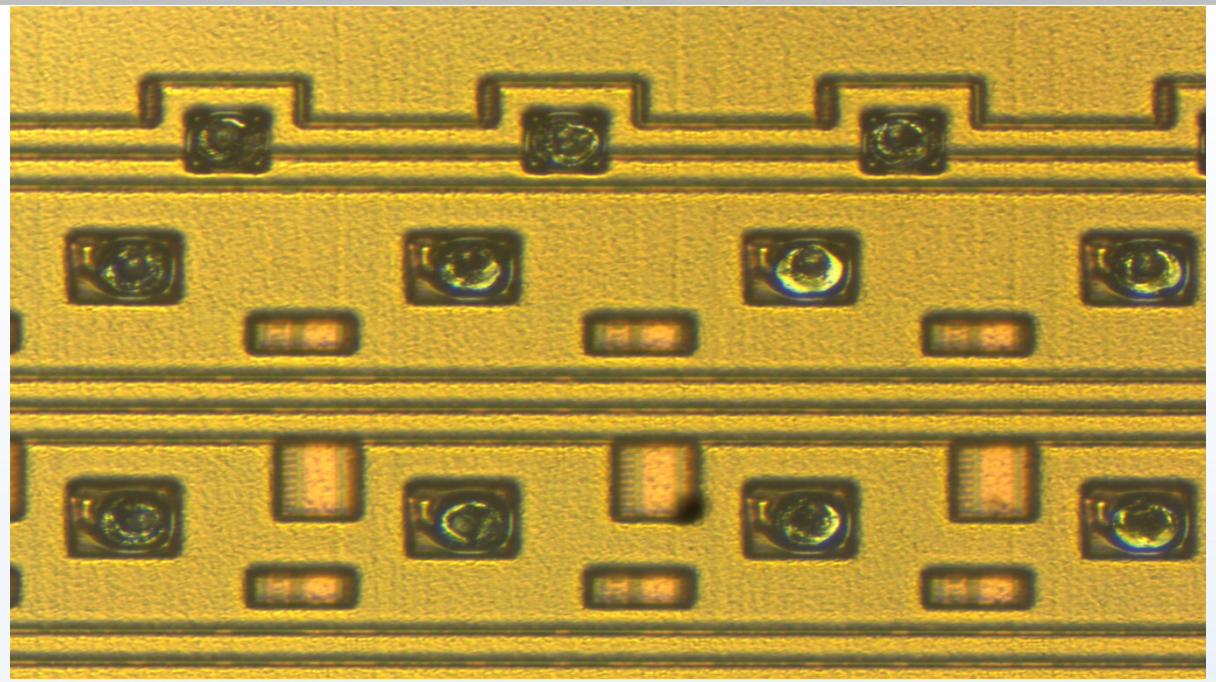
→Indium connection existed

→‚Random‘ point of disruption

Chip- / Module Probing: Ripped off module

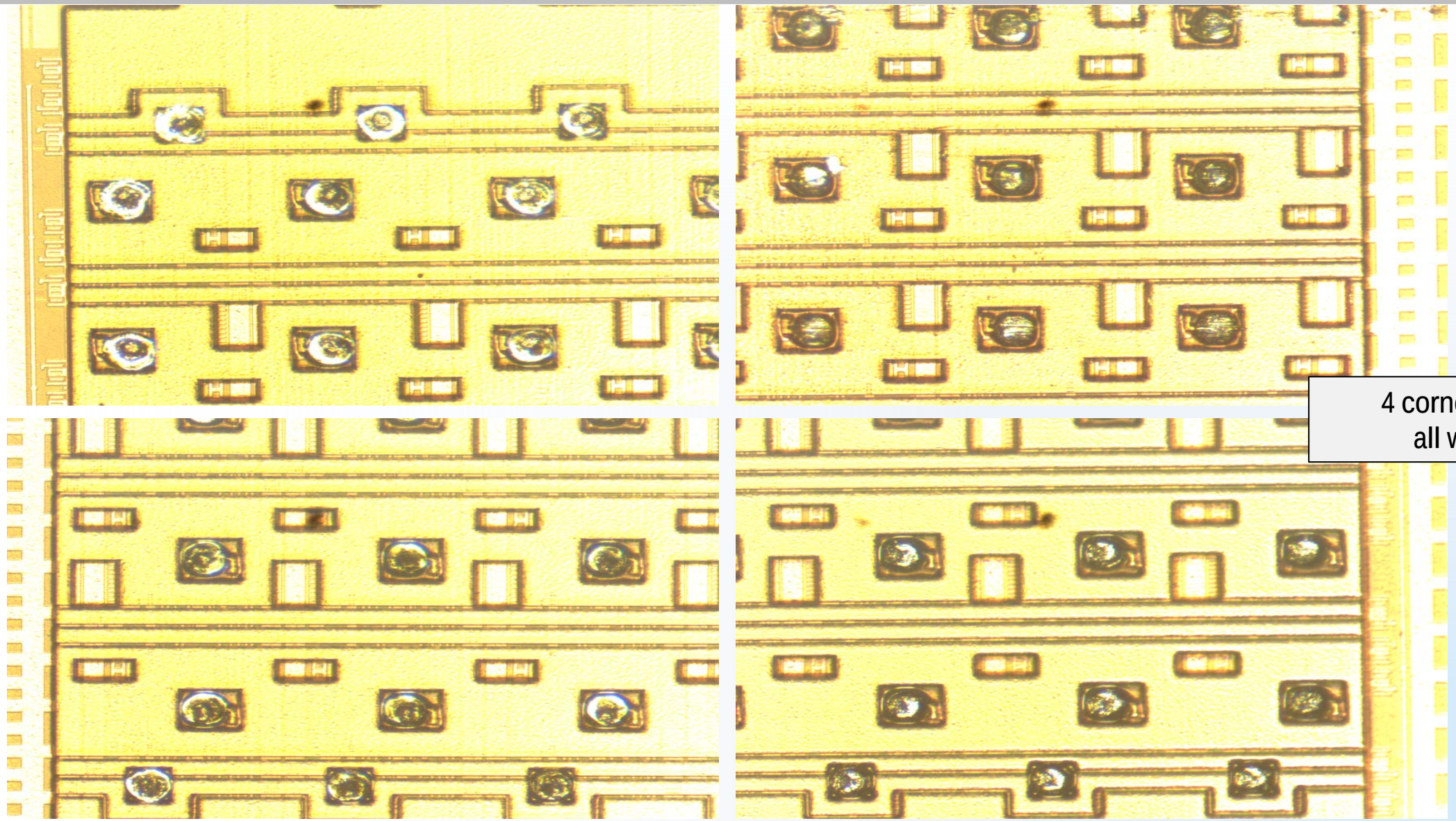


Processed ASIC – UBM visible
→ No indium on the ASIC side



Ripped of ASIC – Indium residuals
→Indium connection existed
→‚Random' point of disruption

Chip- / Module Probing: Ripped off module



4 corners of the module,
all were connected