AGIPD Firmware/Software Development

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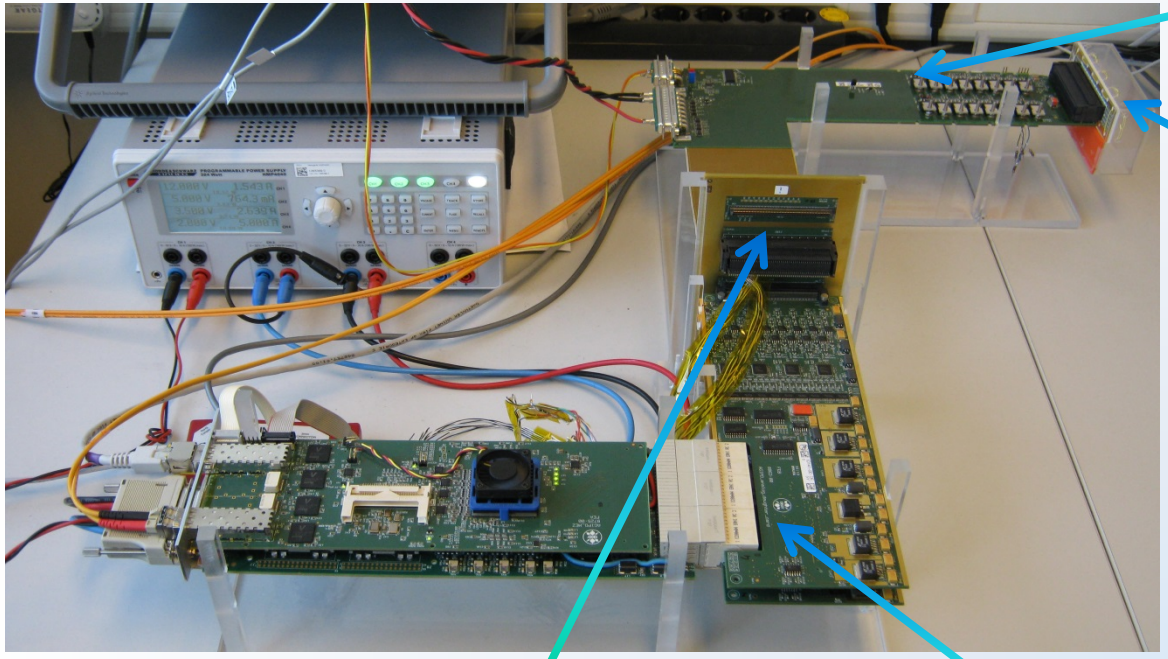
AGIPD Meeting
01-02 April, 2014

Outline

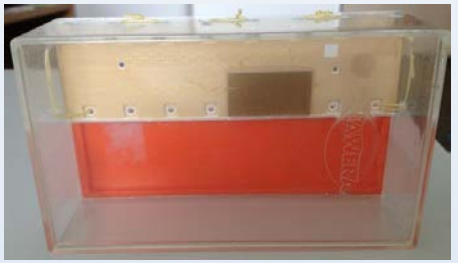
- Reminder: hardware set-up
- FPGA firmware/software development
  - Reminder: concept of AGIPD FPGA firmware/software
  - Standalone DAQ software development
  - Status of FPGA firmware development
- Summary and Outlook

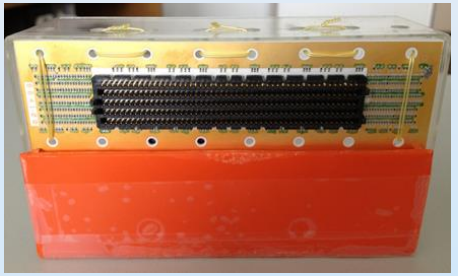
Reminder: Hardware Set-Up



Vacuum board

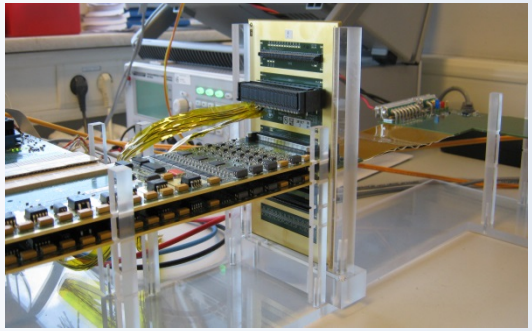
ASICs ceramic board





Digital read out

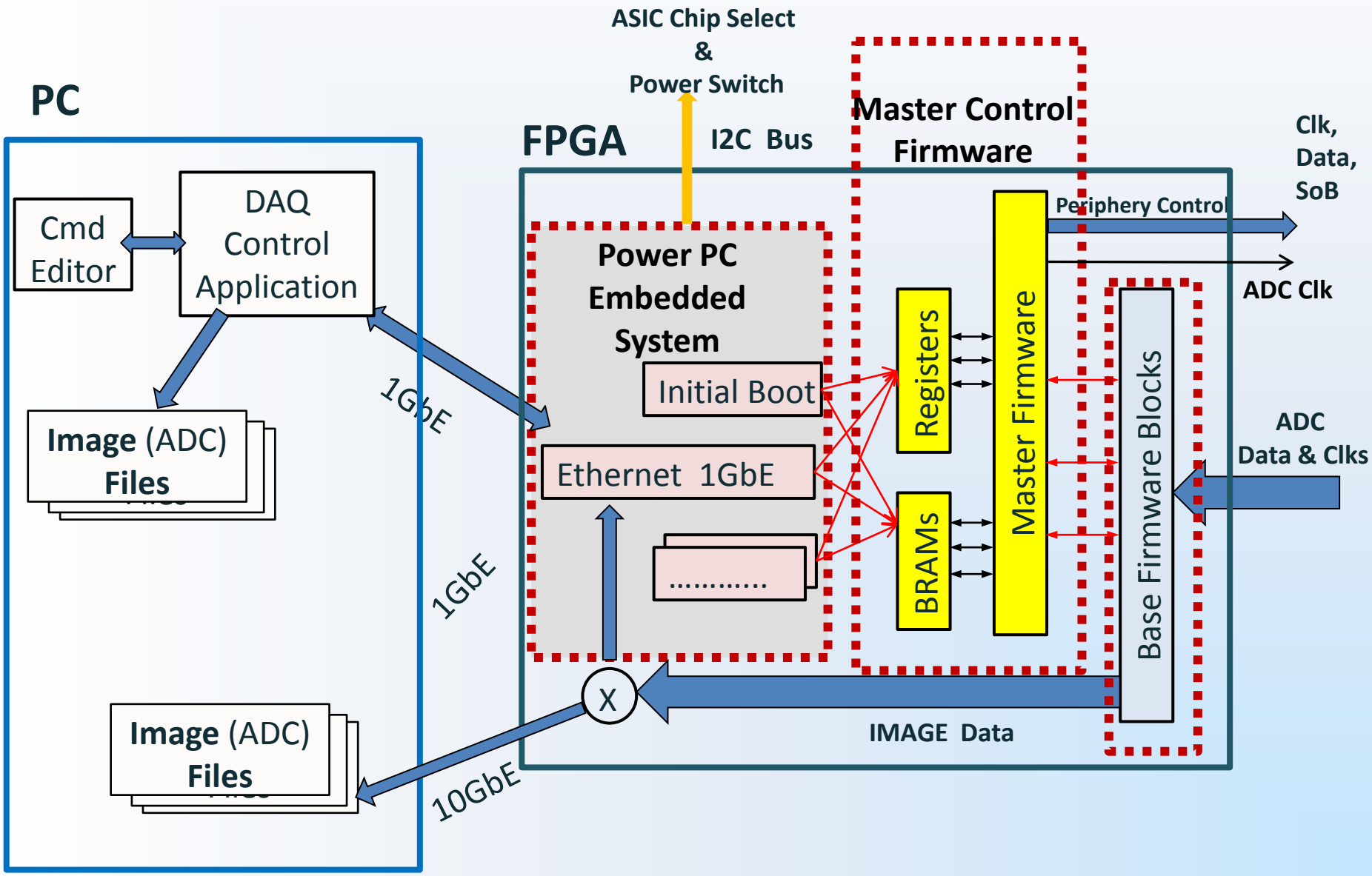
Backplane



Analogue boards

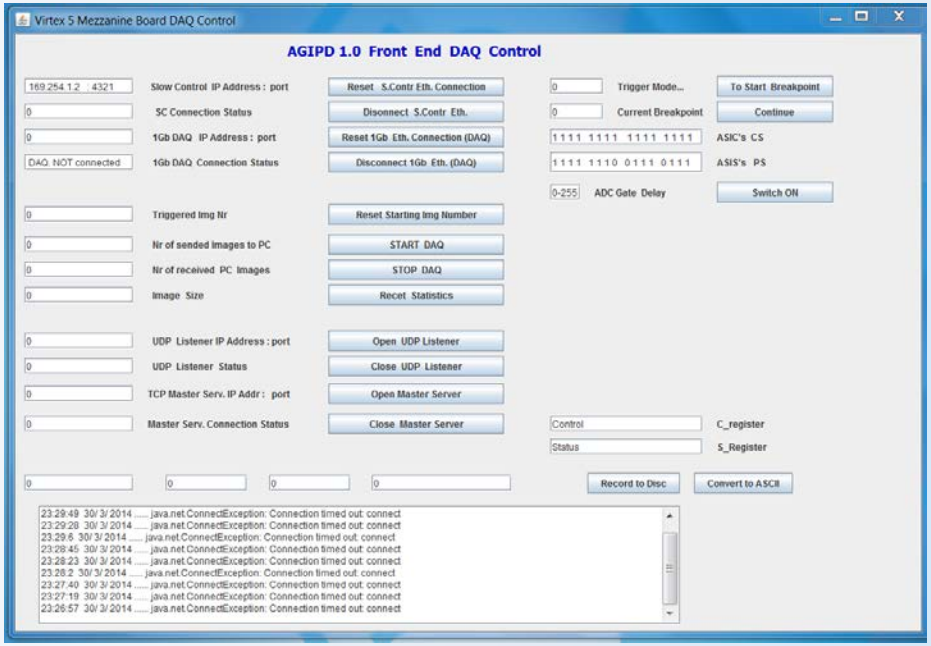
FPGA firmware/software development

Reminder: concept of AGIPD FPGA Firmware/Software



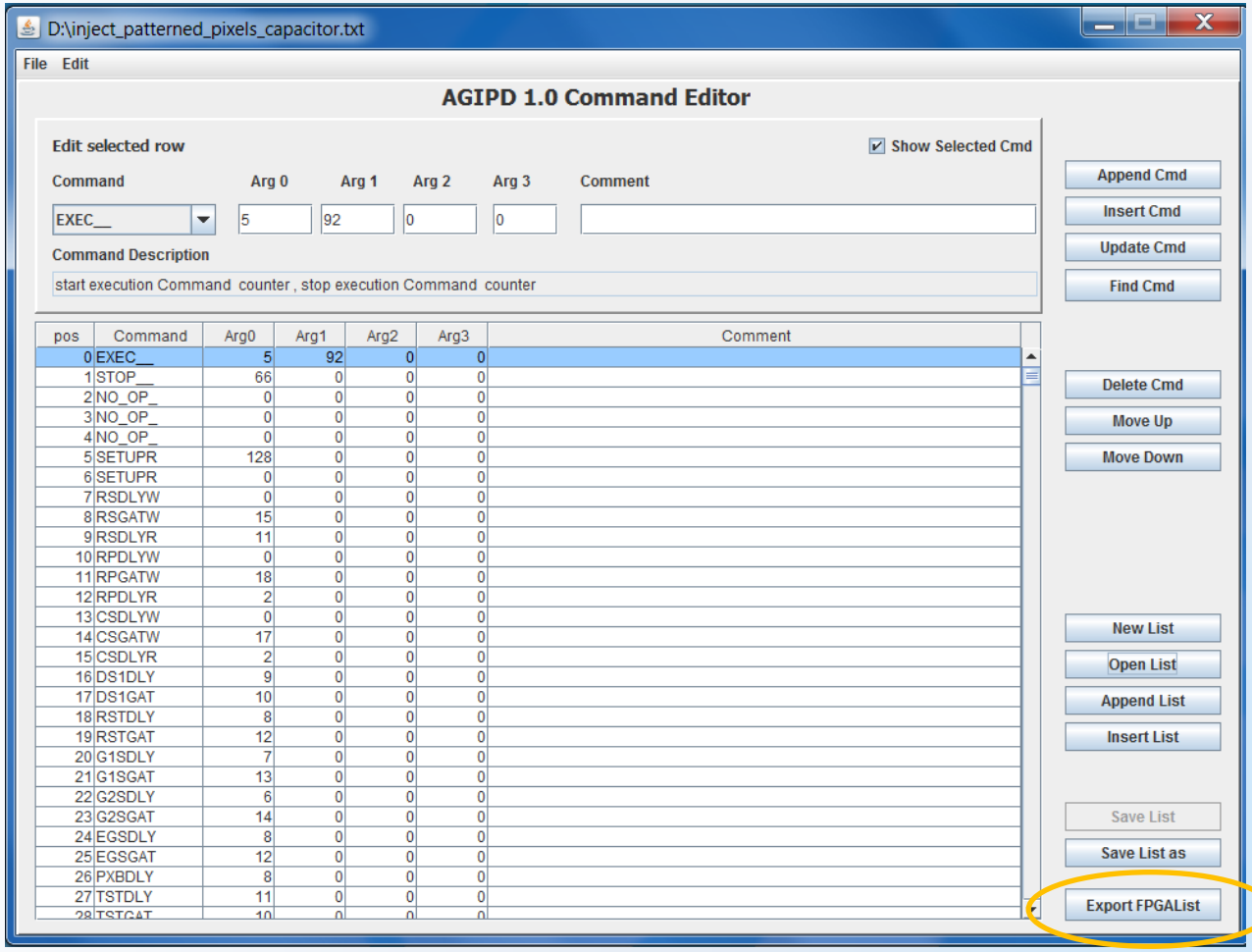
Standalone DAQ software

- DAQ monitor & control application
  - Basic features available: Gigabit Ethernet(TCP/IP) client
    - Triggering and debugging execution of user detector algorithms
    - Receive images packets & assembling image
    - Record image into hard disk (Binary & ASCIIs files)
    - ASICs chip select & power switching
  - Advance functions in debugging and test stage



Standalone DAQ software

- User command editor
  - Added: Sent to FPGA to update user algorithm



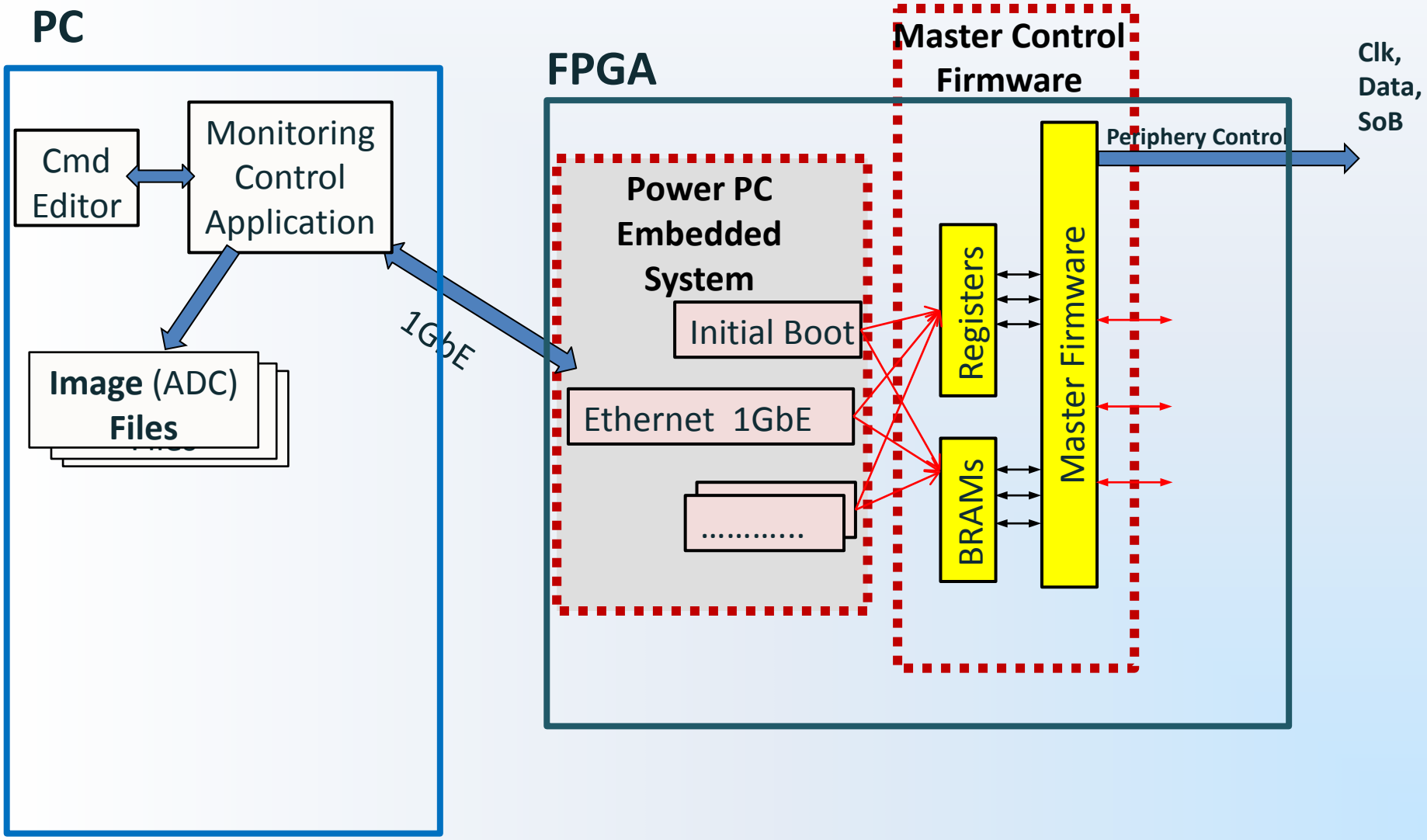
pos	Command	Arg0	Arg1	Arg2	Arg3	Comment
0	EXEC__	5	92	0	0	
1	STOP__	66	0	0	0	
2	NO_OP_	0	0	0	0	
3	NO_OP_	0	0	0	0	
4	NO_OP_	0	0	0	0	
5	SETUPR	128	0	0	0	
6	SETUPR	0	0	0	0	
7	RSDLYW	0	0	0	0	
8	RSGATW	15	0	0	0	
9	RSDLYR	11	0	0	0	
10	RPDLYW	0	0	0	0	
11	RPGATW	18	0	0	0	
12	RPDLYR	2	0	0	0	
13	CSDLYW	0	0	0	0	
14	CSGATW	17	0	0	0	
15	CSDLYR	2	0	0	0	
16	DS1DLY	9	0	0	0	
17	DS1GAT	10	0	0	0	
18	RSTDLY	8	0	0	0	
19	RSTGAT	12	0	0	0	
20	G1SDLY	7	0	0	0	
21	G1SGAT	13	0	0	0	
22	G2SDLY	6	0	0	0	
23	G2SGAT	14	0	0	0	
24	EGSDLY	8	0	0	0	
25	EGSGAT	12	0	0	0	
26	PXBDLY	8	0	0	0	
27	TSTDLY	11	0	0	0	
28	TSTGAT	10	0	0	0	

Status of AGIPD FPGA Firmware Development

- Things are done and working!
  - Power PC TCP/IP Server ←→ DAQ Monitor and Control software
  - Command interpreter (3-Lines periphery interface) ←→ Command sequence
  - 64 channels ADC readout (*fine tuning for every FPGA board?)
  - Record images data into DDR2 memory (Power PC DMA Engine)
  - Transmit image data via TCP/IP Gigabit Ethernet
  - AGIPD 10G standalone module: Faked data emulating AGIPD image structure →DDR2 Memory→ 10G Gigabit Ethernet
  - I2C control for ASICs chip select and power switch

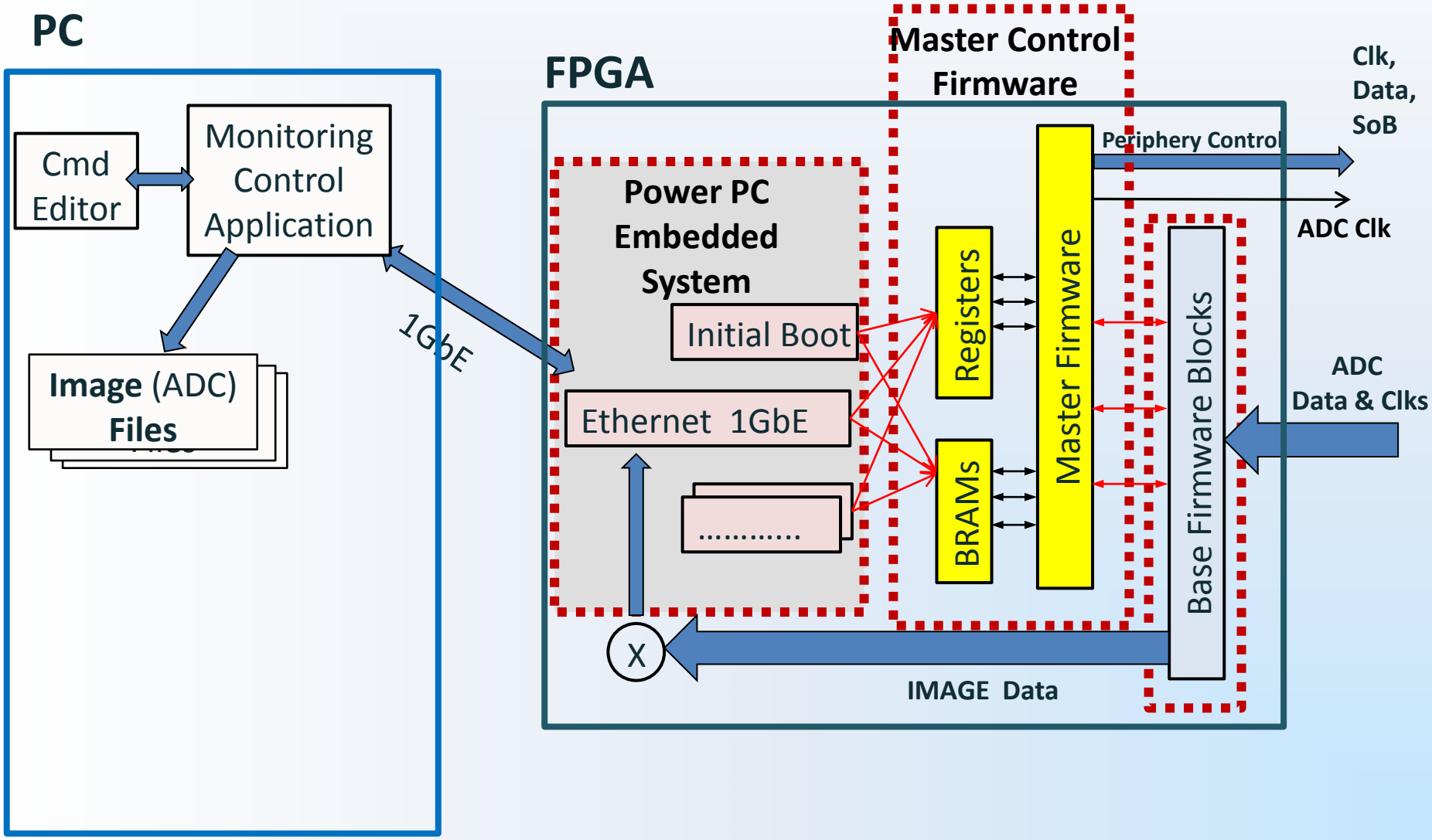
Status of AGIPD FPGA Firmware Development

- Talk to the ASIC periphery interface



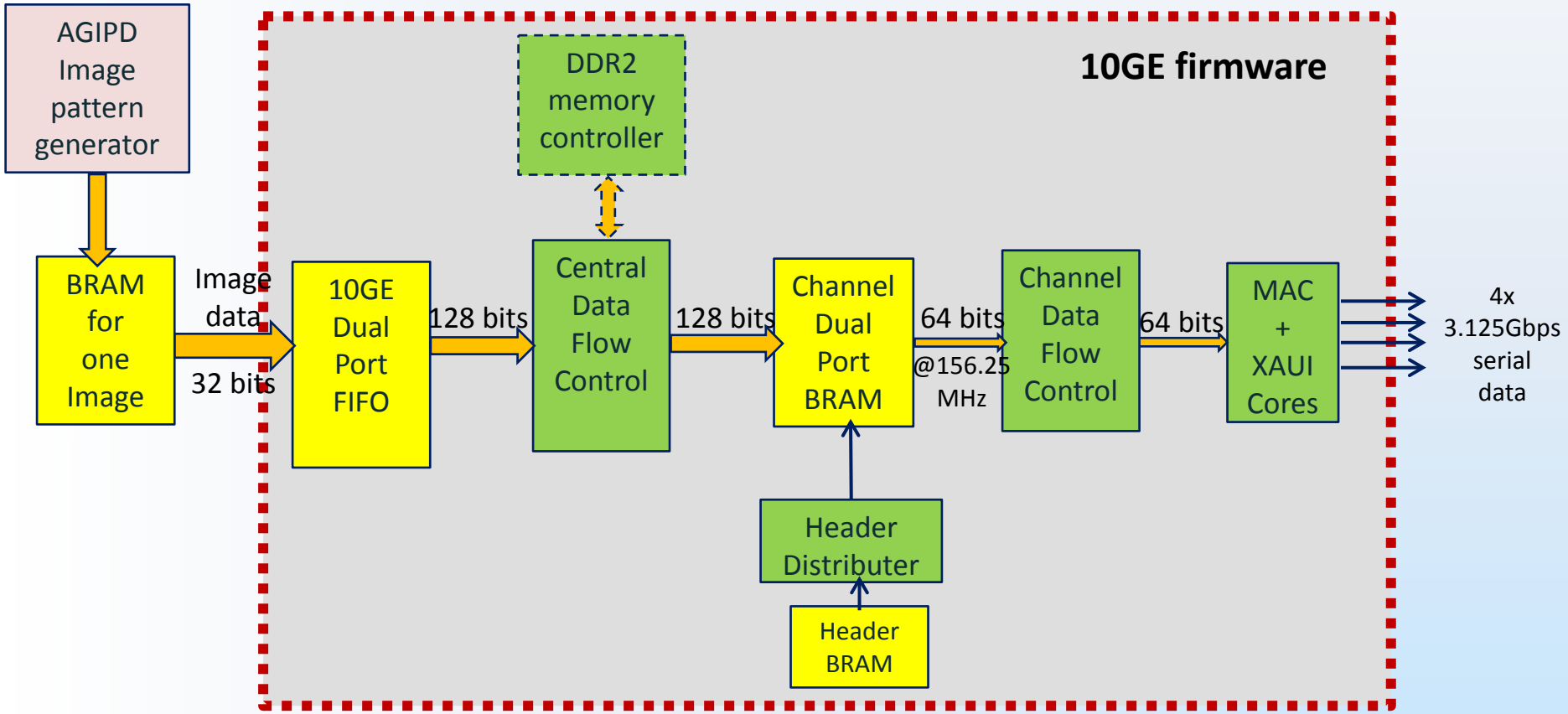
Status of AGIPD FPGA Firmware Development

- 64 Channels ADC image data readout



Status of AGIPD FPGA Firmware Development

- Standalone 10G Channel



Summary & Outlook

Status and Summary

- Standalone DAQ system development
  - Basic features available: Gigabit Ethernet TCP/IP server
    - Triggering and debugging execution of user detector algorithms
    - Receive images packets & assembling image
    - Record image into hard disk (Binary & ASCIIs files)
    - ASICs chip select & power switching

- FPGA Firmware
  - Power PC TCP/IP Ethernet Client ←→ PC DAQ System
  - Command Interpreter (3-Lines ASIC periphery interface) ←→ Command Editor
  - 64 channels ADC readout (image data)
  - Record images data into DDR2 memory (Power PC DMA Engine)
  - Transmit image data via TCP/IP Gigabit Ethernet
  - I2C control for ASICs chip select and power switch
  - AGIPD 10G standalone module: Faked data emulating AGIPD image structure →DDR2 Memory→ 10G Gigabit Ethernet

Things to do

- Preparation for beam test in APS in June
  - Shipping list cross check with FS-DS
- Standalone DAQ system
  - More user friendly and simplified GUI interface
  - 10G UDP listener test
- FPGA Firmware
  - Understanding the instability of ADC readout (hardware? Firmware?)
  - Fine Tuning of ADC synchronization with ASIC command
  - Pattern A,B,C tests (command editor templates)
  - 10G module integration
  - APS conditions (trigger, timing, …) adaption
- Hardware debugging

AGIPD Software/Firmware Development

Thank You!

AGIPD Software/Firmware Development

Spare

Slides