AGIPD Full DAQ Chain Test

(16 ASICs module)

Very new FW & SW

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Command interpreter module

External Control

Triggers:
GUI,
Signals

Control messages
TCP IP message
or , pipe, file.

Command interpreter running in FPGA providing accurate timing for the command execution with 1 clk period granularity

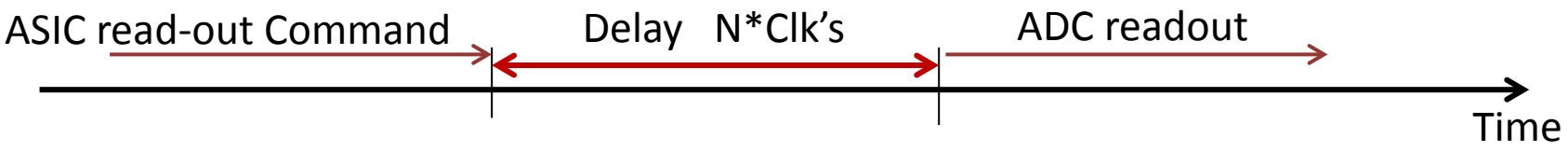
Program consist of AGIPD periphery control commands ++

Defines output data flow

to Ethernet Module

Real time reconfiguration algorithms, even reloading the code is possible !

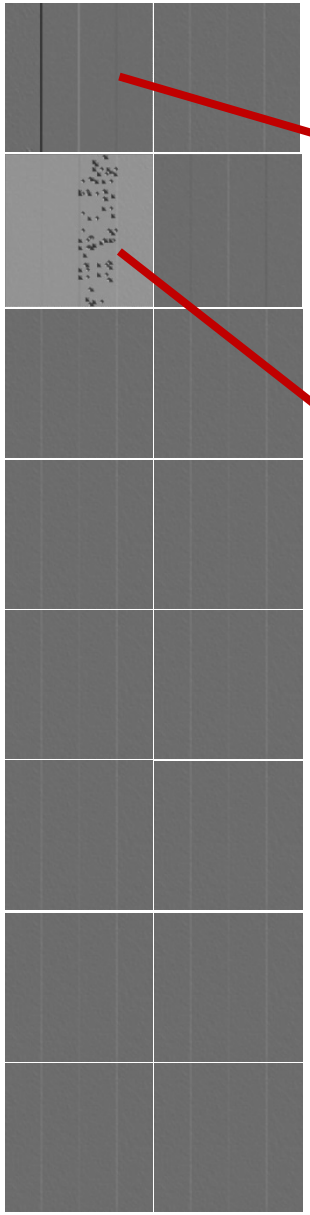
Example:

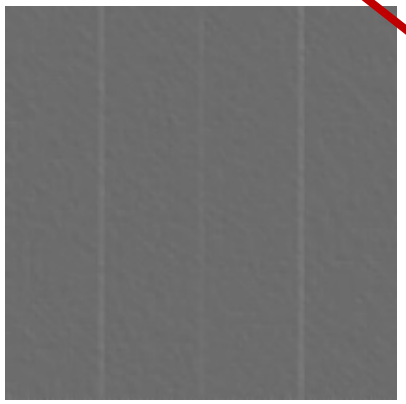


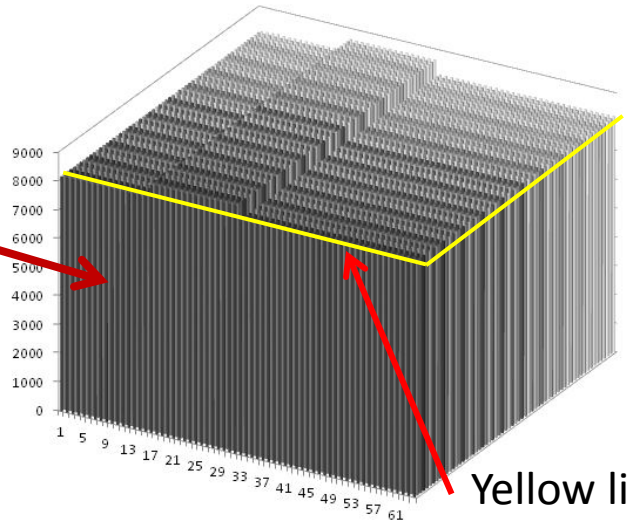
I.Shevyakov AGIPD meeting 01.04.2014

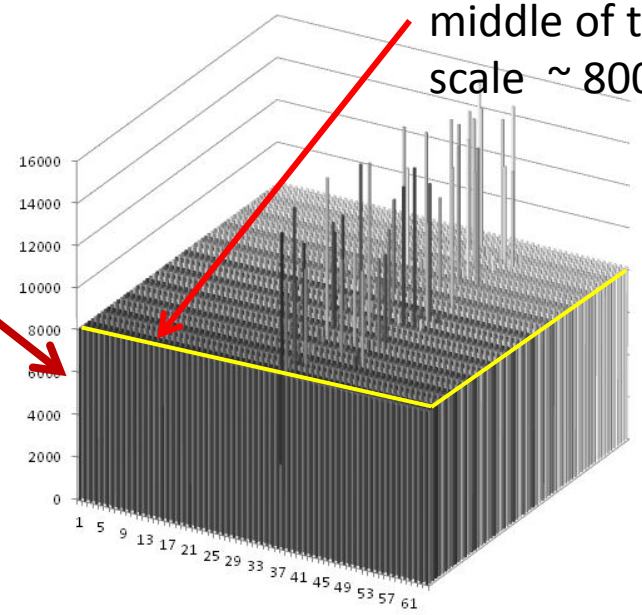
ADC Piedestals , (ASIC‘s power OFF)

Readout Clk: 33.3 MHz





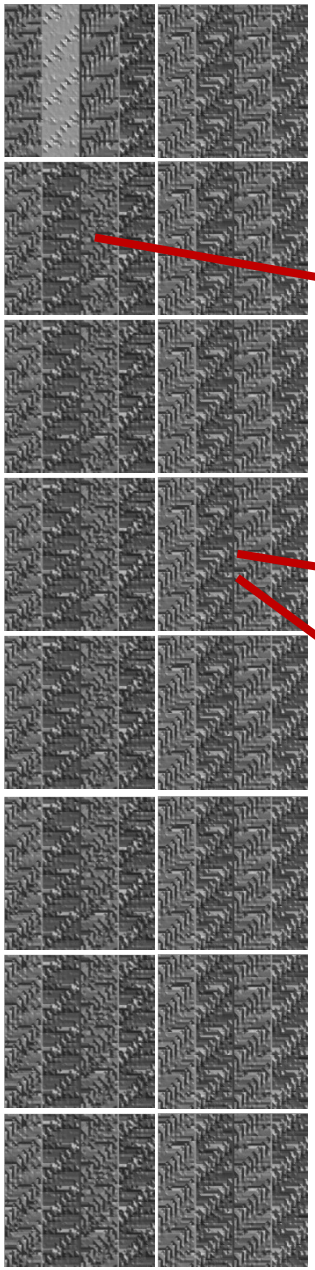


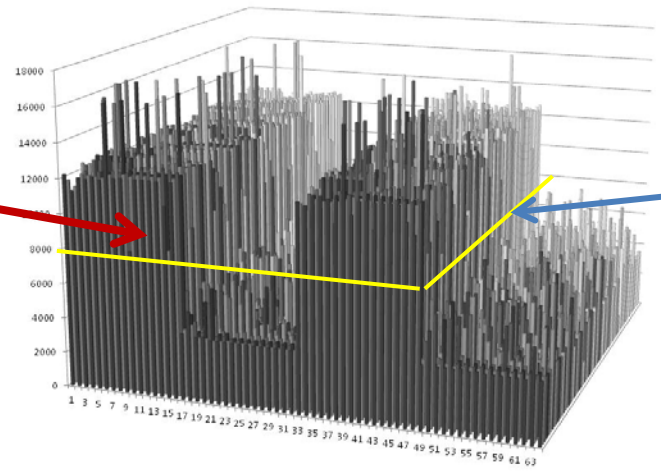


Yellow lines is a middle of the ADC scale ~ 8000 ac

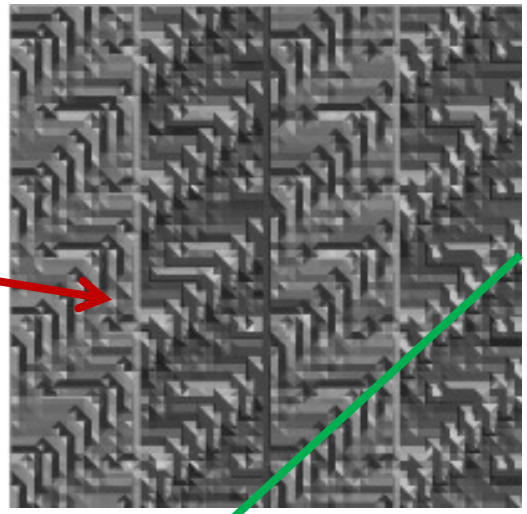
Pattern (Pixels) TP Capacitor Injection mode

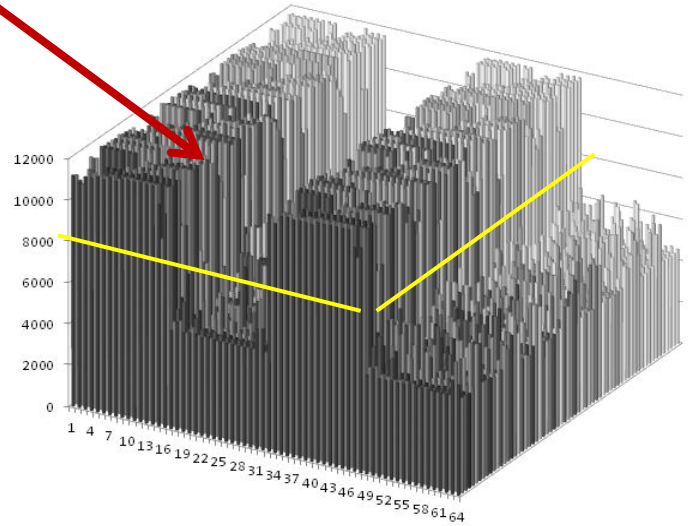
Readout Clk: 33.3 MHz





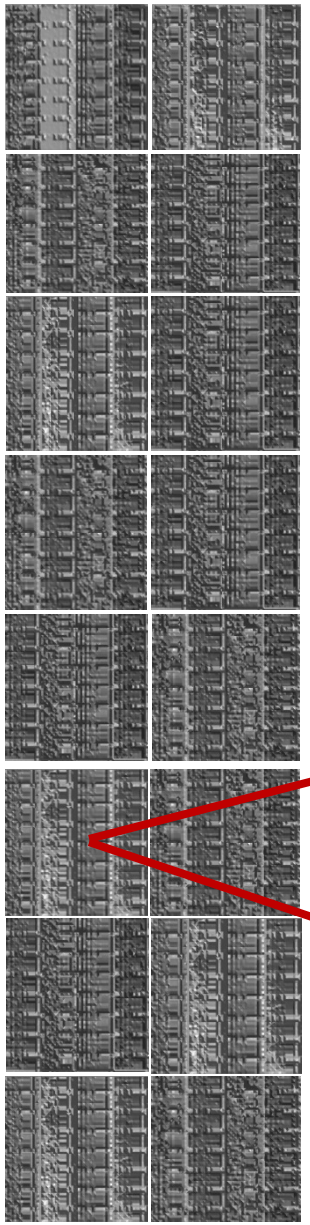
Yellow line is a middle of the ADC scale ~ 8000 ac



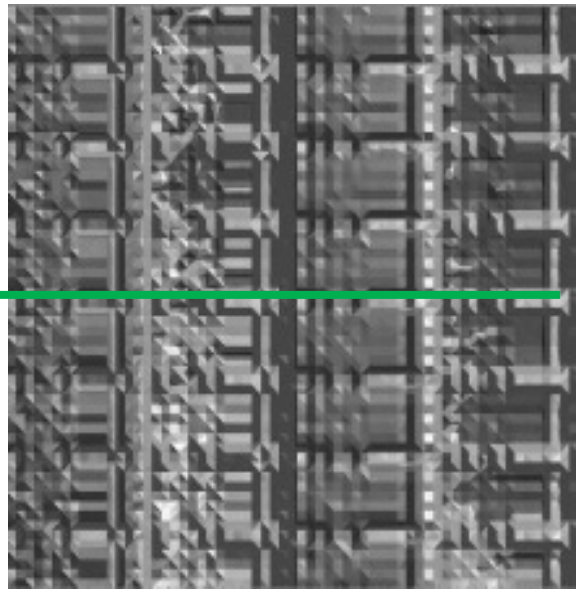


Patterns have some slope -> ADC dada have an offset ?

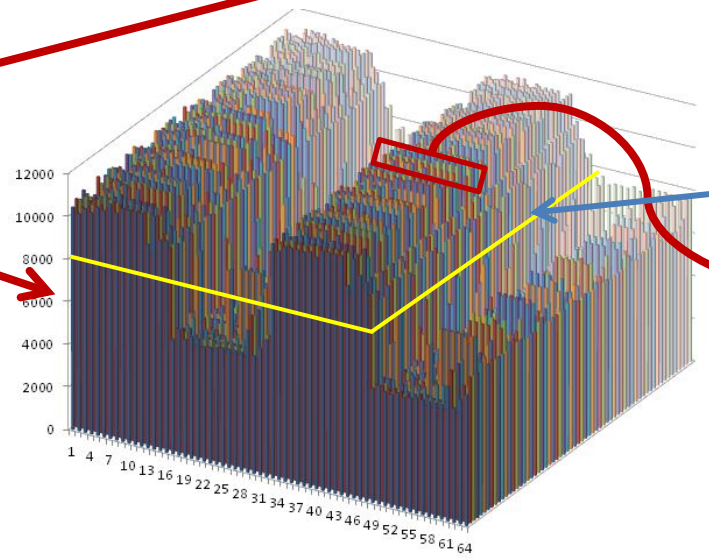
ADC readout gate tuning (timing , width)



Readout Clk: 33.3 MHz



Patterns has the horizontal alignment



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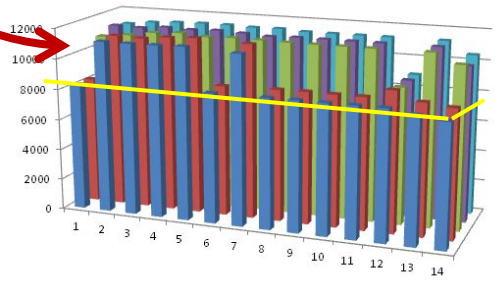

Summary

- ADC Readout requires further fine tuning (basically timing)
- FPGA Command interpreter working reasonable or fine
- Full DAQ chain with 1GbE and backend data recording is OK
- Offline processing now really required