# WP2.4 : Interface electronics


Peter Göttlicher

AGIPD consortia meeting
PSI, April 4th 2012

HELMHOLTZ ASSOCIATION

# Outline

- General setup

- EMI/Grounding as planned for circuits/layouts/system
- Power supplies

- Analogue part
- Digital part
- Backplane
- Quadrant

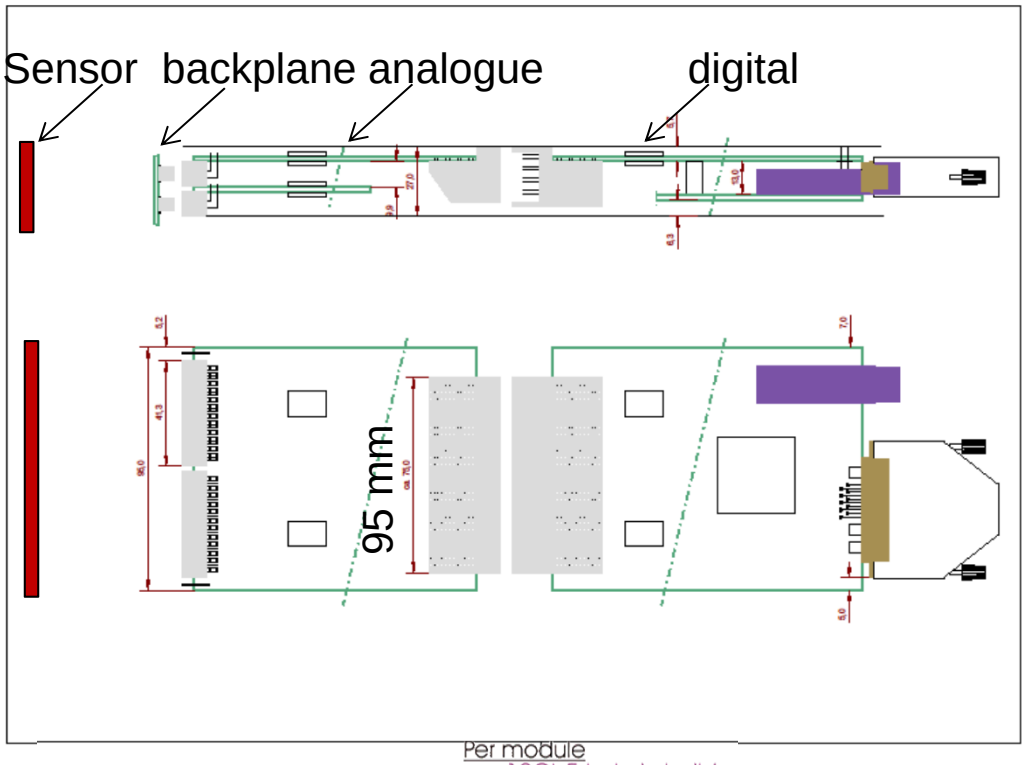
- Reject handling
- Train builder activities

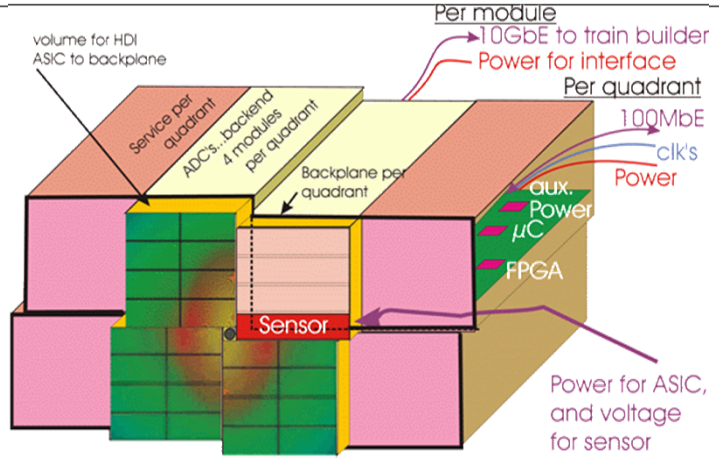
- Summary/Outlook

# General setup

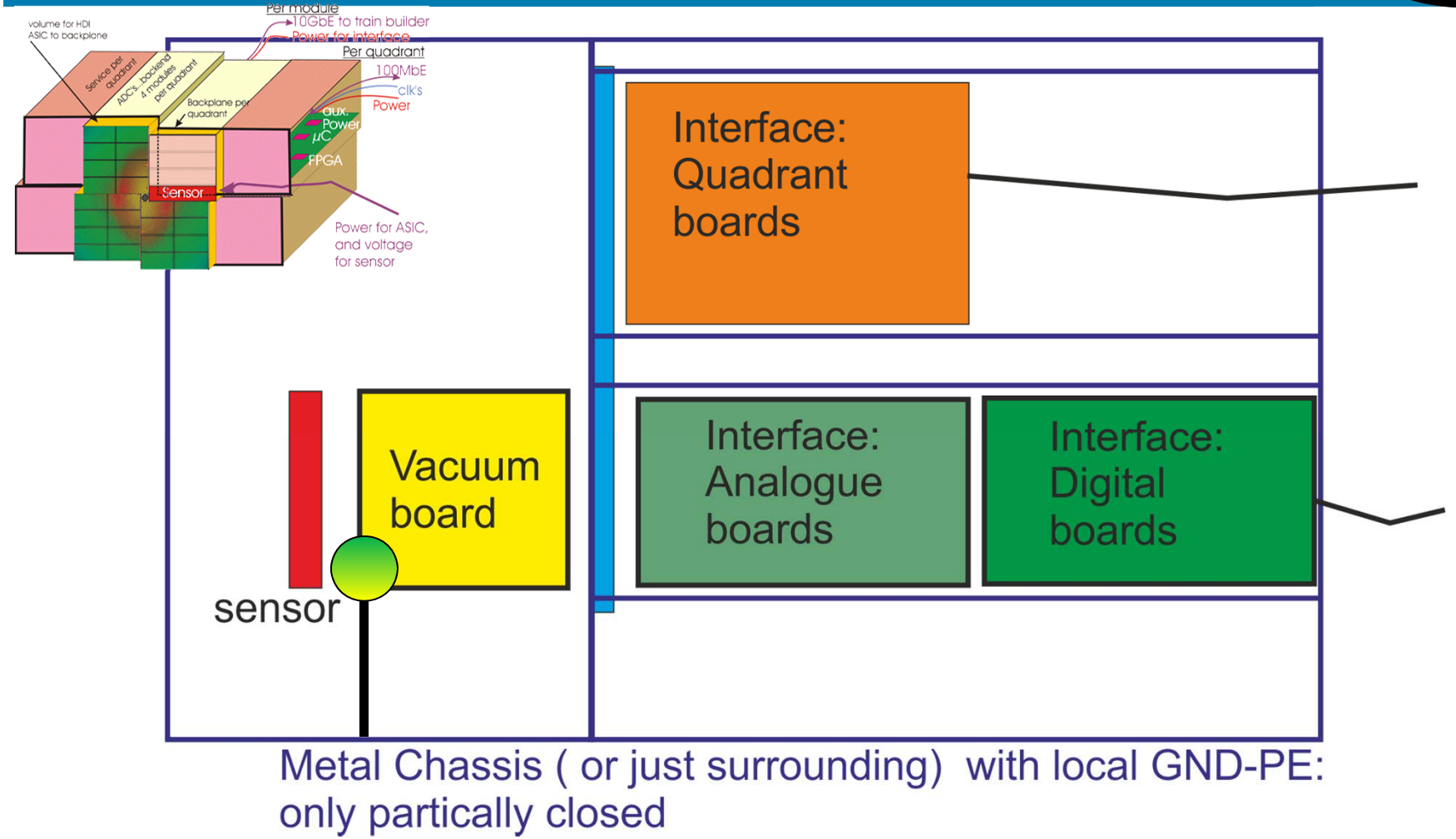
## Interface electronics:

- Two boards for analogue to allow compact analogue line for 64 channels.
- Two boards for digital part to profit from “common” developments.
- Backplane to guide signals to the side. At quadrant level control gets control electronics installed.
- Fit everything behind sensor
  Allow space for rail at the side.
- From XFEL: C&C
  Continuous system-clk : 99MHz
  bunch clk: 4.5MHz with jumps
  bunch-reject



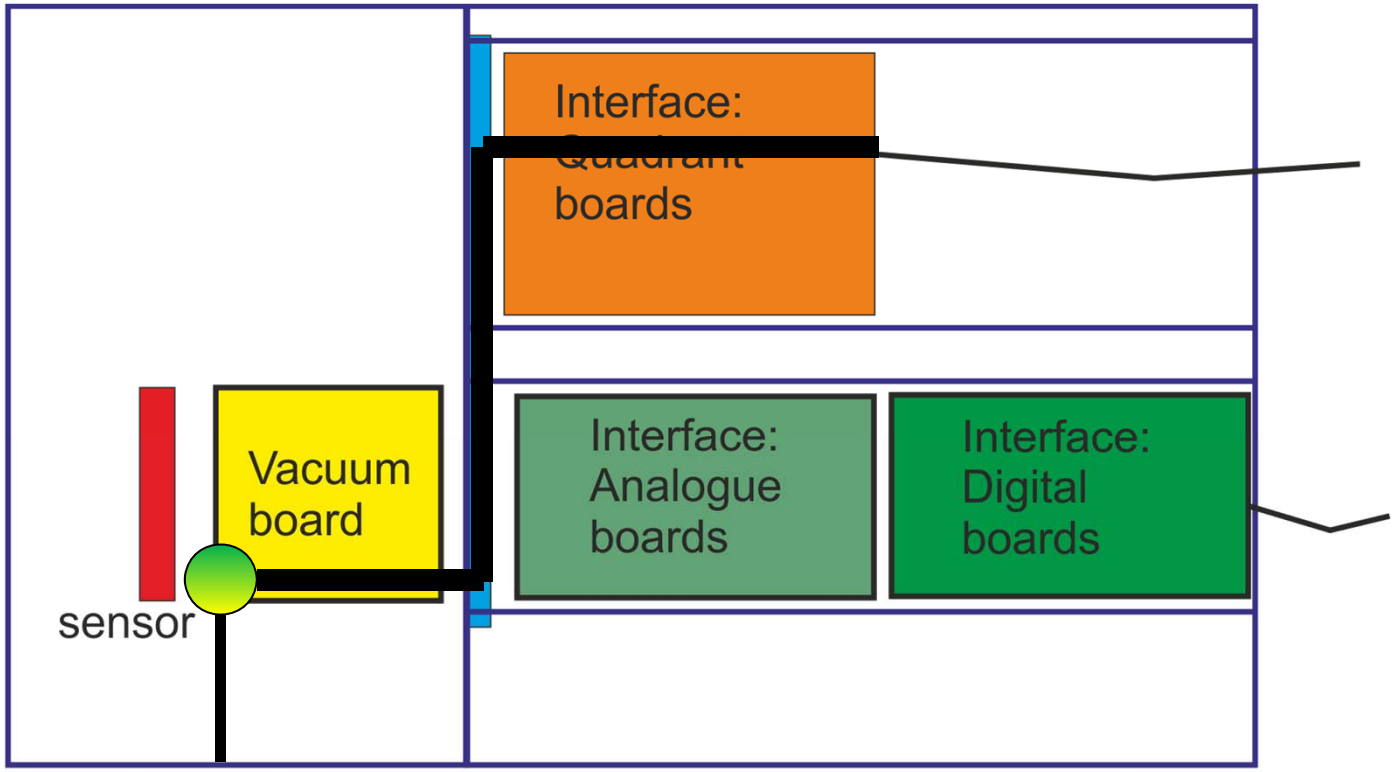
# Grounding/EMI: Task for circuit/layout/system




1. **Choose main grounding point:**
   At most sensitive part the detector plane

Task for designers of vacuum board

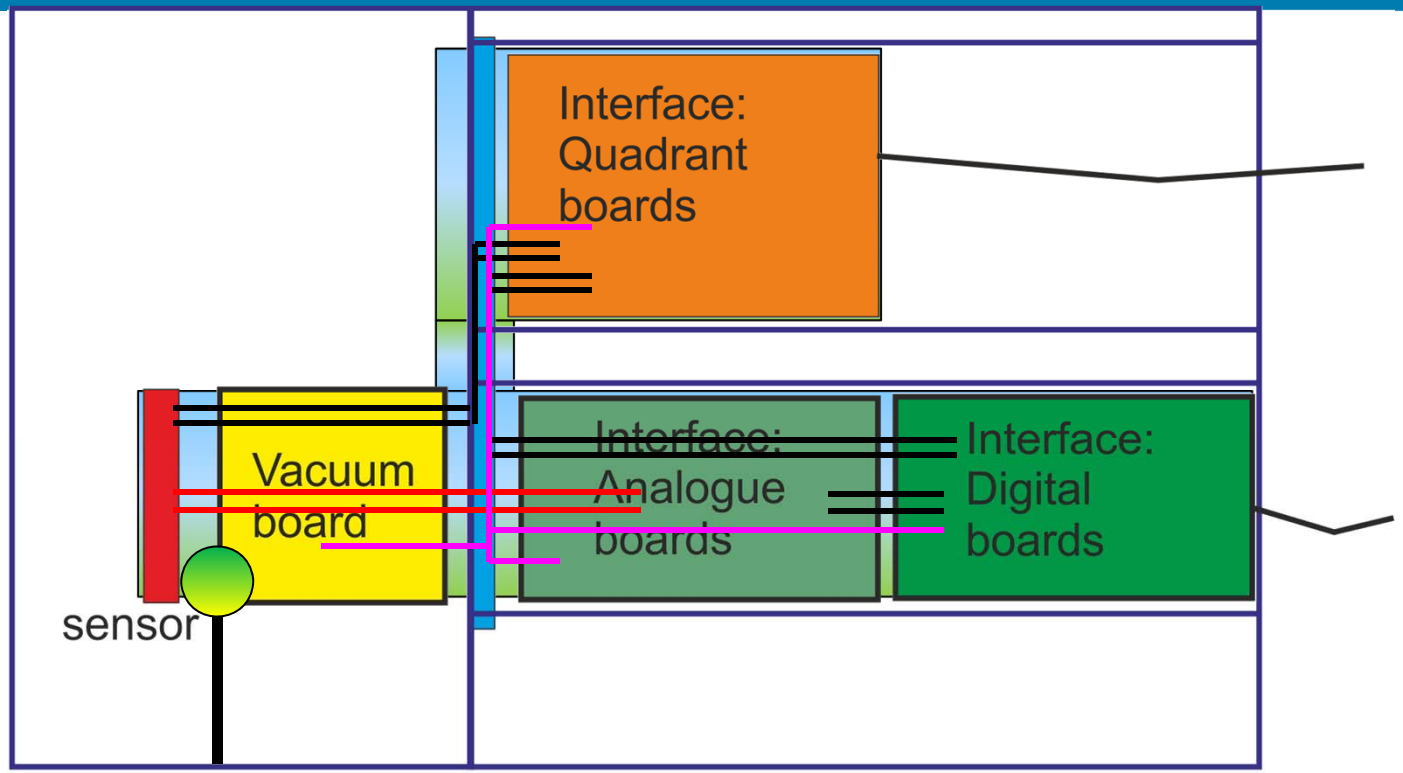
# Grounding/EMI: Step by step




Metal Chassis ( or just surrounding) with local GND-PE:
only partically closed

2. **High power for the ASIC's**
   Keep it out of the reference GND: allowing DC-drops of 0.1-0.2V.
   C-L-C filters at both ends.
   Low impedance routing between supply and return
   On Vacuum board: Power and ASIC output will mix their areas.
   Good filter for HV near ASIC

# Grounding/EMI: Step by step



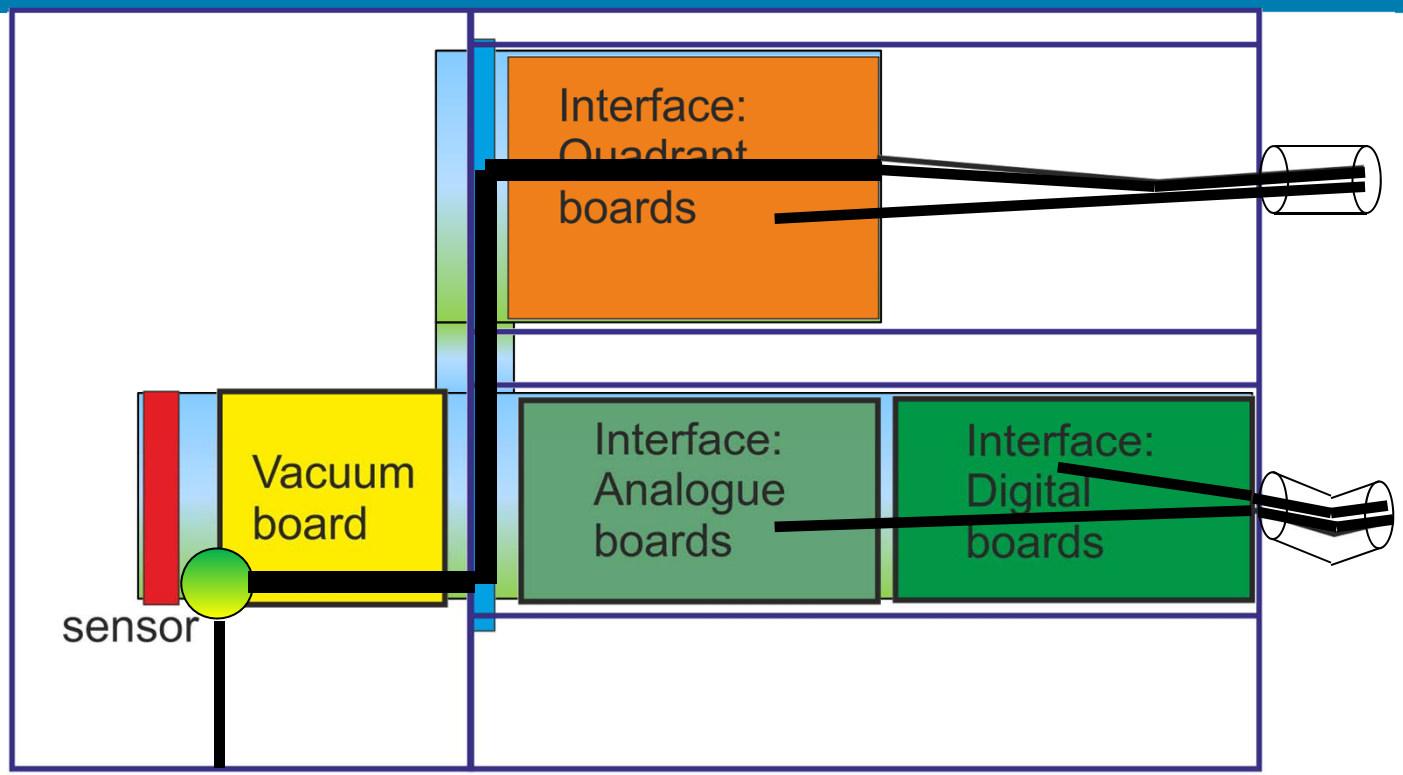

Metal Chassis ( or just surrounding) with local GND-PE:
only partically closed

**3. Fast signals only differential, slow ramp's with low current single ended**

- LVDS from Interface-Quadrant to vacuum board
- LVDS from Interface-Quadrant to Interface digital
- LVDS from Interface-digital to Interface-analogue
- JTAG from Interface-Quadrant to Interface-digital (only for boot)
- I2C from Interface-Quadrant to all
- All to be routed on top of continuous reference-GND plane

!!!! Fast differential analogue passing through power on Vacuum-board !!! Minimized loops also between each another

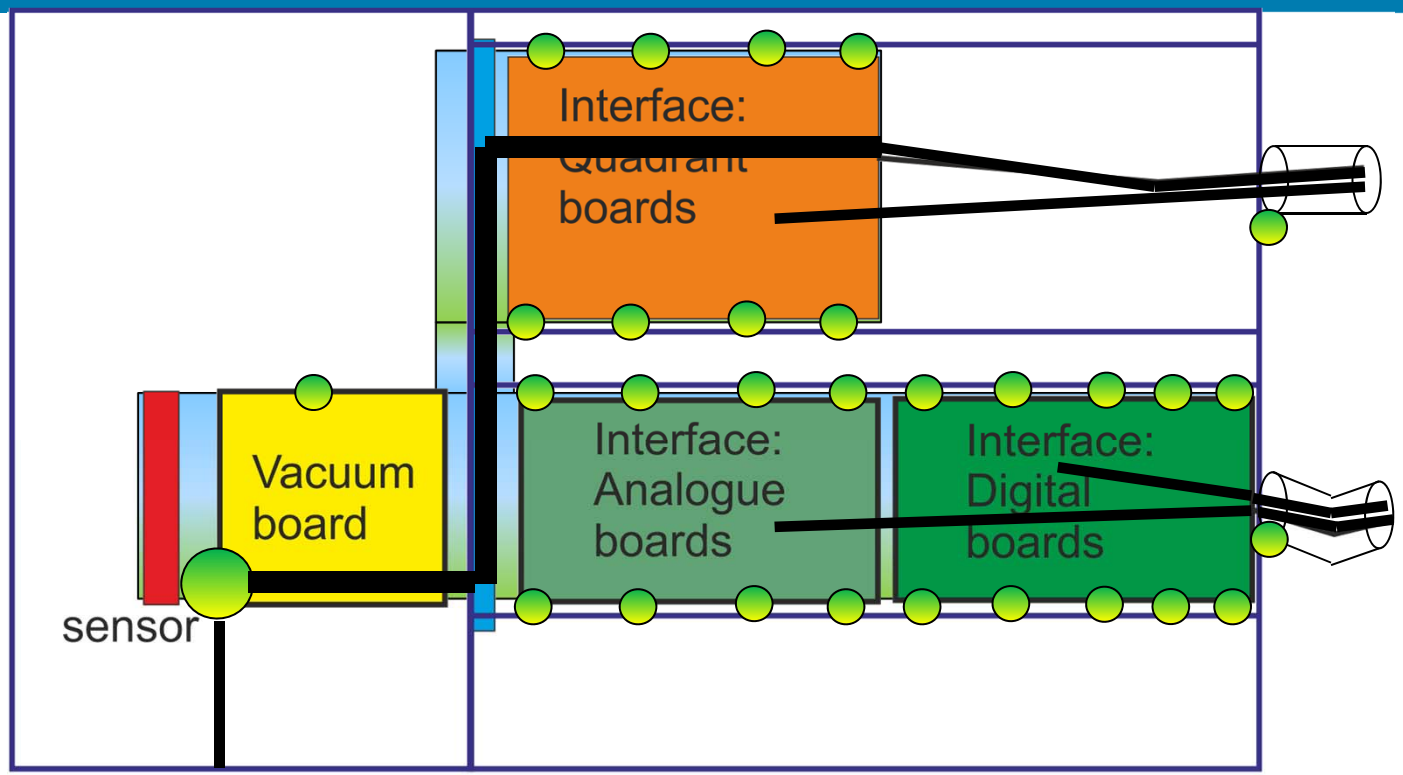
# Grounding/EMI: Step by step




Metal Chassis ( or just surrounding) with local GND-PE:
only partically closed

4. **Power for the high consumers Analogue and Digital and ASIC**
   - brought in from exteranal as floating voltages
   - Connected to reference close to consumers
   - C-L-C filters at input
   - Option to use shielded cables:
     closed EMI-Zone for higher frequences.
     but GND-loop for lower frequences.

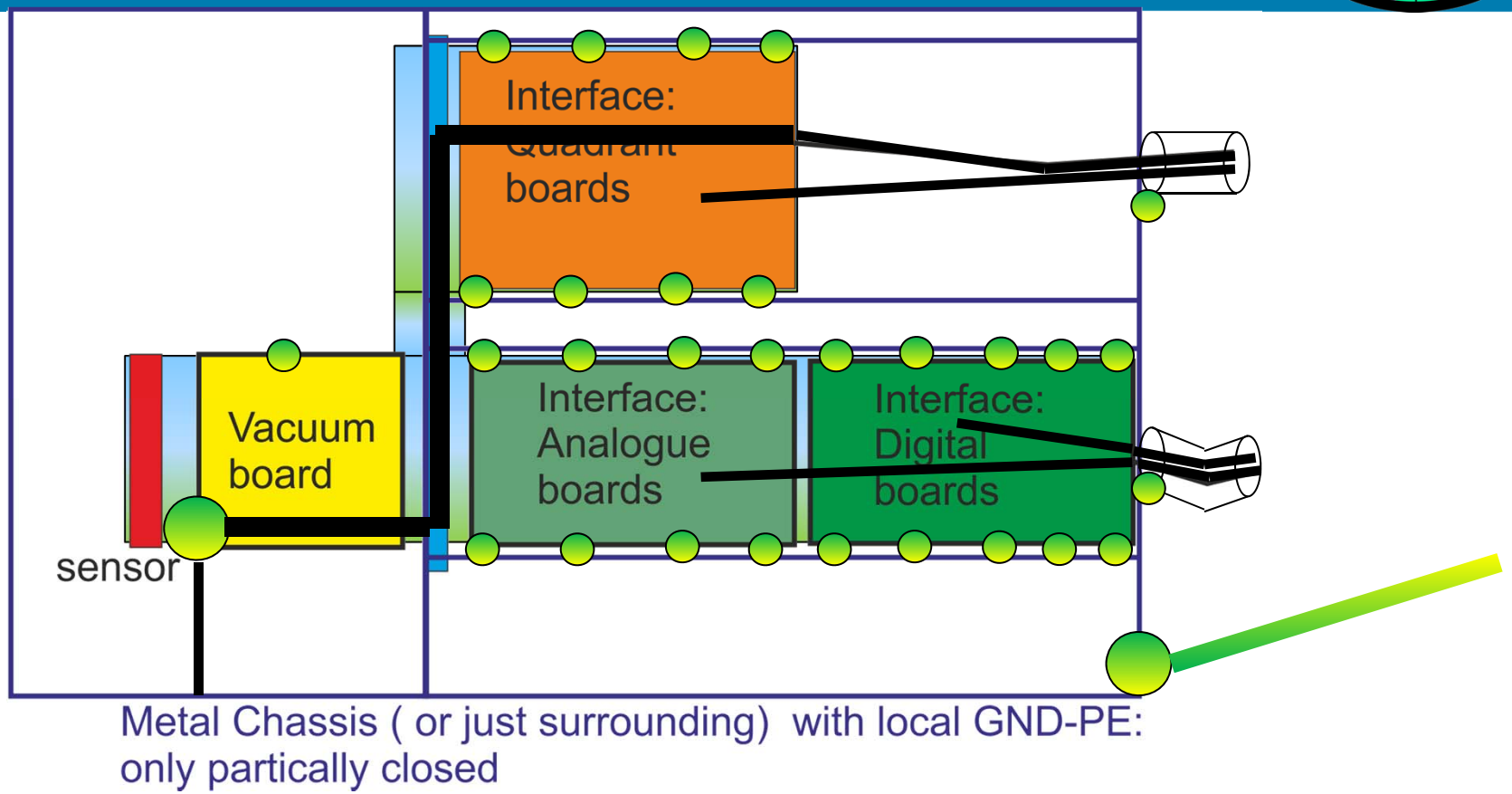
# Grounding/EMI: Step by step




Metal Chassis ( or just surrounding) with local GND-PE:
only partically closed

5. **Optional jumpers to connect PE and reference GND**
   - High frequencies anyway have C-couplings everywhere
   - LOW impedance connections are good to guide them back immediately
   - Low frequencies is a risk to pick them up on system level.
     No risk in a good system, where CHASSIS is free of external currents.
   - Jumpers every few centimeters to rail (rail should be conductive!)
   - Jumpers can also be bridged with capacitors.

# Grounding/EMI: Step by step




**6. GND connections to external**

General: Cable connections re planned for the back panel

Getting tehre and only there additional GND-PE-connections would be the general rule.

By that: Low frequency currents are kept out of the detector head.

# Power supplies

- Required are floating power supplies
- XFEL required detailed specifications, not only our consumptions.
- On my view: That is part of WP 2.5 given away to XFEL.
- I have written them and transferred

  Keeping modular and by that flexible to changes from us
  We don't have a final design tested: Changes of currents/voltages
  ASIC: - Accounting one positive voltage up to >1.66A per ASIC
  (Three option see next slide
  worst case option 10A supplies and keeping separated,
  one channel 6 ASIC's, close to yesterdays 1.63A)
  For that option another 16 channels, or are you sure to keep/reduce?
  Any voltage below +5V – losses: cable/board/regulator
  - A low current negative voltage could be generated at quadrant or adding another 16 power-channels.

- Also the budget was subtracted from AGIPD!
- Getting a generic system for XFEL?

  Purchase rules of XFEL!
- Format seems to be OK for XFEL, values also from our side?

# Power supplies

Power requirements

| What electronics group? | How often? | Polarity | Voltage [V] | Current [A] | Comment |
|---|---|---|---|---|---|
| Interface | 16 | plus | 12 - 14 | 3 | |
| Interface | 16 | plus | 3 - 5 | 10 | |
| Interface | 16 | minus | 1 - 5 | 10 | |
| ASIC's | 16 | plus | 2 - 5 | 30, may be 20 | One of these options |
| | 32 | plus | 2 - 5 | 16, may be 10 | |
| | 48 64 | plus | 2 - 5 | 10 8 | |
| Quadrant | 4 | plus | 12 - 14 | 2 | |
| Quadrant | 4 | minus | 3 - 6 | 2 | |
| Sensors | 4 (1 channel for 4 modules in a quadrant) | plus | 100 - 1000 | <5mA | Safety: <12mA |

**3 ASIC options**
- with 1 supply per module
- or 2
- - or 3 (4)

Written down with a view to the commercials within the low ripple systems.

Leaving freedom to get a standard system

That table I will fill with realistic estimates from schematics for the spread sheet. Here is with looking a bit to commercial available modules.

# Power supplies

Example of a WIENER/ISEG system


Variant with less different channels

| Number of channels | Power per channel | polarity | Required voltage range | Required current range |
|---|---|---|---|---|
| | [W] | | [V] | [A] |
| 84 100 | 50 | both | 0 - 6 | 0 - 10 |
| 20 | 50 | plus | 12 - 14 | 0 - 3 |
| None | 150 | plus | 0-5 | 0 - 30 |
| 4 | 12 | plus | 100 - 1000 | 0 - 5mA, <12mA |

Scalable for single module systems


**Requirement to XFEL:**

2 times 3kV supplies from 230V, single phase

…. Might depend on the final vendor choise

# Power supply

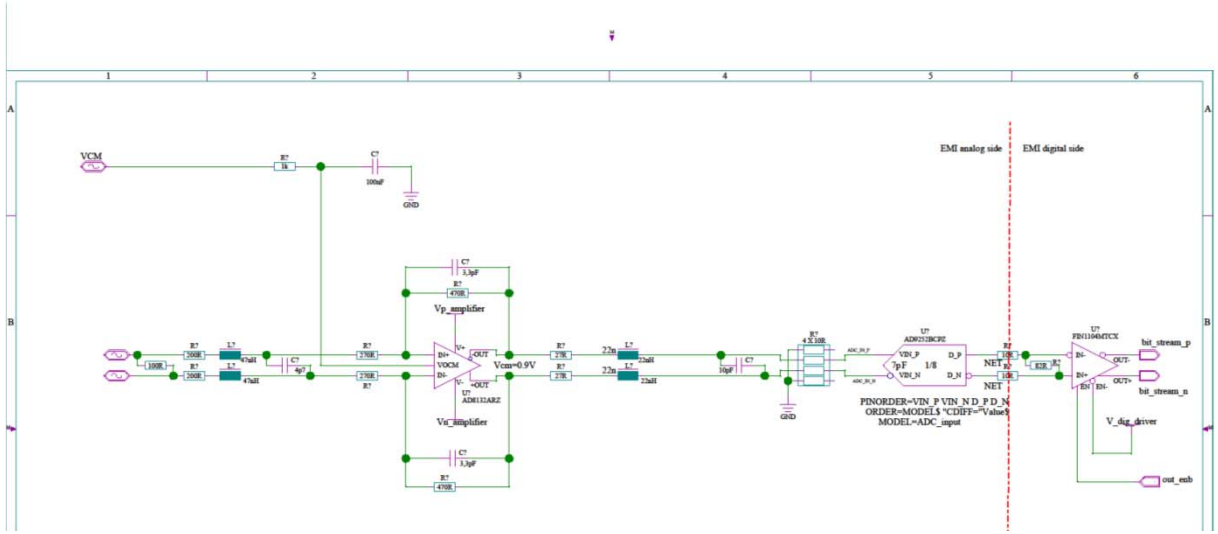
Other issues

- Inlet 230V ?
- Adjustable/monitoring of V and I (1%)
- Current as limit causing a trip
- Floating, voltage limit as nice to have
- Remote sensing as nice to have (10m)
- Low ripple (<30mV)
- Safety: Low voltage system < +-30V

  (total difference <60$V_{DC}$ for open operation)

  High voltage < 12mA/channel (only DESY regulation ?)
- Remote control
- 19'' Mechanics
- Air stream cooling
- Hardware interlock

# Analogue part




## ONE amplifier stage for

- Filtering picked up noise
- Converting to ADC requirements
- Differential termination with 100Ω
- Common mode pull with ~ 470Ω to 0.9V
- Assumption was input from ASIC +-1V

  … now: to be adjusted to +-0.5V

**Taken away**:

=> adjustable common mode voltage to which the ASIC-out is pulled

## EMI separation

from digital part,
R + true LVDS-buffer

## Train cycled operation

Charge storage and current control within powering circuit.

## Missing: slow control

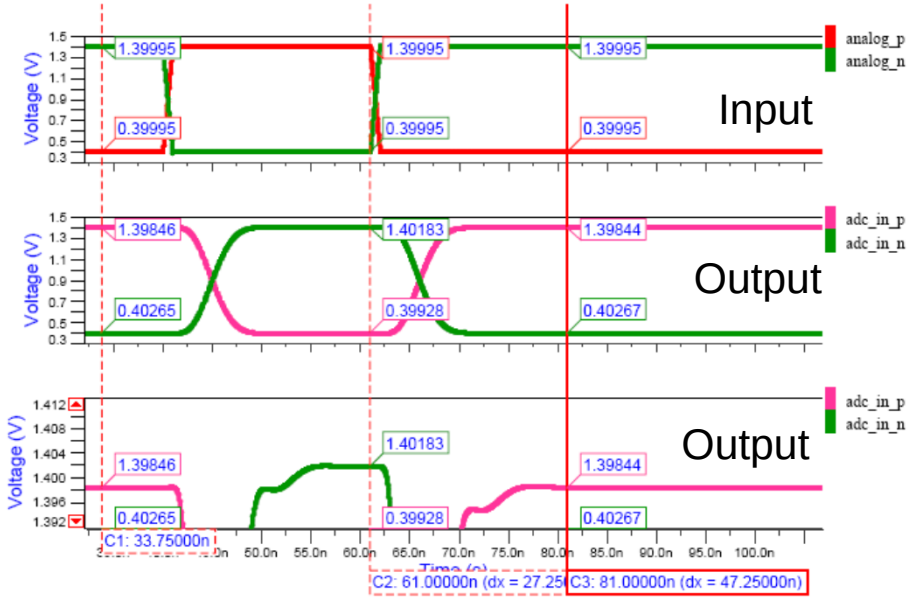
# Analogue Part

## Optimized for 50MS/s

What is the up-to-date rate?
- Containing the storage cell leakage?
- Feasibility of the driver?

Getting slower
- increases influence of leakage
- allows lower bandwidth for receiver

But that gets frozen into hardware.




Yesterdays talks: To be moved to 40MS/s

ADC sampling clock more complicated to adjust to the early agreements with XFEL/C&C:

99MHz = 22* bunch-clk continuous

multiply by 2 divide by 5 and phase-jump well before train.

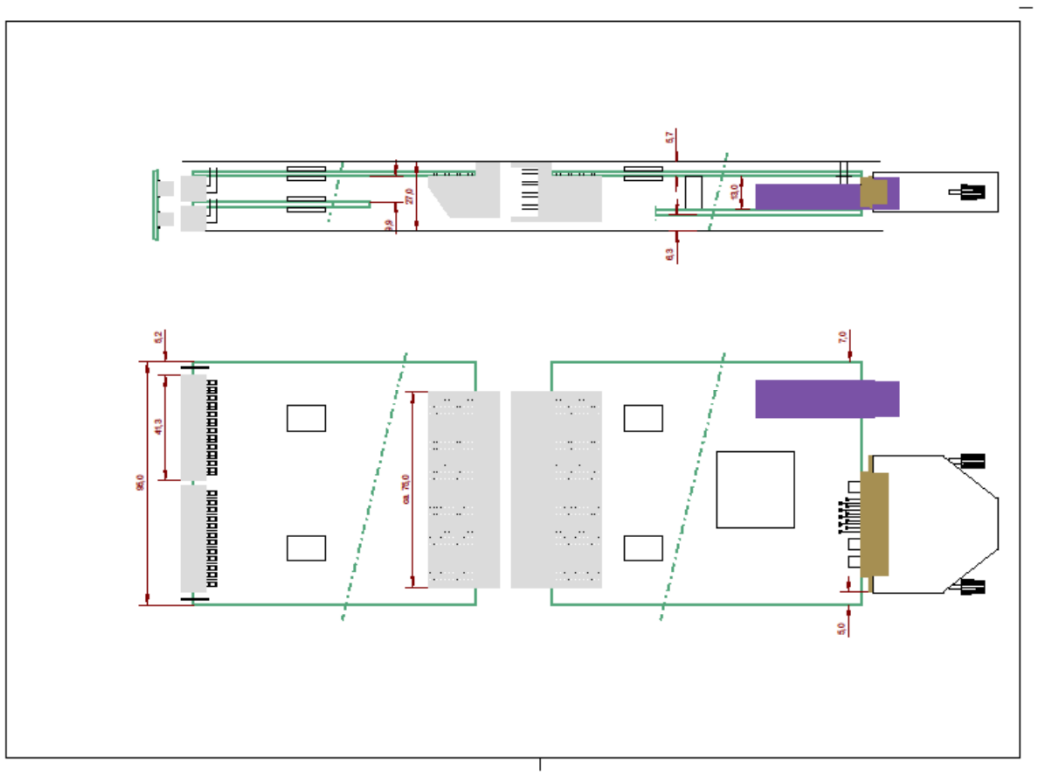
(easier is 33MHz, but 20% more storage time or allowance of storage time uncertainty of 12.5ns)

# Digital part

Different requests at DESY-side from X-ray groups for high speed/high input-count interface:

⇒ Common FPGA mezzanine

⇒ And user specific carrier



For prototype OK.

Later mezzanine needs small modification, so that everything fits behind sensor.

We need only ONE 10GbE.

To be done shortly after first experience.

# Digital part

Mezzanine board:

FPGA

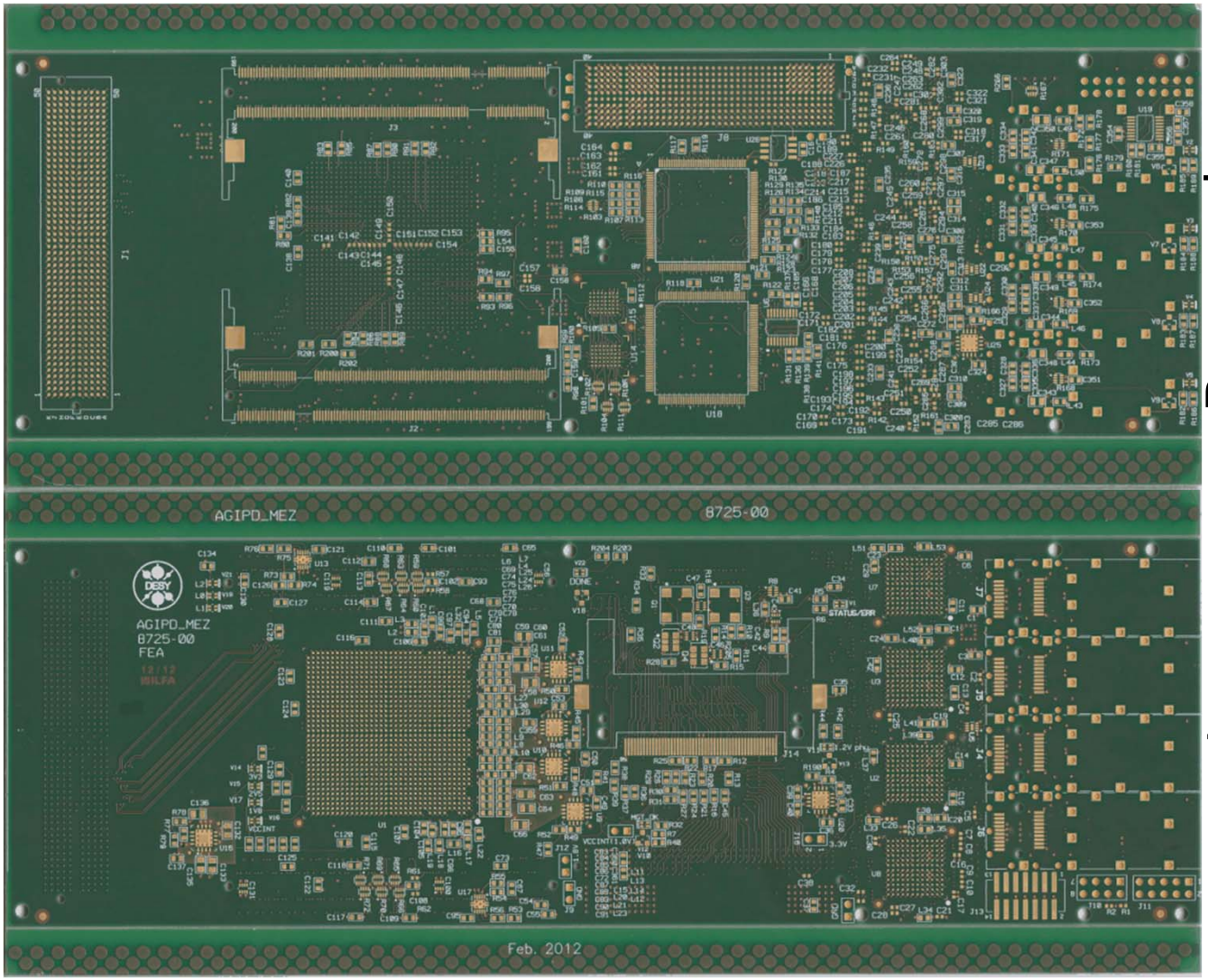
2x-DDR2-memory slots SoDIMM

10GbE 4x
Later reduced to ONE

JTAG reconfigurable Via Quadrant electronics.

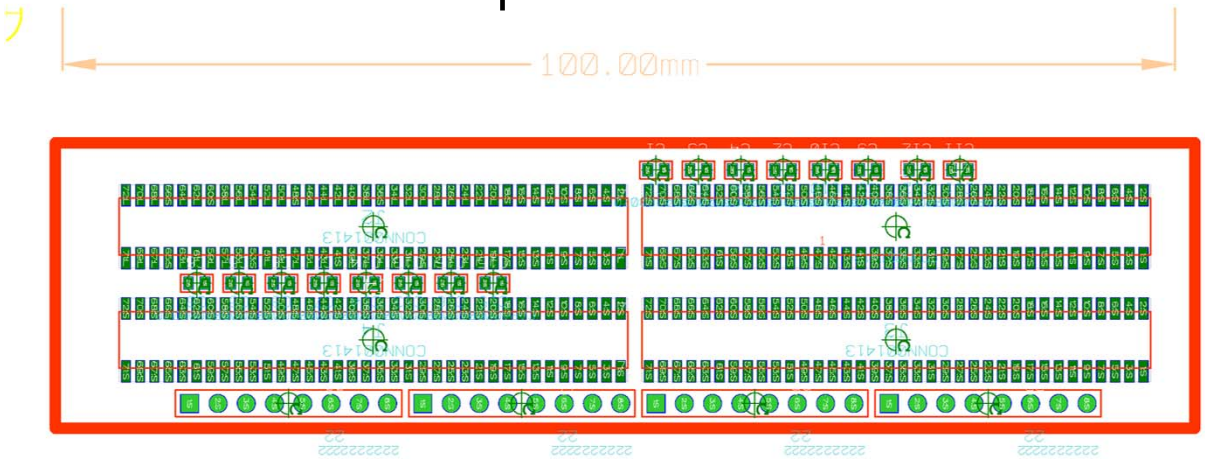
25cm x 8cm

In Production



# Backplane

- Companies see no problem to get a backplane vacuum tide
- Vias just to be filled and that is standard
- We will need internal vias to be filled and micro-vias to access on both sides the connectors. “dense space”




Space check: View from the interface side

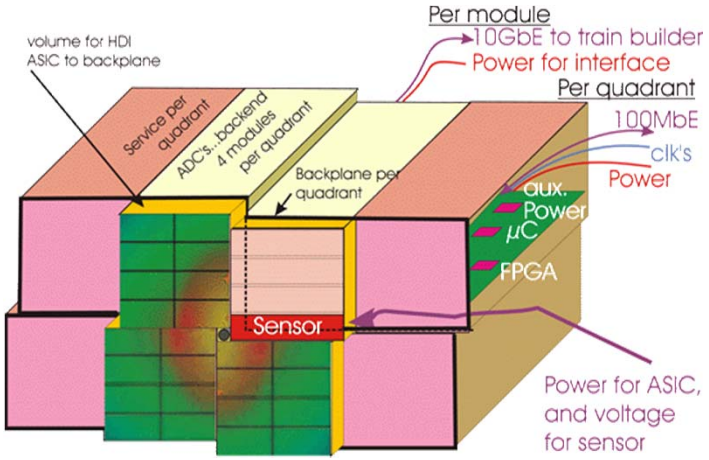
Real work to be started after agreements with vacuum board

# Backplane

## Signals transferred via backplane to the ASIC's

- 3 times LVDS-pairs:
  - clk: best the system-clk delivered by XFEL-C&C
    ( continuous 99MHz=22 * bunch clk)
    switch to digitizing clock for reading
  - data: 16 last bits before strobe are used
  - strobe: Bunch-clk or strobe to accept data
- 16 chip-selects
  - while running all are selected
  - while boot: I2C register on vacuum board controlled by quadrant µC.

# Quadrant



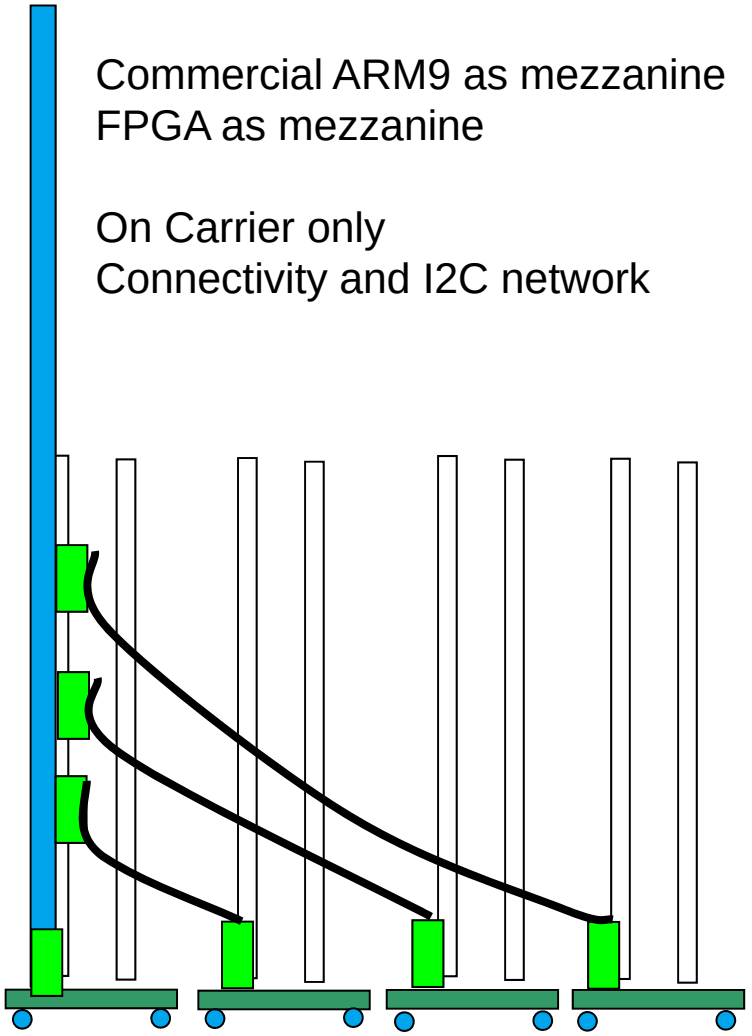

Most of it is reuse/evaluation for early stage

Carrier to be done in close contact with the backplane

To be decided:

- Power for ASIC via quadrant or via connectors directly at vacuum tank.
- Number of lines to ASIC to be verified
- Neg. supply for ASIC?

For long times operation can be done with evaluation etc.



Commercial ARM9 as mezzanine
FPGA as mezzanine

On Carrier only
Connectivity and I2C network

# Reject handling

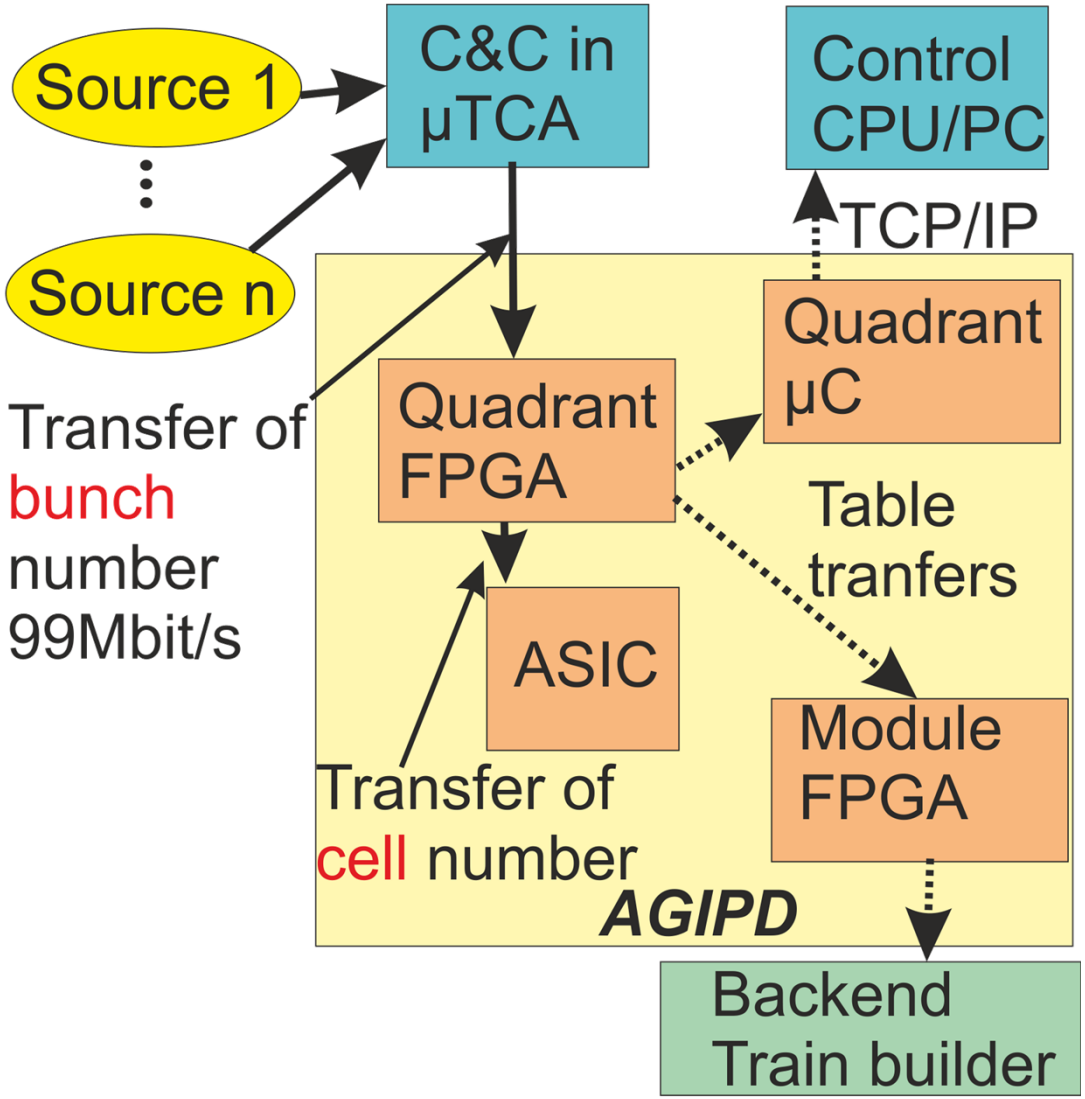
**AGIPD Internal:**

- Defined by need of ASIC

**External is generic for XFEL**

Specifications are requested by XFEL

- Reject as early as possible
- Random transfer allowed
- Random latency
- Transfer on the agreed cable
  system-clk (99MHz),
  bunch-clk(4.5MHz),
  data-in, data-out
  with single data rate
- ZERO or ONE rejected bunch-nr per bunch
- LVDS signal, floating coupled.
- After end-of-train more "rejects can be handled", but need of an end-record.
  ( "upgrade", not first priority)
- Same cable for other commands as train-start/train-end.

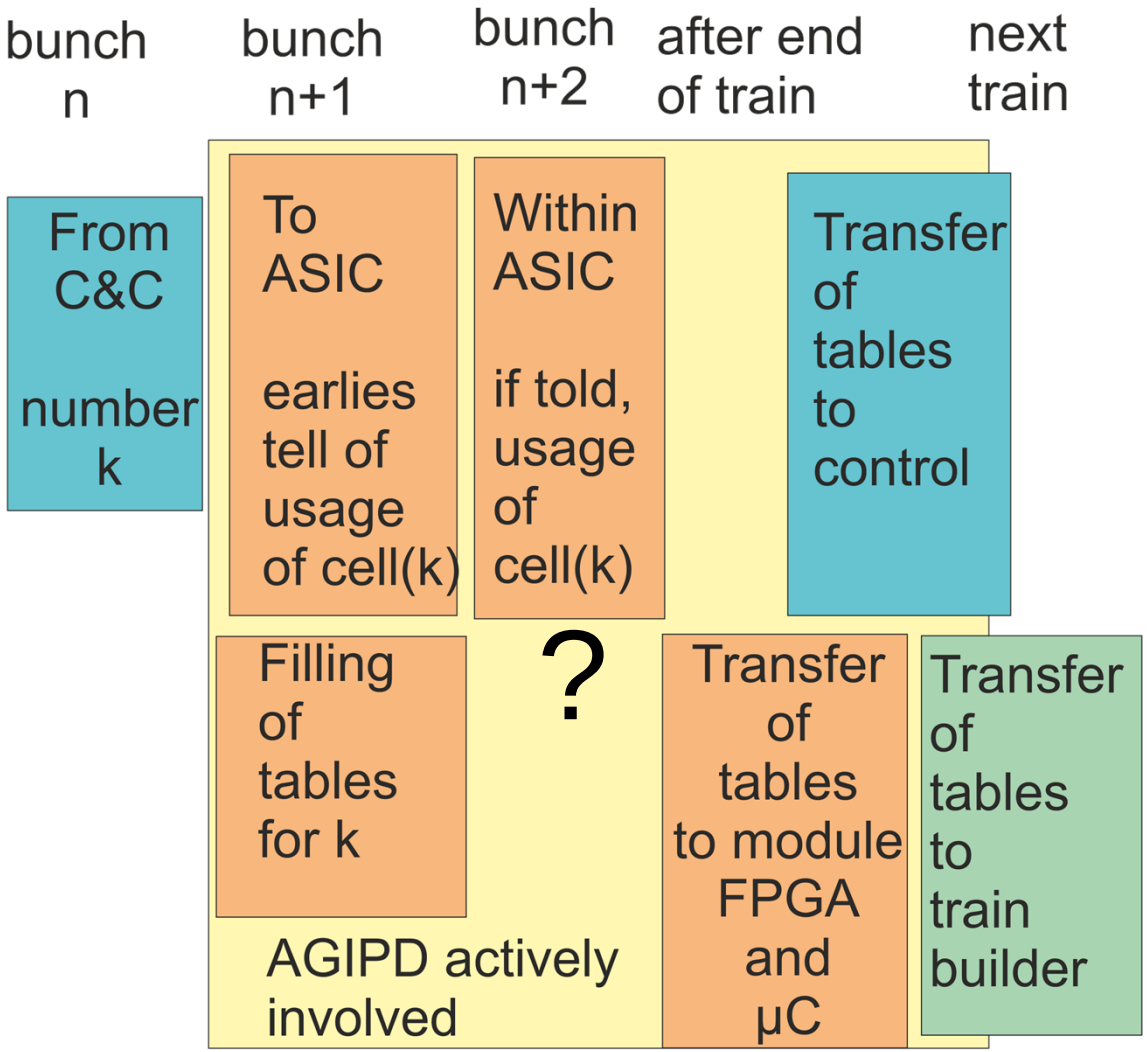


# Reject handling

At start of train, always a free cell is available,

**Latency**:
(only AGIPD internal)
Later it might need 1 or 2 bunches to get a cell free

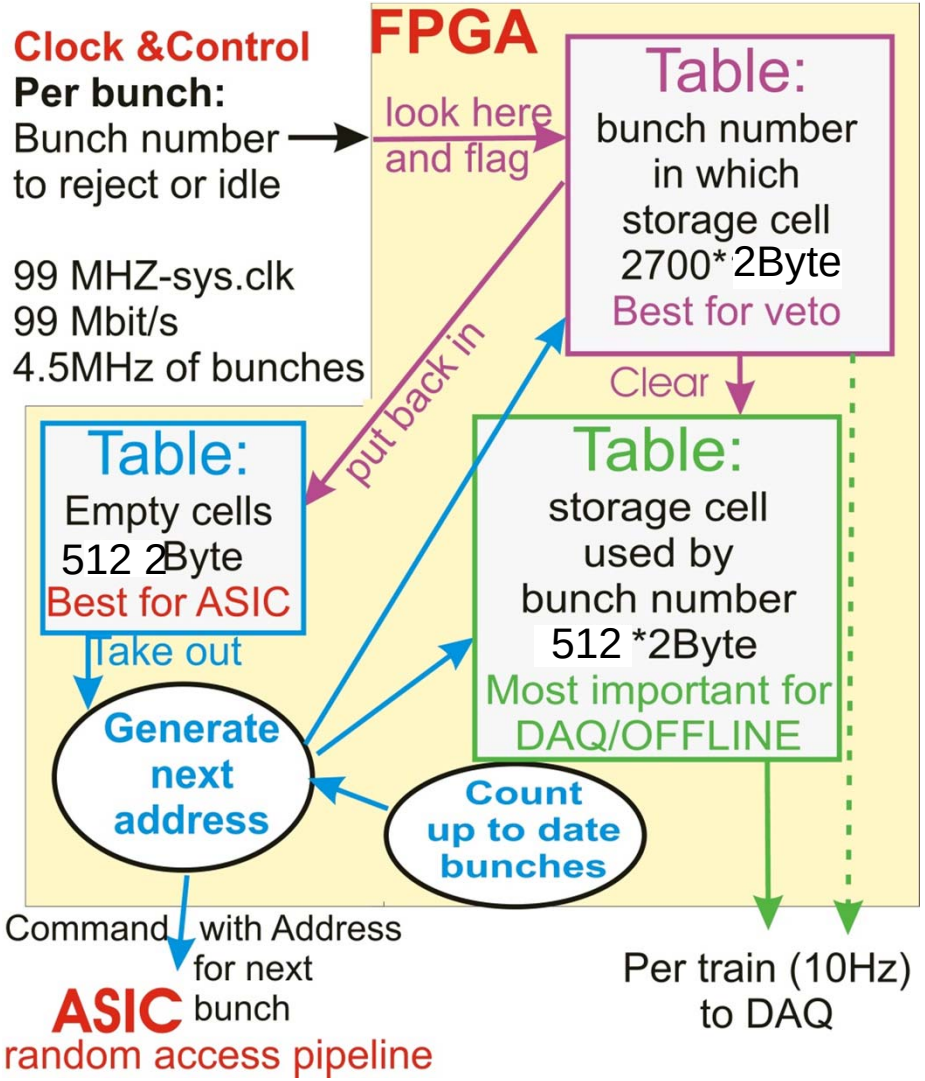
Actions are in parallel, so that it matters only at the end of the train



# Reject handling

- Received from C&C
- Configured to ASIC with a
  CLK: 99MHz or 198MHz or ?
  needs
  table free_cells
- Backend needs
  bunch_nr(cell)
- Internal reject needs
  cell(bunch_nr)
  Optional also to backend

Updated to be prepared for
More than 256 storage cells.



# Train builder activities

- Discussions for the definitions of records are started.
- In very first draft
  - Train framing
  - Picture data as everybody
- But there is more information: I think useful, may be needed later on:
  - Tables of cell usage
  - “Slow data” to get in somewhere: Temperatures, Voltages, Currents,
  - Storage times within cell might get interesting for calibration/corrections: Readout order or time per picture, Cell-nr might be the readout order.
    We still readout per picture?
    Storage time is a formula between bunch-nr=write time and readout-time(or cell-ID) = read-time. + offsets(pixel)

It’s a fraction of the total volume, but need other types of records.
I have formulated very early.
Are there statements, that we never need it?

# Summary and Outlook

- Ditigal part: Mezzanine in production
  Carrier few weeks for layout
- Analogue part: Few weeks for Mother board (all infrastructure + 32 channels)
  1 Month layout
  follow production
  Daughter board will just follow.
- Backplane: Agreements needed: mechanics, vacuum board.
- Quadrant: Evaluation board are expected to be sufficeint for operation
  Use Mezzanine FPGA and redign only additional carrier
  Confidence of settled parameters: Vneg for ASICs, backplane, vacuum board.
- Definitions against XFEL: Reject requests: To be formulated and Power…. Update from our side?