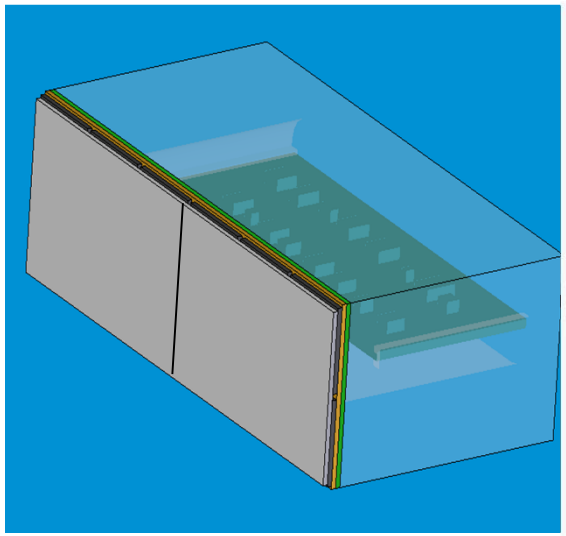
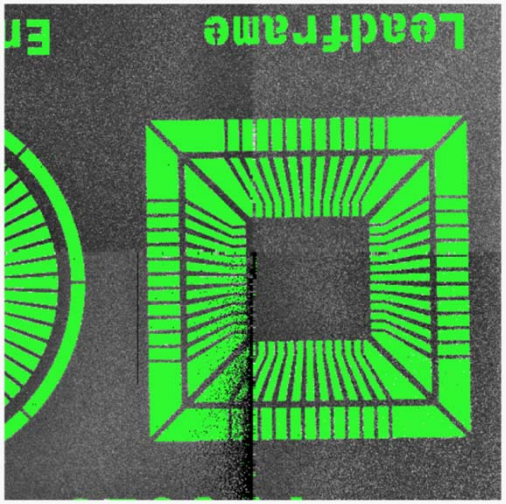
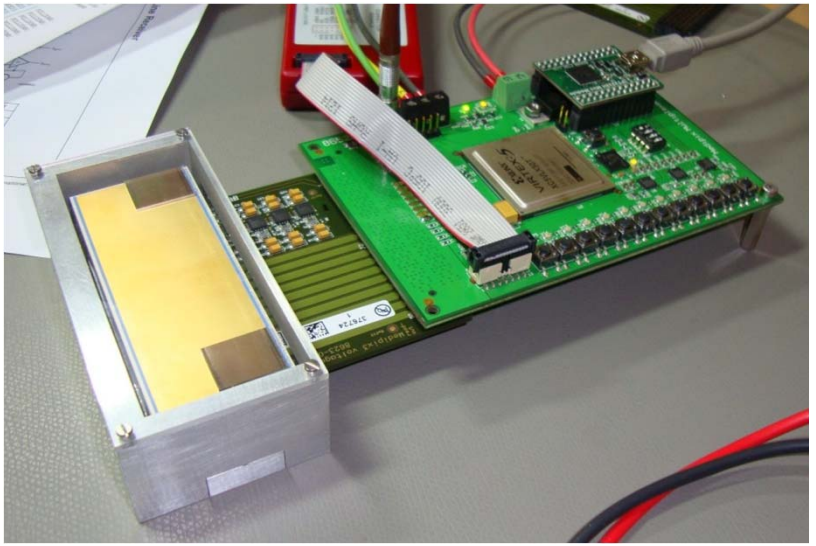
Medipix PCBs and mechanics







Sabine Lange, Sergej Smoljanin, David Pennicard, Matthias Bayer
Detector Group DESY

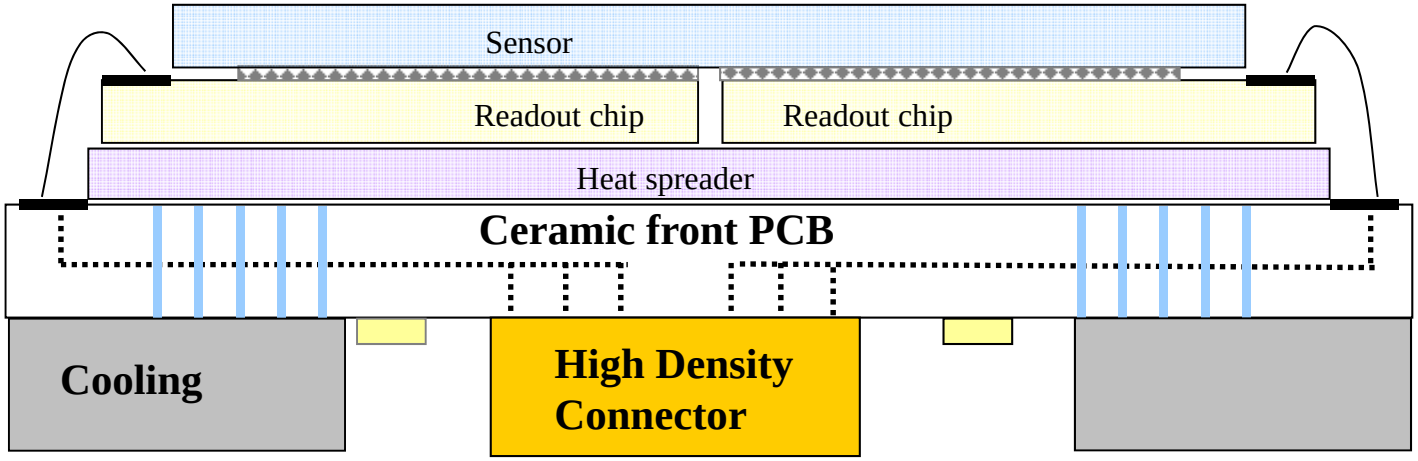
AGIPD Meeting 06.09.2011

HELMHOLTZ ASSOCIATION

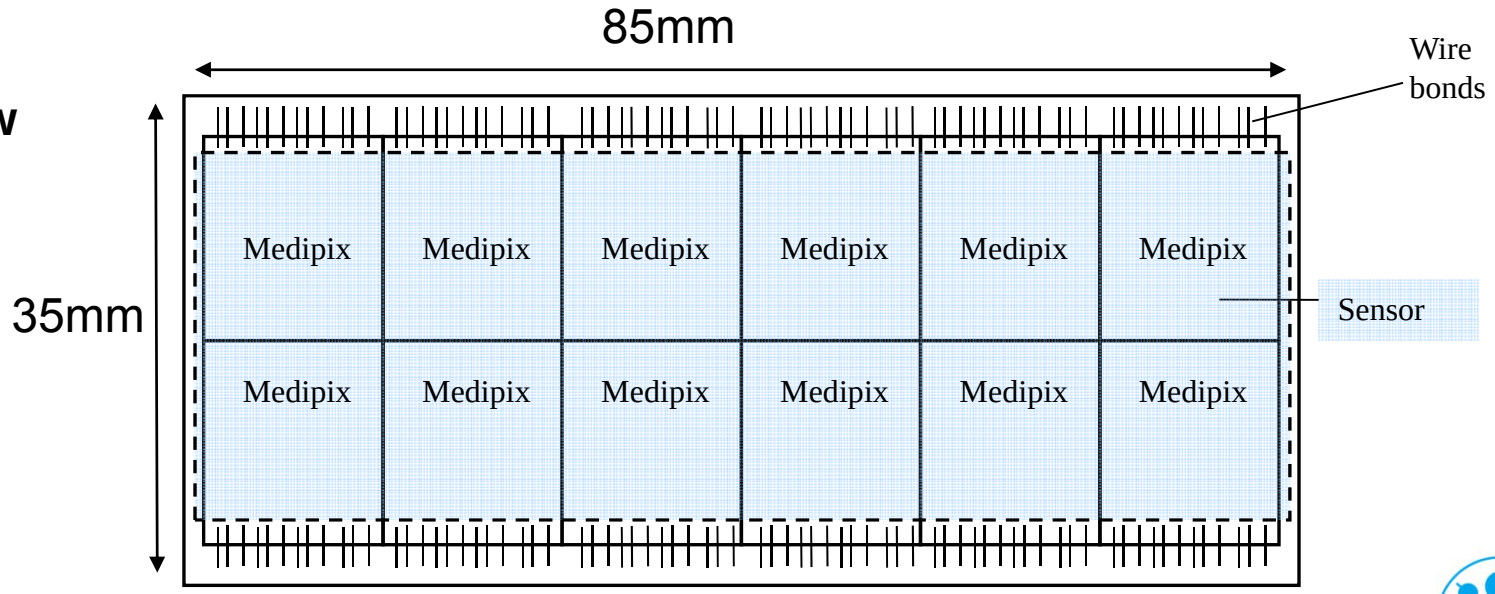
DESY

Detector assembly on ceramic PCB

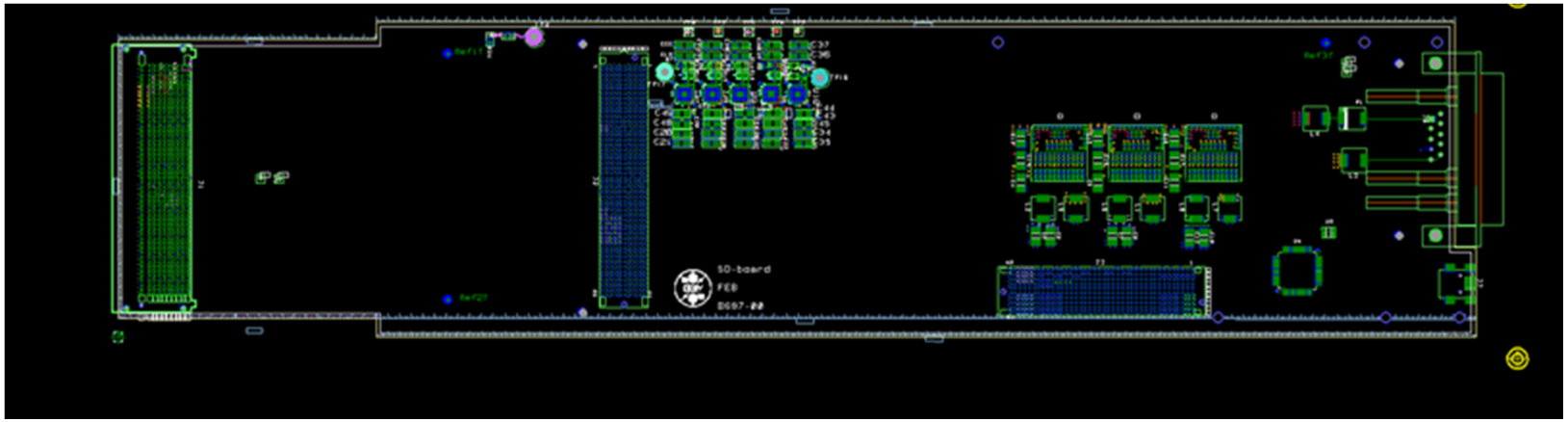
Side view

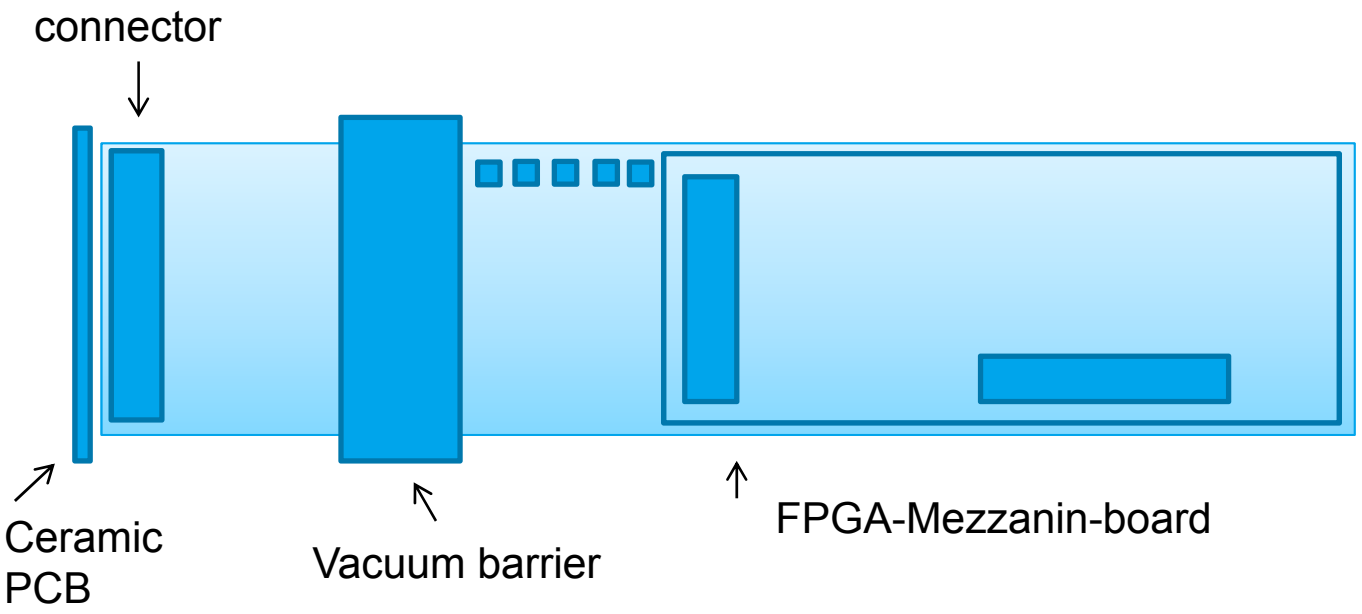


Top view

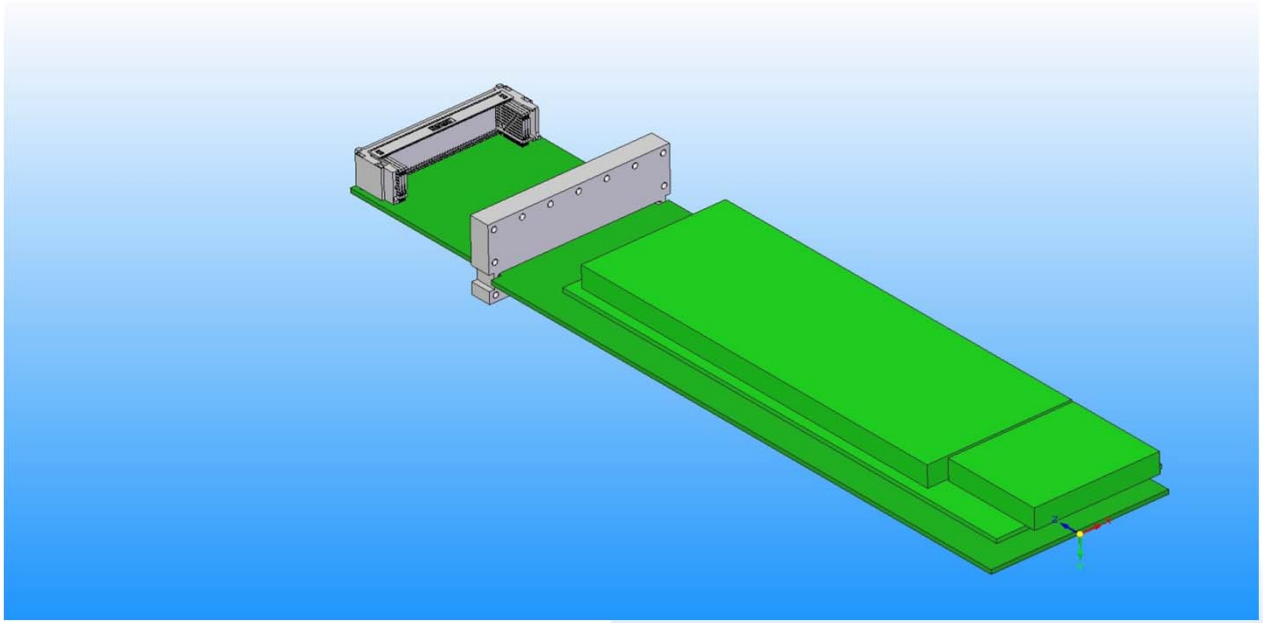


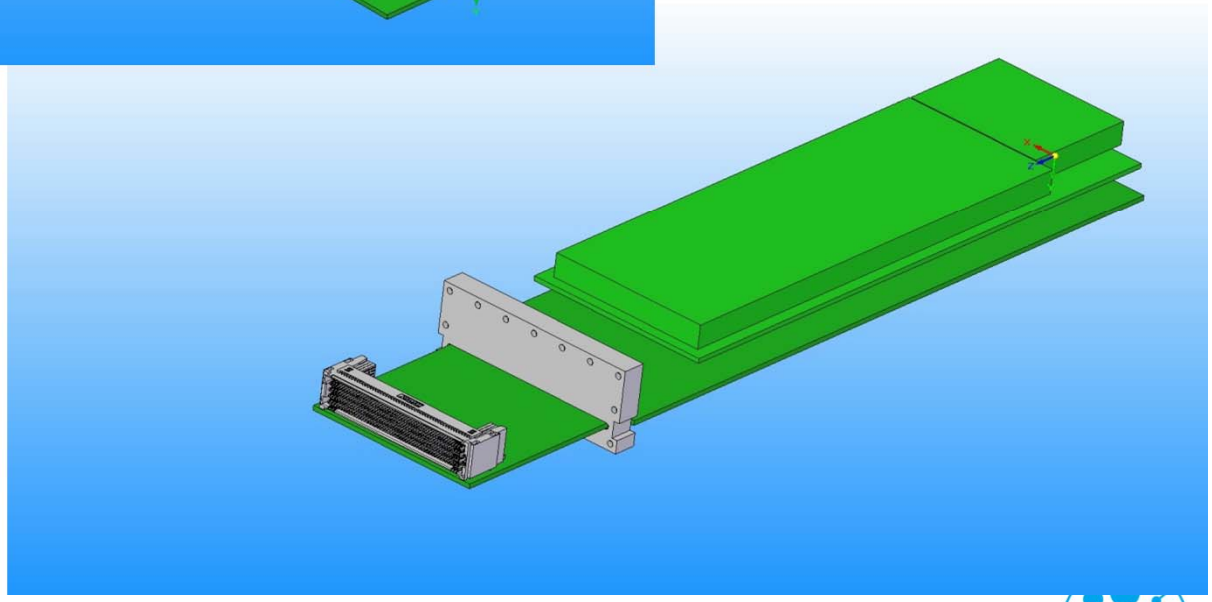
Carrier board FPGA-Board



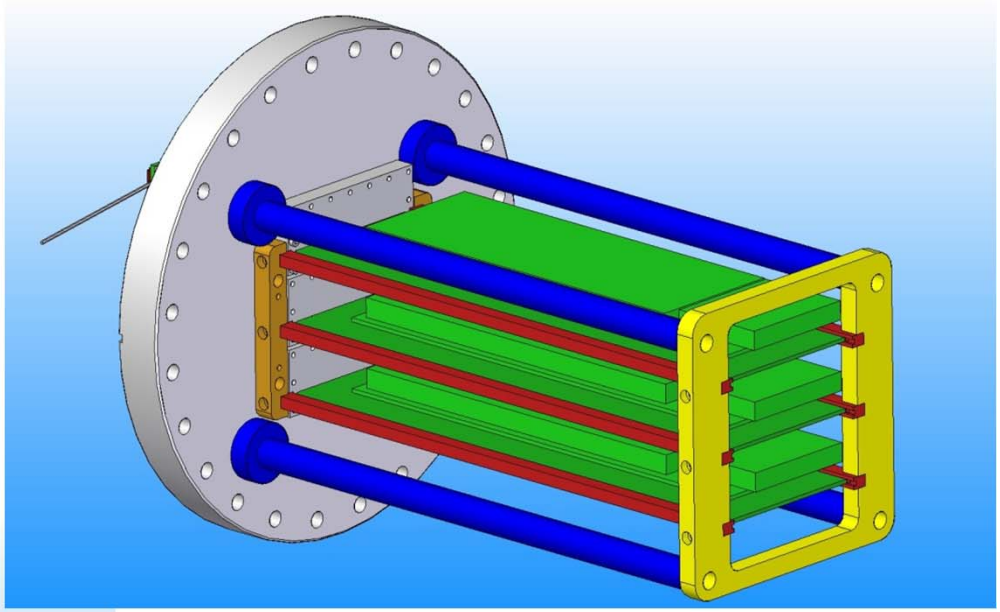


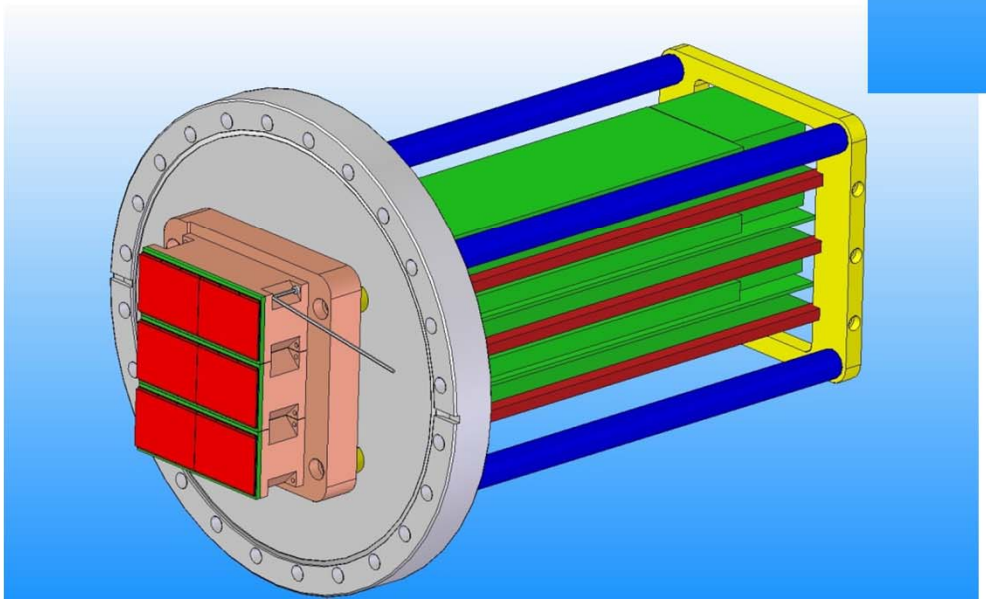
FPGA-board and carrier board





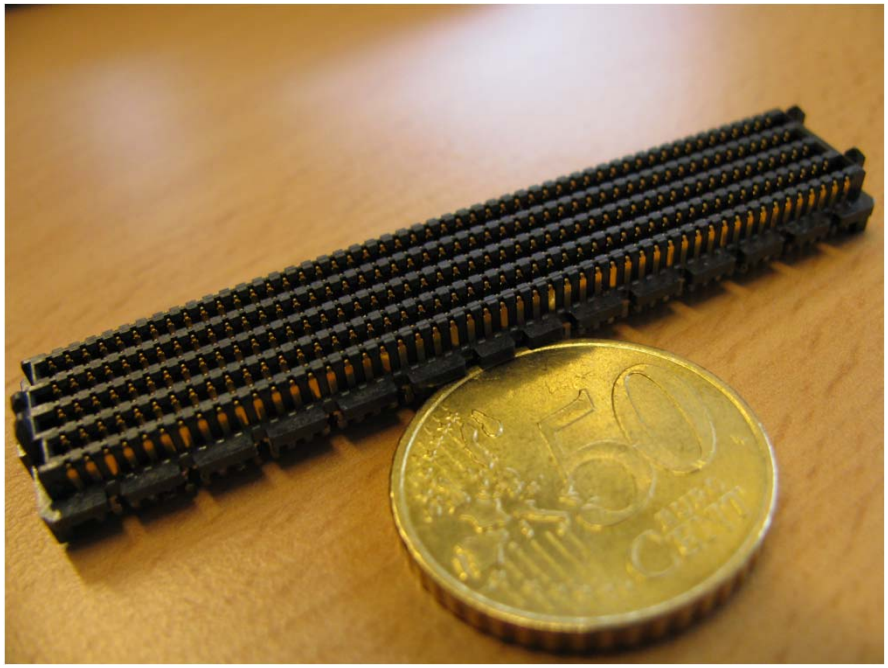
Mechanics



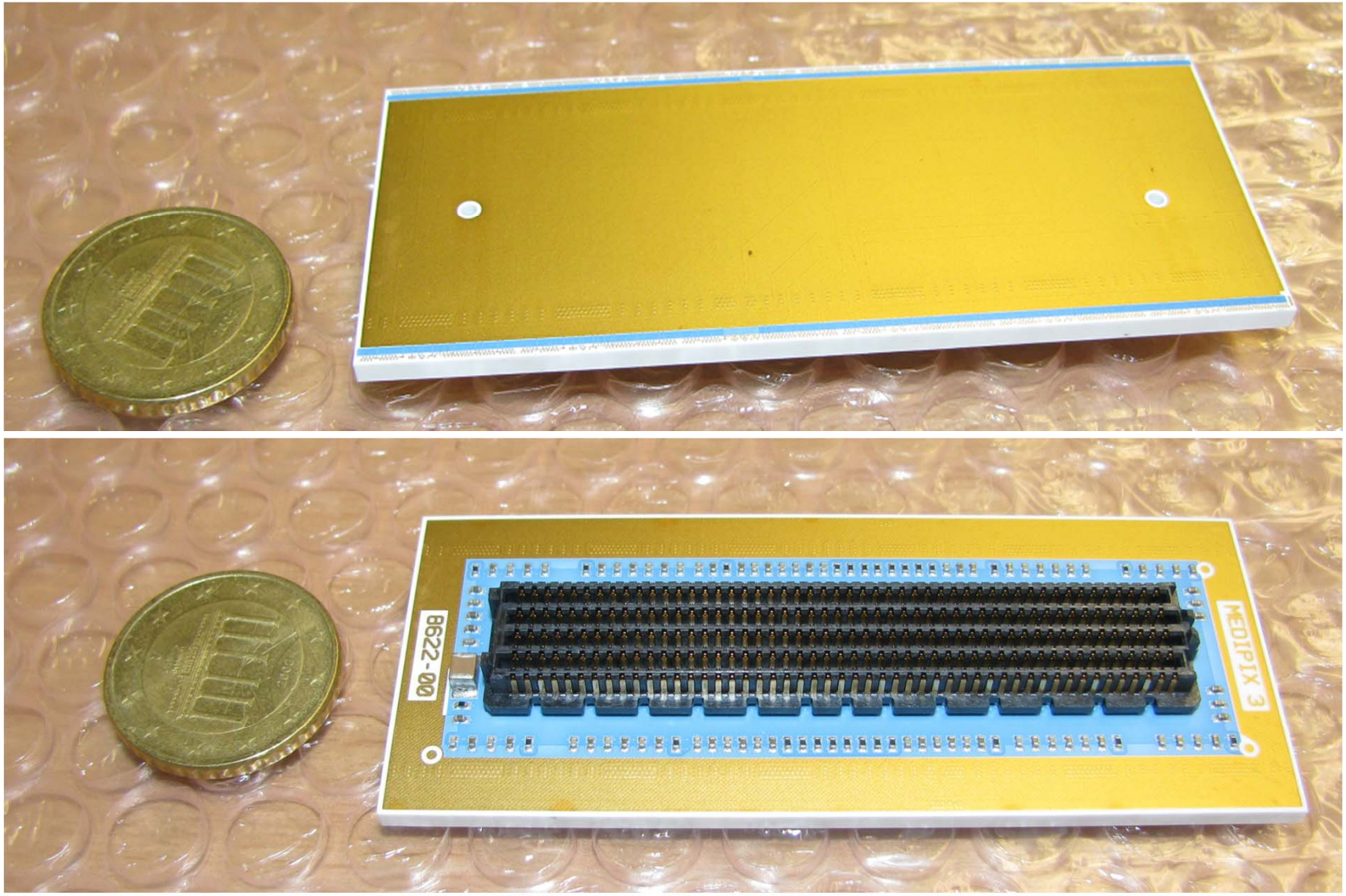


High-density connector for front PCB

- 500 pins including voltage supplies
- Samtec High Speed/High Density Open Pin Field Array, SEAM Series
  - Number of rows: 10
  - Number of pins per row: 50
  - pitch: 1,27 mm
  - Operating Temperature Range: -55°C to 125°C
  - Maximum Current per pin: 2A

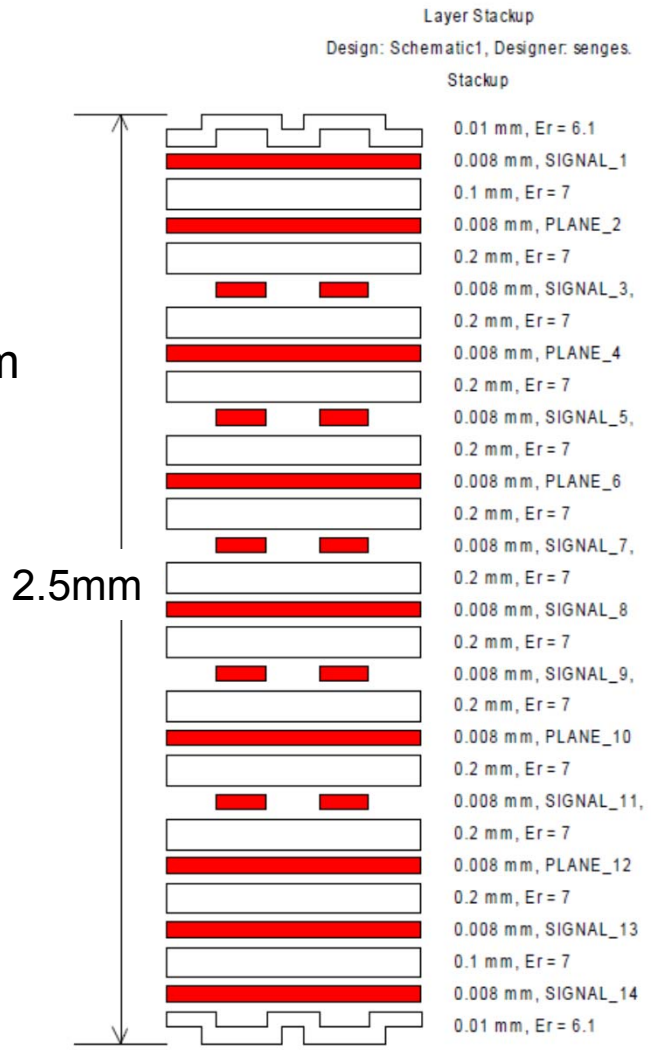


Completed module ceramic PCB



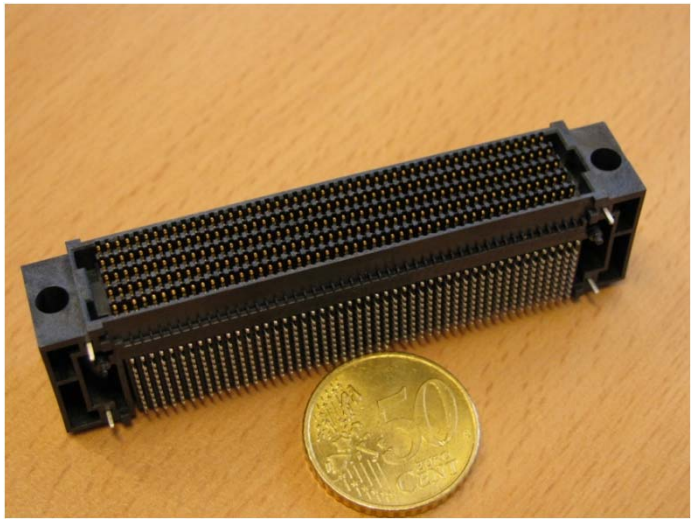
Multilayer PCB in LTCC Technology (KOA, Japan)

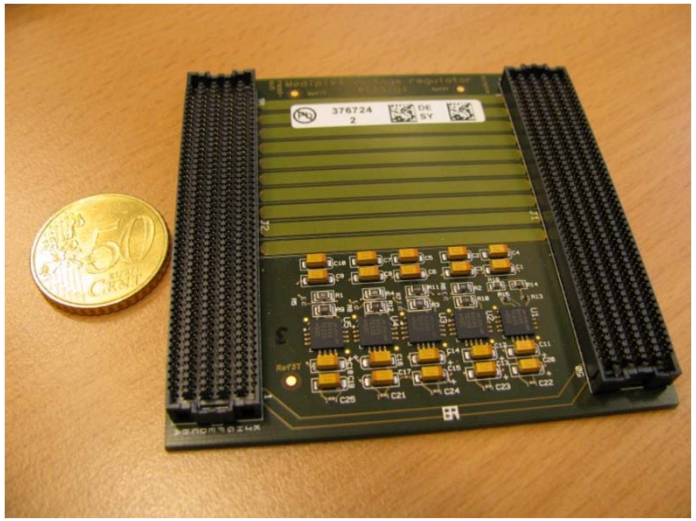
- 14 Layer
  - Maximum Number of Layers: 20
- Thickness of Signal Layer 200µm
  - Standard thickness: 80µm, 100µm, 125µm
- Trace Width 70 µm, 170µm Diff Pair Spacing (100Ω impedance)
  - Minimum Trace Width: 60 µm
  - Minimum Trace to Trace spacing: 60µm
- Via diameter 100µm
  - Available via diameter: 100µm, 150µm, 200µm



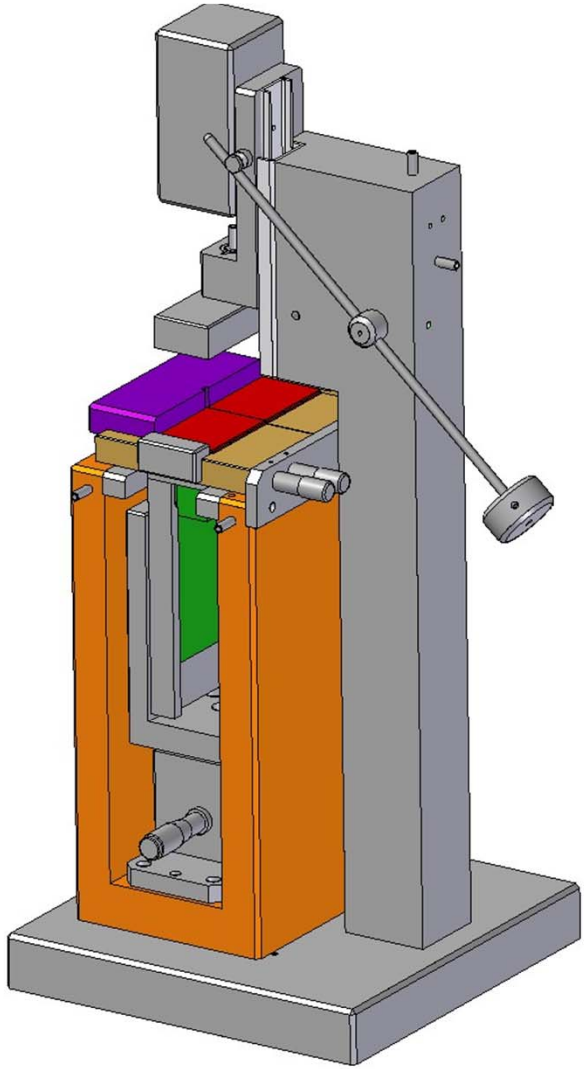
Voltage regulator PCB

- Transfer of the data
  - 150 LVDS through the board
- Power supply
  - 5 low-dropout linear regulators
  - each regulator 4A
- Hi-Density right angle connector, SEAF-Series

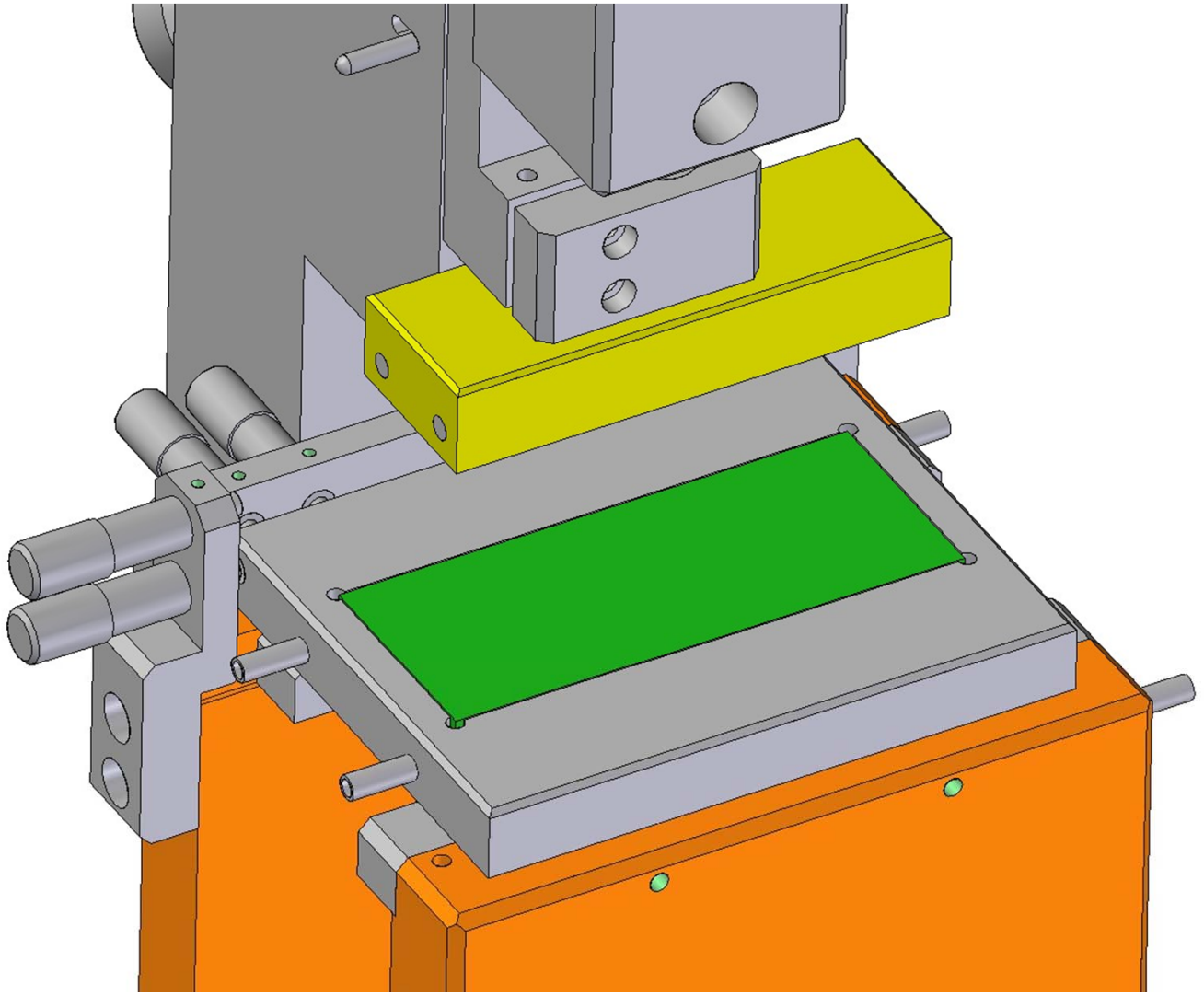




Gluing station



Gluing station



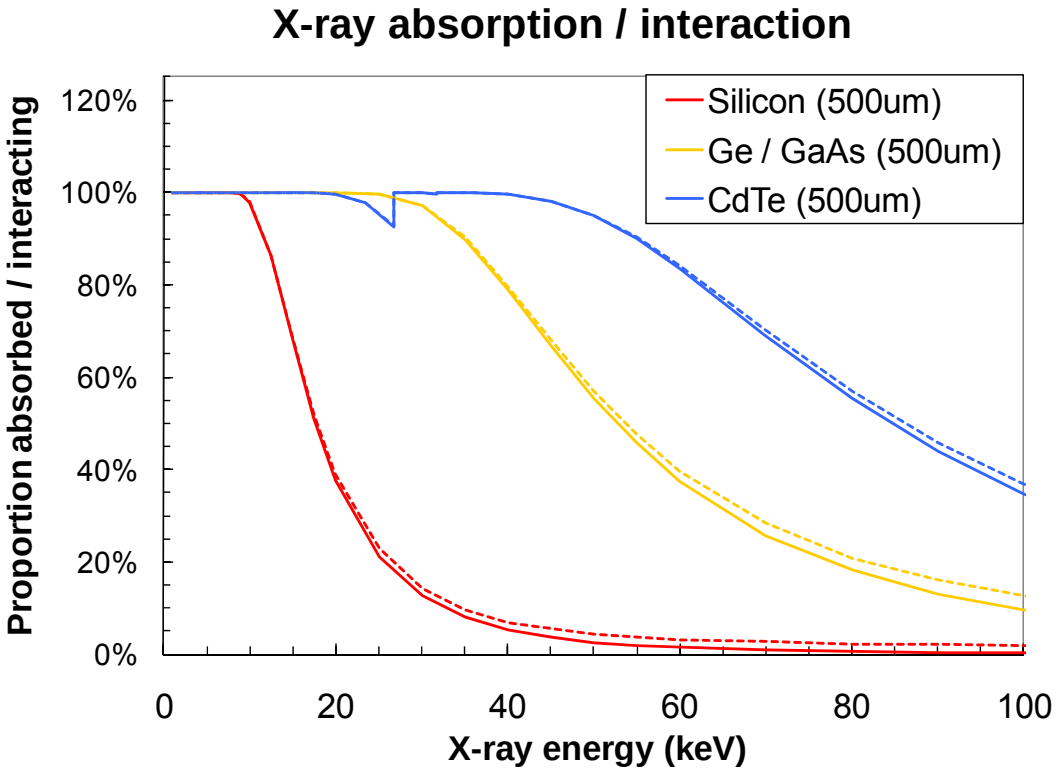
Large-area Medipix3 project

Thanks for listening

High-Z materials

> Many Petra-III (DESY synchrotron) experiments up to 100 keV x-ray

- Replace silicon with another semiconductor



> Germanium:

- Germanium (Canberra),

  Still tests: How sensitive are diodes to high temperatures

- Indium bump bonding (IZM)

  Relatively cold bonding (<100°C)

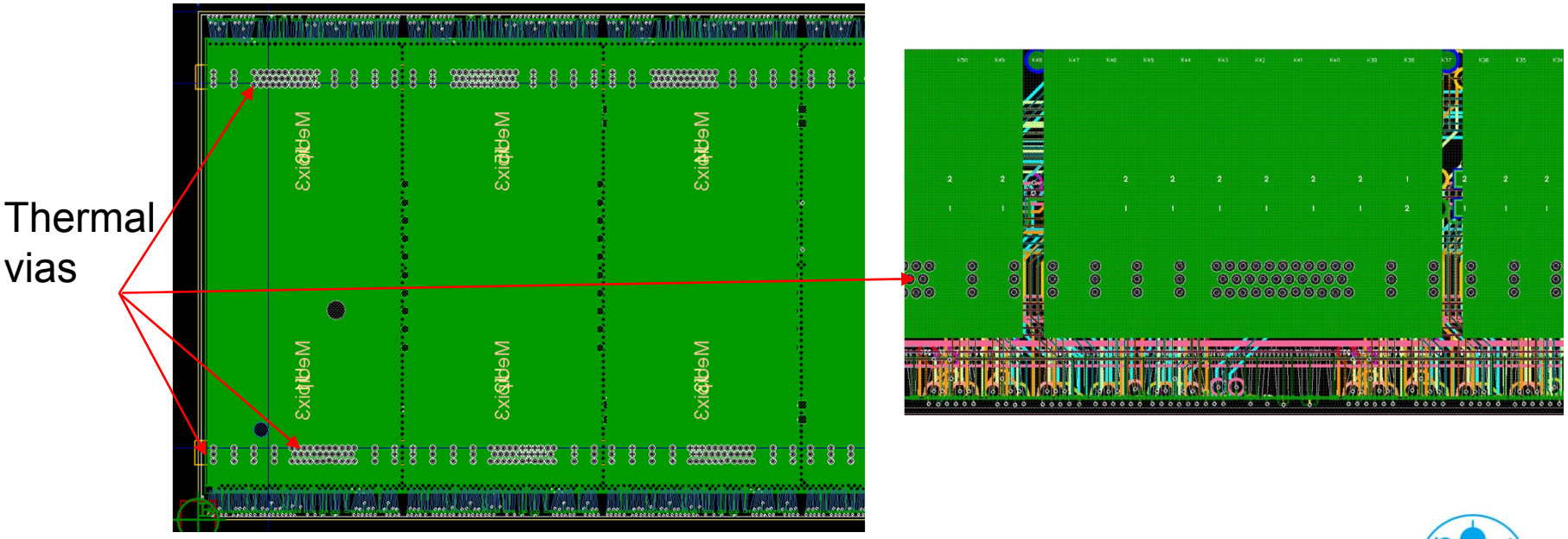
Mechanics and cooling

Design issues

> Cooling frame occupies space on the back underneath each PCB

> available space for connectors reduced

> Thermal vias make routing more difficult



Ceramic PCB