Backend electronics and software

AGIPD collaboration meeting

C.Youngman for WP76

Hasylab 25b/109, 5-Oct-2010

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Contents

- For those who have forgotten what WP76 is
- Backend systems overview
- Electronics status
  - Train Builder (readout)
  - Clock and Control (sequencer)
- Some related items (single crate DAQ, VETO)
- Software status
  - Testing with XCAM
  - AGIPD FEE micro-processor and slow control status
- DM, test hardware... related news
- Conclusions

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What is WP76 doing = Project definition

- The WP76 website is a useful source of information
  - http://www.xfel.eu/project/organization/work_packages/wp_76/

- What is WP76 doing is described in the cTDR (Oct.2010)
  - http://www.xfel.eu/project/organization/work_packages/wp_76/infos/
  - In a nutshell:
    - ➔ DAQ: providing hardware and software for Photon Beam Systems:
      - beam lines (motor drives, etc.)
      - detectors (2D pixel detectors, small data volume detectors, etc.)
      - hutches
    - ➔ DM: providing software and hardware for data:
      - storage
      - access
      - analysis

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… and who are they = Manpower update

- In house
  - Nicola Coppola – started 1-Mar-2010
    - Detector DAQ software and beam line software and interfaces
  - Burkhard Heissen – 1-Jun-2010
    - Data management software framework design, configuration, workflows...
  - Sergey Esenov
    - DAQ software development
  - Irina Kozlova – started 1-Aug-2010
    - Data management software development.
  - Bartosz Poljancewicz
    - IT administrator…
  - Dana Wilson
    - Hardware (shapers, micros…), front end (OS, FPGA…) software
  - Krzysztof Wrona
    - Data management organization and development, IT group leader
  - Christopher Youngman
    - DAQ organization and development
  - Coming in 2011
    - 2 DAQ and 1 DM FTE
- External:
  - STFC and UCL FTEs for TB and CC system development (contracts)
  - FEA and FEB developments (pay costs incurred)

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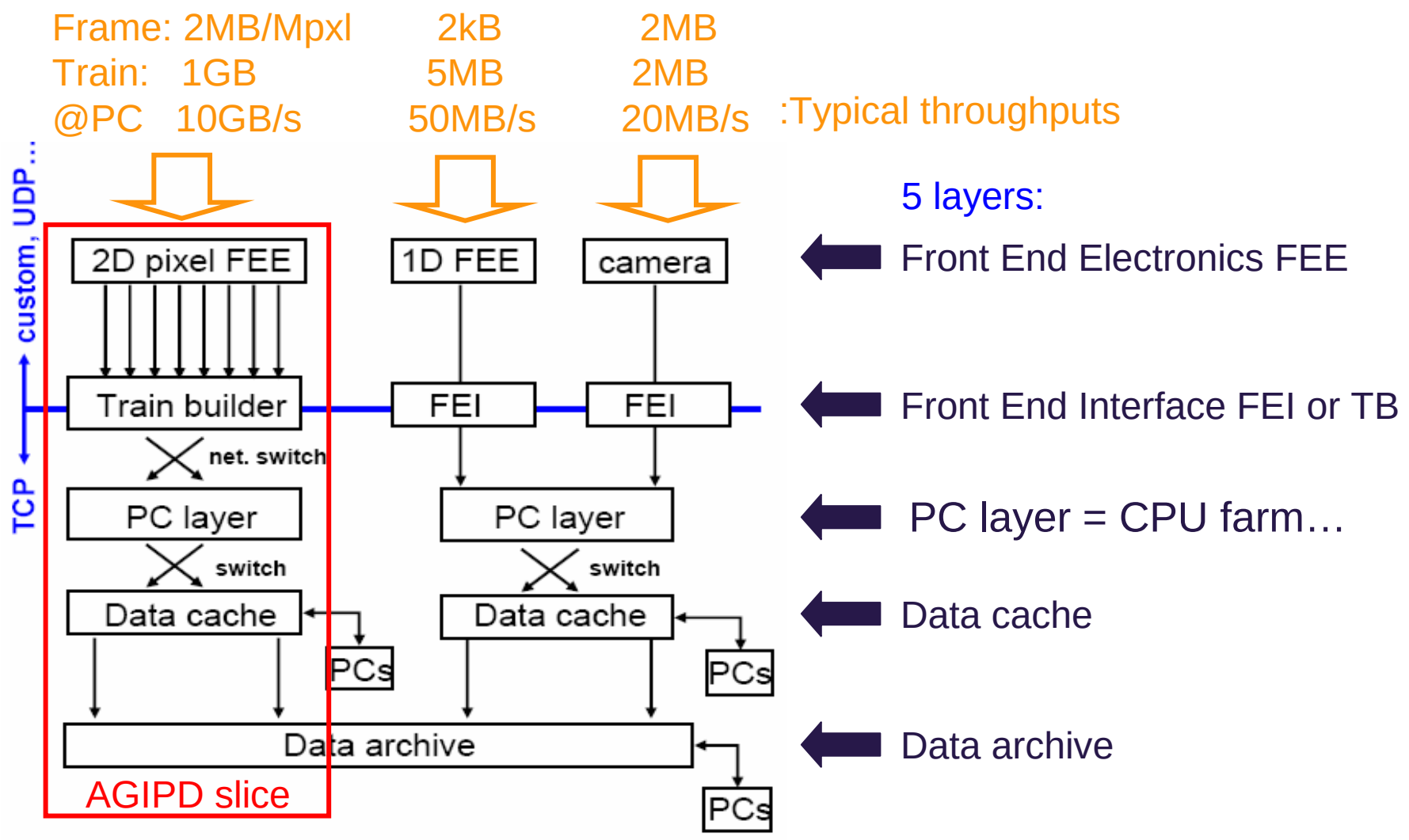
Reminder of DAQ + DM architecture



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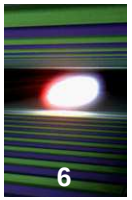
Embedding 2D detectors into architecture



- Three electronics developments started 2008
  - Dual 10Gbps FMC
    - ➔ 1GB/s fibre data transfer per link standard (FEI–FEE–PClayer)
  - Train builder (TB)
    - ➔ Builds max. 512 frames of 2MB size into contiguous block per trains from FEE and sends block to PCLayer
  - Clock and Control (CC)
    - ➔ Sequencer for FEE (interface to EXFEL timing system)
  - Quarterly meeting of experts
    - ➔ http://www.xfel.eu/project/organization/work_packages/wp_76/daq/2d_pixel_detectors/

All necessary contracts have been signed

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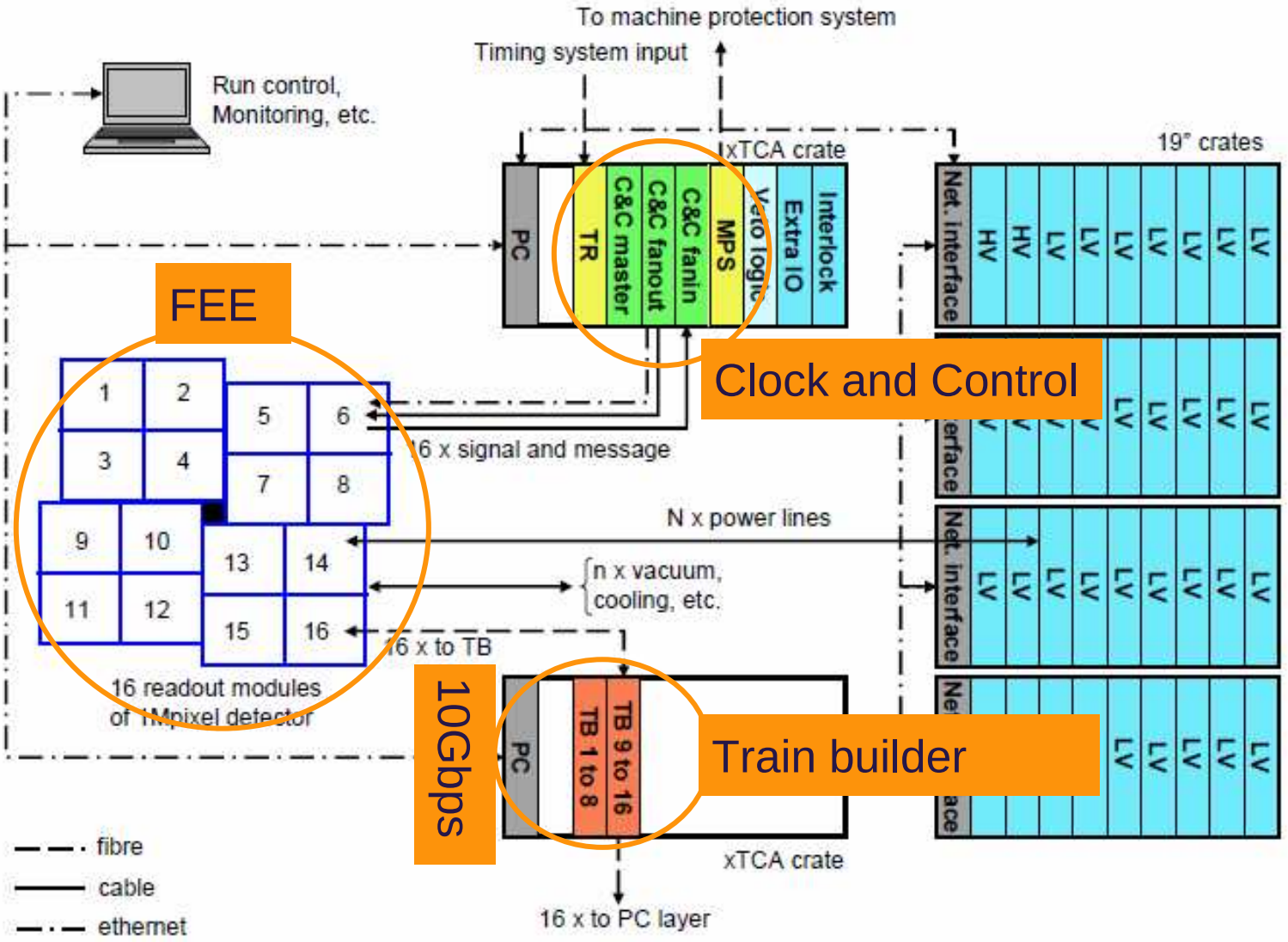
1Mpxl DAQ what it approximately looks like



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10 GE fibre link - status

- Led by DESY-FEA collaboration with STFC and Uni-HD
- FMC mezzanine layout with 2 links (PHY+optical) done
  - board targeted for use in TB, AGIPD, LPD
  - DSSC using own Vertex 6 development
- UDP data transfer rates (of 10Gbit/s max):
  - FPGA to FPGA = wire-speed without losses
  - FPGA to PC (UDP 2009) = 78% without losse
  - Bit transmission Error Rate ~10**-15
- Sufficient PHY chips ordered for targeted users

Source: M.Zimmer, DESY-FEA

First production boards delivered to TB group May/2010

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Train Builder - status

- Led by STFC
- Train builder functionality:
  - Receive data from 16 FEEs/Mpxl
    - → Input FPGA orders and store data in memory
    - → Barrel shifter switch builds full frames (+trains) in output memory
    - → FPGA sends data from entire train to PClayer node
- Work proceeding on Phase 1 demonstration board
  - Tests of memory interfaces using FPGA evaluation boards
  - Tests of FPGA to Mindspeed X-point switch development
  - Layout design of ¼ Mpxl (double width AMC) board started.

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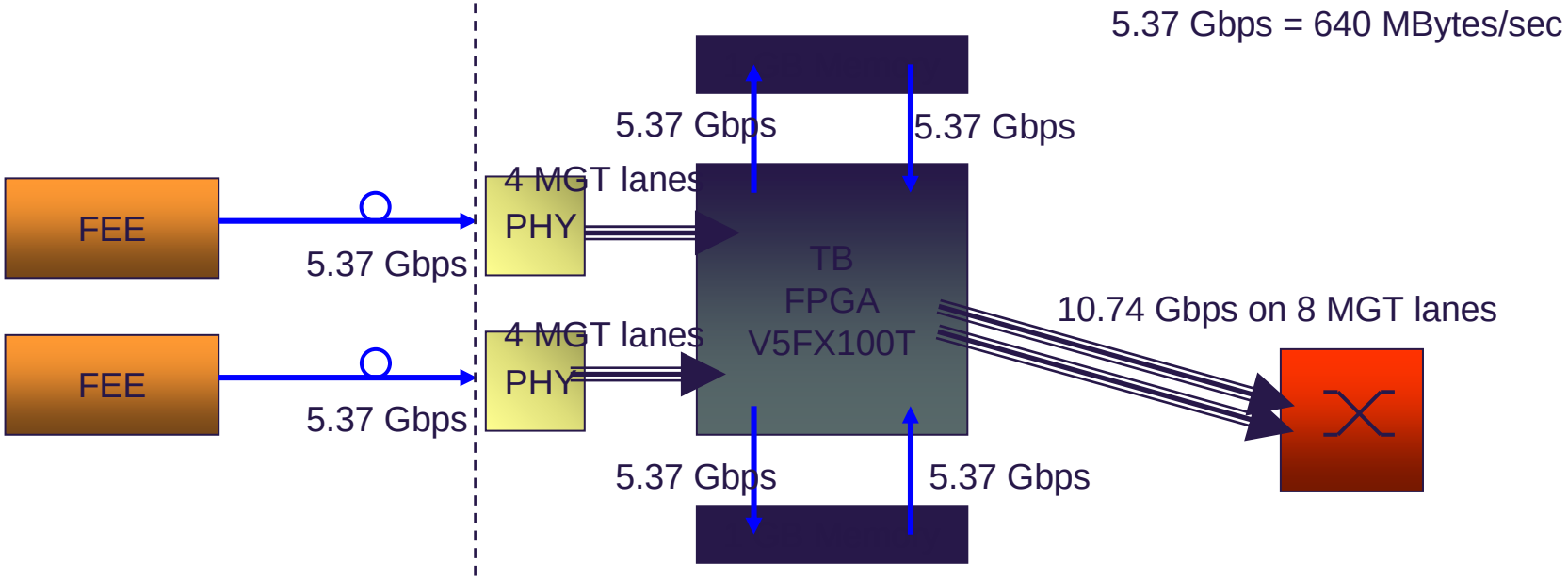
Train builder Data Memory Rates Requirements (clarified)

Source: J.Coughlan, STFC

FEE link 1/16 x 1 Mpixel, 2 bytes per pixel, 512 pipeline depth , 10 trains per second



Each FEE module link delivers ~ 5.37 Gbps pixel data (+ header info, formatting)

TB FPGA handles 2 x FEEs with **2 Memory interfaces**

Each Memory Total I/O Rate ~ 1.28 GB/sec (Concurrent R&W)
Achieved ~ 1.8 GBytes/sec on dev board

IO rates required have been achieved

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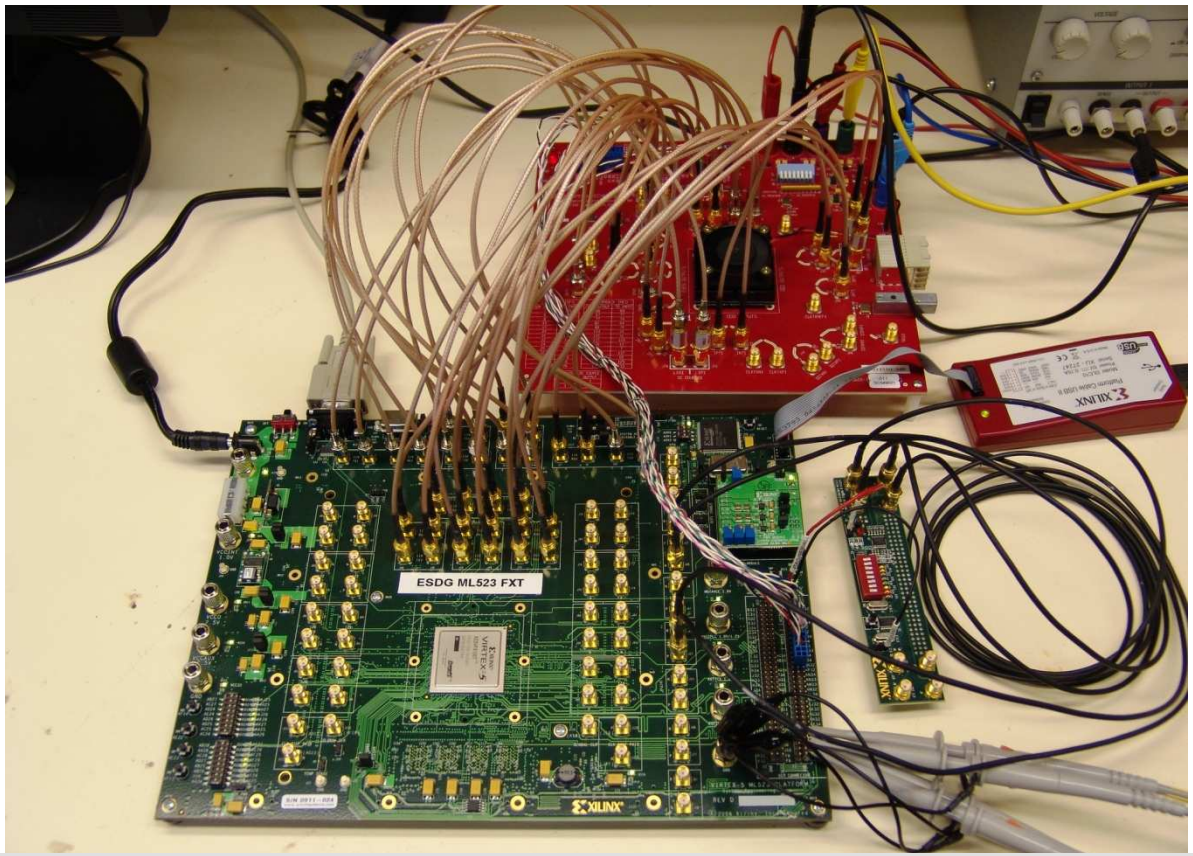
FPGA and XPOINT Test Boards

Source: B.Halsall, STFC



- **MGT**
  - **2 x 4 TX & RX @3G**
  - **16 Diff pairs**
  - **32 SMA Coax**
- **Xpoint control**
  - **9 signals**
  - **4 wire Serial IO**
  - **1 Switch Line**
- **Clocks**
  - **2 diff pairs**
  - **4 SMA coax**
- **RS232**

Programming and synch. issues understood – throughput achieved, no errors

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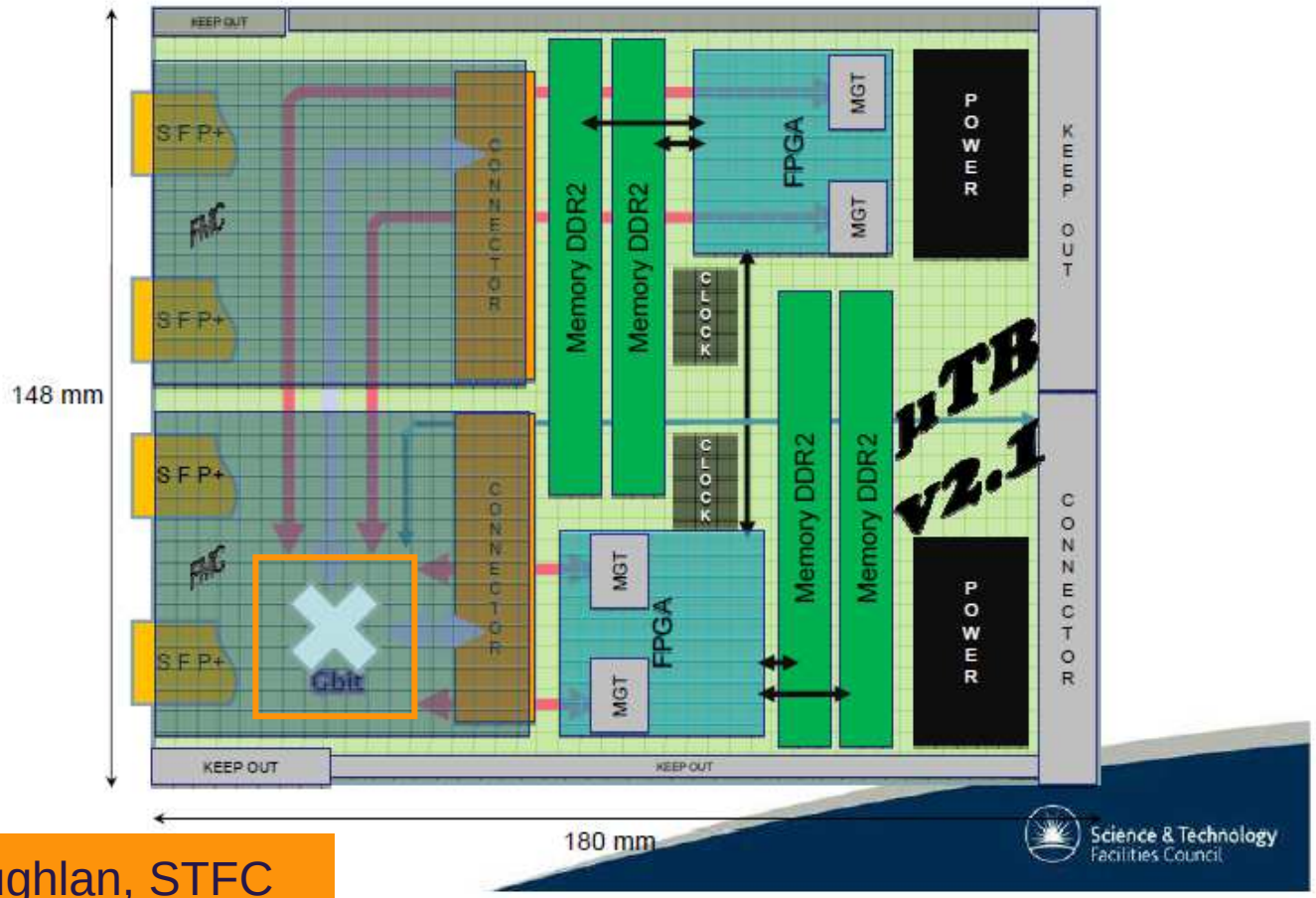
Train builder micro-TCA demonstrator board

- Schematic of Phase 1 demonstrator board started (Sep. 2010)
  - Use to prove TB concept. Expect first PCB ~April 2011



Source: J.Coughlan, STFC

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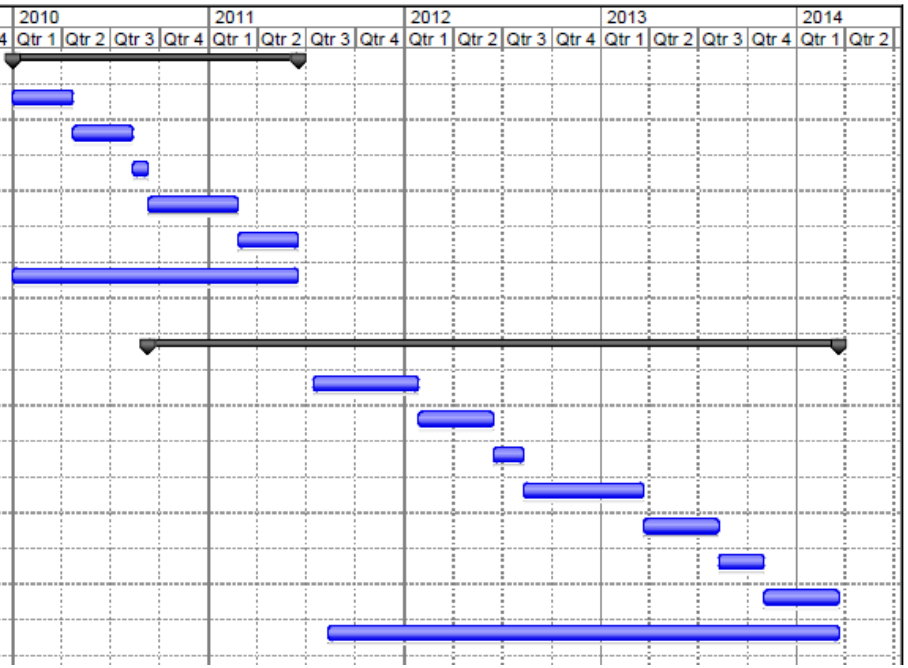
TB time schedules

Task Name	Start	Finish
PHASE 1 : Train Builder Demonstrator AMC	**Fri 01/01/10**	**Thu 16/06/11**
Design Schematics	Fri 01/01/10	Thu 22/04/10
PCB Layout	Fri 23/04/10	Thu 12/08/10
Manufacture	Fri 13/08/10	Thu 09/09/10
Test	Fri 10/09/10	Thu 24/02/11
Iterate	Fri 25/02/11	Thu 16/06/11
Firmware & Software	Fri 01/01/10	Thu 16/06/11
PHASE 2: Train Builder 1/2 Megapixel ATCA	**Thu 09/09/10**	**Thu 20/03/14**
Prototype Design Schematics	Fri 15/07/11	Thu 26/01/12
Prototype PCB Layout	Fri 27/01/12	Thu 14/06/12
Prototype Manufacture (2 off)	Fri 15/06/12	Thu 09/08/12
Prototype Test	Fri 10/08/12	Thu 21/03/13
Production Design changes	Fri 22/03/13	Thu 08/08/13
Production Manufacture (15 off)	Fri 09/08/13	Thu 31/10/13
Production Test	Fri 01/11/13	Thu 20/03/14
Firmware & Software	Fri 12/08/11	Thu 20/03/14



- Due to contract delay running ~6 months behind
- Expect LPD super module tests Summer/Autumn 2011
- Phase 2 = production boards 2013

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Clock & Control

- Led by UCL (University College London)
- Continuing with Phase 1 development
  - Overall design of master and slave boards agreed
  - CC-FEE fast signal spec defined (clock, event, veto, status)
    http://www.xfel.eu/project/organization/work_packages/wp_76/daq/2d_pixel_detectors/clock_and_control/
  - CC-VETO VETO handling specified (variable or fixed latency):
    http://www.xfel.eu/project/organization/work_packages/wp_76/daq/2d_pixel_detectors/clock_and_control/
  - Grounding question resolved and plugs/cables agreed (RJ45,CAT5)
  - CC generic carrier board defined (DESY-FEA DAMC2)
  - CC will use crate xTCA (MTCA.4 pgmic), see single DAQ crate soln.
- Milestones:
  - Workshop with DESY electronics and timing groups held in July
    - ➔ Finalize backplane usage and details of XFEL timing interface
    - ➔ Petra3 timing details and use of timing interface (see single crate DAQ)
  - Phase 1 = single DAMC2 prototype end of 2010 (still possible?)

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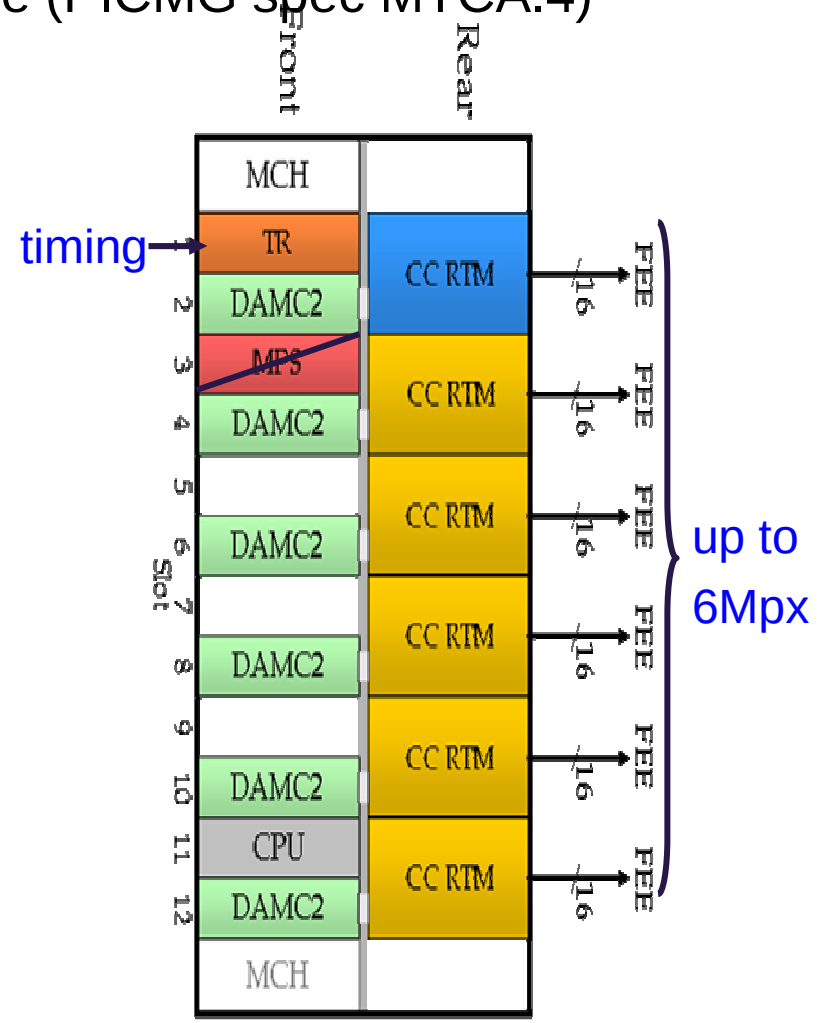
CC Hardware

Uses xTCA for Physics crate & backplane (PICMG spec MTCA.4)

12 slot crate layout:

- LINAC timing receiver board, sources:
  - timing and data telegrams onto bussed lines
  - 99MHz and 4.5MHz p-2-p clock signals
- DAMC2 digital card host:
  - CC master board
  - Additional CC slave boards
- Rear Transition Module (RTM):
  - Connector platform for IO with camera FEE
- MCH hub:
  - Mediates p-2-p, PCIe, etc. on backplane



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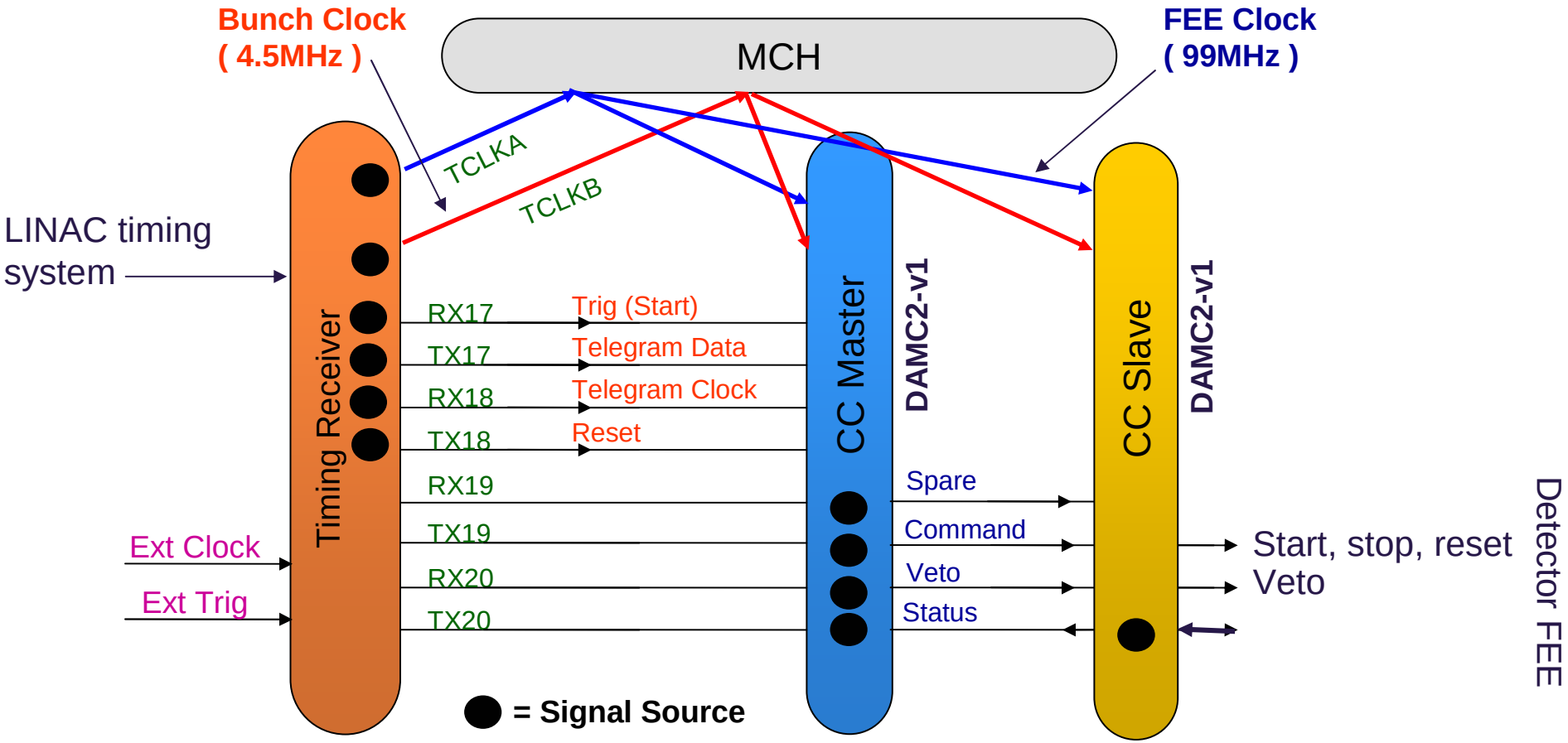
CC backplane signals – phase 1 board



Phase 1 = TR board clock distribution + MCH jitter ~100ps
phase 2 = DAMC2-v2 clock distribution + MCH jitter ~few ps

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CC time schedules

GANTT chart (Clock and control system for 2D Megapixel detectors)

	Task name	Start date	End date	2009		2010				2011				2012				2013			
				Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
1	Phase 1	2009-10-01	2011-03-31																		
2	Trigger dev board	2009-10-01	2010-03-31																		
3	Firmware	2009-10-01	2011-03-31																		
4	Design	2009-10-01	2010-03-31																		
5	PCB layout	2010-04-01	2010-08-16																		
6	Manufacture	2010-08-17	2010-09-30																		
7	Test	2010-10-01	2010-11-30																		
8	Detector integration	2010-12-01	2011-03-31																		
9	Phase 2	2011-04-01	2013-09-30																		
10	Firmware	2011-04-01	2013-09-30																		
11	Design	2011-04-01	2011-09-30																		
12	PCB layout	2011-10-01	2012-03-30																		
13	Manufacture	2012-04-01	2012-06-29																		
14	Test	2012-06-30	2012-12-31																		
15	Integration with detectors	2013-01-01	2013-09-30																		

- Due to contract delay running ~6 months behind
- Expect first 1Mpxl prototype Spring/Summer 2011

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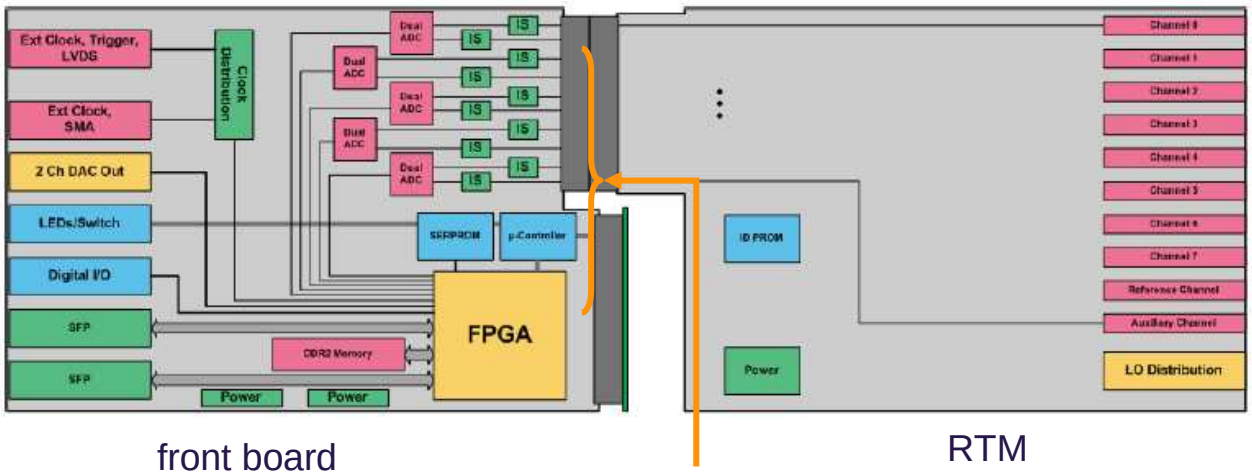
Single crate DAQ development

- Developing a single crate DAQ system
  - Based on XFEL LINAC control xTCA crate standard (K.Rehlich)
    - ➔ double width Micro TCA with open upper half backplane
  - Front side digital (FEI) board, either:
    - ➔ DESY-FEA DAMC2 generic Vertex5FPGA board, or
    - ➔ COTS, e.g. STRUCK SIS8300 125MHz 10 channel ADC
  - Rear Transition Module (FEE) board
    - ➔ Hosts analogue-to-digital sensor interface (shaper, ADC…)

STRUCK (shown) or DAMC2



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Single crate DAQ development

- Aimed at detectors / systems
  - 4-8 APD channel readout for Ch.Bressler at Petra3
  - VETO system management (input to 2D CC veto dist.)
- Milestones for APD system using STRUCK SIS8300
  - May-Jun: design, simulate, prototype 1 channel shaper (RTM)
    - ➔ First PCB expected mid Oct for tests.
  - Sep: acquire Schroff crate, cpu, and hub
    - ➔ Has arrived and being tested
  - Sep: acquire STRUCK 10 channel 125MHz ADC board
    - ➔ Now expect end of next week
  - Oct-Dec:Interface DAQ to XFEL timing receiver board firmware/control
  - Oct-Dec:Interface DAQ to STRUCK ADC board firmware/control
  - Feb 2011: Commissioning at Petra3

Use this to test DAQ and control hardware and software.

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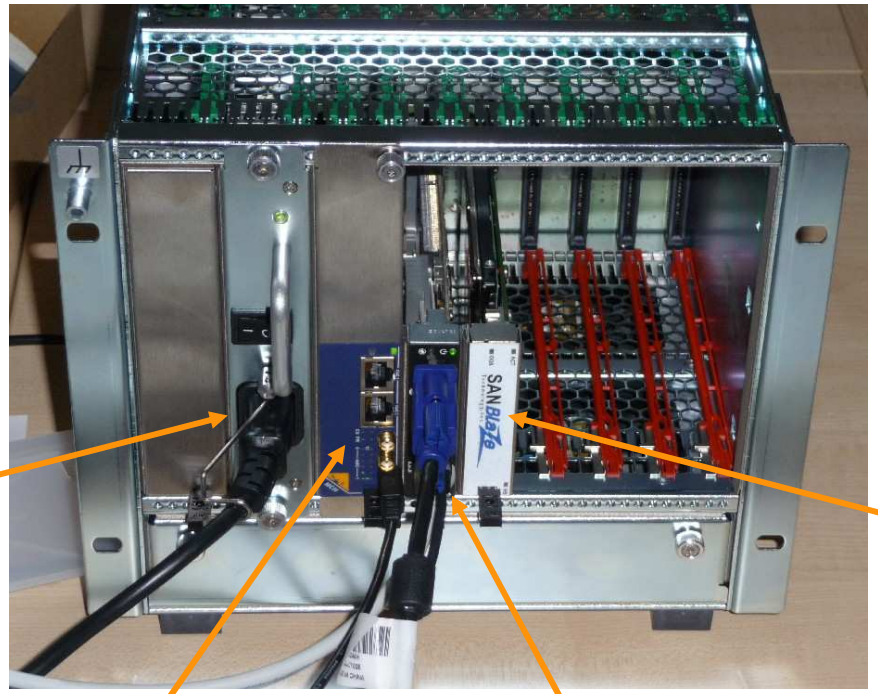
xTCA for Physics 6 slot Crate (Schroff)

- Intelligent Platform Management Interface (IPMI)
  - Remote control and monitoring of slots boards, PS
  - Hot swap and power management
  - Identification of backplane and boards



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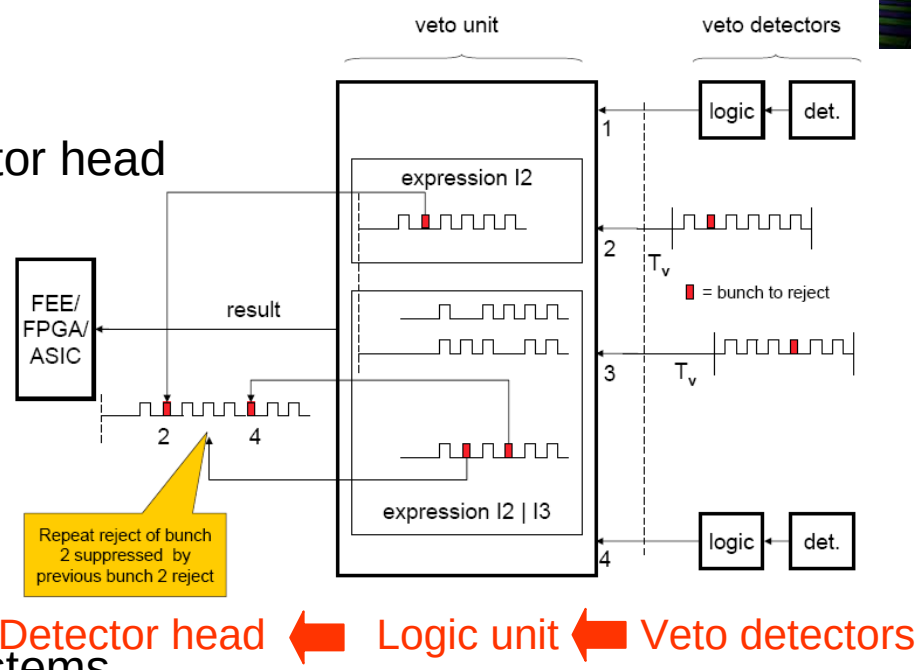
The veto system

- Purpose:
  - reject low quality images at the detector head
- Aim:
  - improve quality of images taken,
  - reduce data volume to backend,
  - optimize storage pipe line usage,
  - i.e. similar to HEP FLTriggers
- Scope:
  - conceived for large area 2D cameras
  - could be used by all DAQ readout systems



- Implementation using xTCA for Physics crate digital boards:
  - multiple conditioned signals from VETO sources (APDs, etc.) received on RTM
  - VETO generated by evaluating logic clauses in FPGA of RTM's host board
  - Bunch number to be VETO'd distributed to detector head
  - For AGIPD+ distribute result via Clock and Control system

Implement by reprogramming DAMC2 in single crate DAQ
Using custom RTMs to connect sources and users.

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Software status

- Ingredients:
  - GUIs for control and monitor
  - Messaging system to interconnect processes
  - Job control system to ensure that processes are started
  - Finite State Machines to navigate transitions
  - Viewers to see the data
  - Logging
  - …
- Have most of these in various degrees of completeness

Need challenge of using in running systems, see next slides

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XCAM status and aim

- XCAM in BBL2 at FLASH
  - 2Mpxl / detector – 2 detectors
  - ~1Hz readout over USB
- Took data 22.9.2010 last 15 minutes of 15-22.9.2010 run
  - 136 images recorded (HDF5 format defined by Nicola)
  - Droplet injected sugar cluster target
  - ~10% target efficiency
- Aim
  - Test software: RC GUI, FSM, JC, XMS on Linux
  - Interface other devices (shutters…)
  - Generate HDF5 output file format
  - Replace windows with linux DAQ and control system

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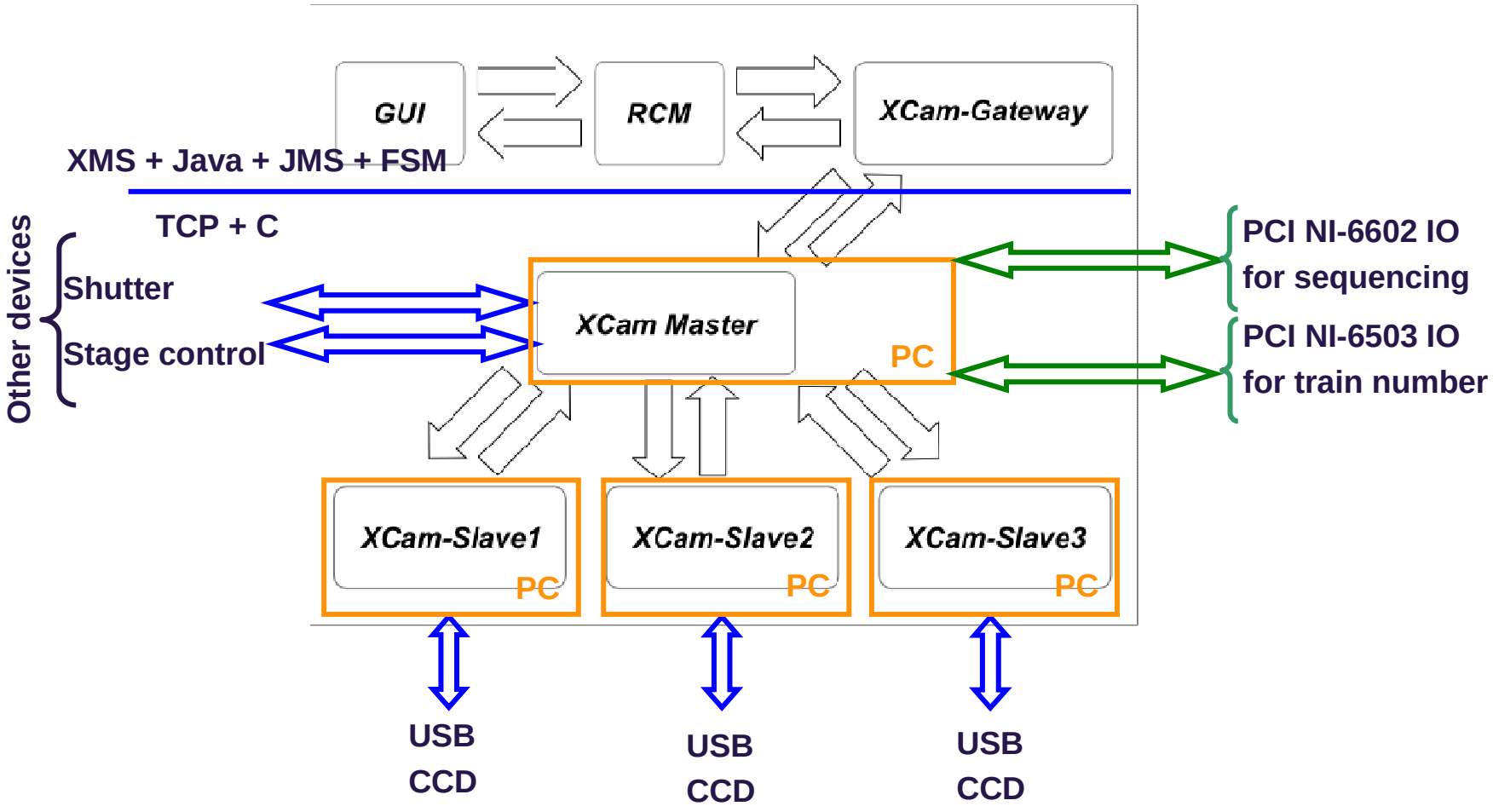
XCAM DAQ overview



This running period = half-way to software we would like to run

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XCAM challenge – full and partial successes

- Control
  - GUI worked (used LibConfig configuration)
  - FSM worked (interfaced to external systems)
  - JC worked partially (used LibConfig configuration)
  - XMS “tagged string” message introduced to match c-layer
  - TCP library used into and throughout c-layer
  - Interfaced to other control devices worked
- Readout
  - USB readout (setup 2009) worked
  - Files written to disk in HDF5 format
  - Interface to synchronizing and train number Nat.Inst. worked (kernel dependent?)
- Took data !

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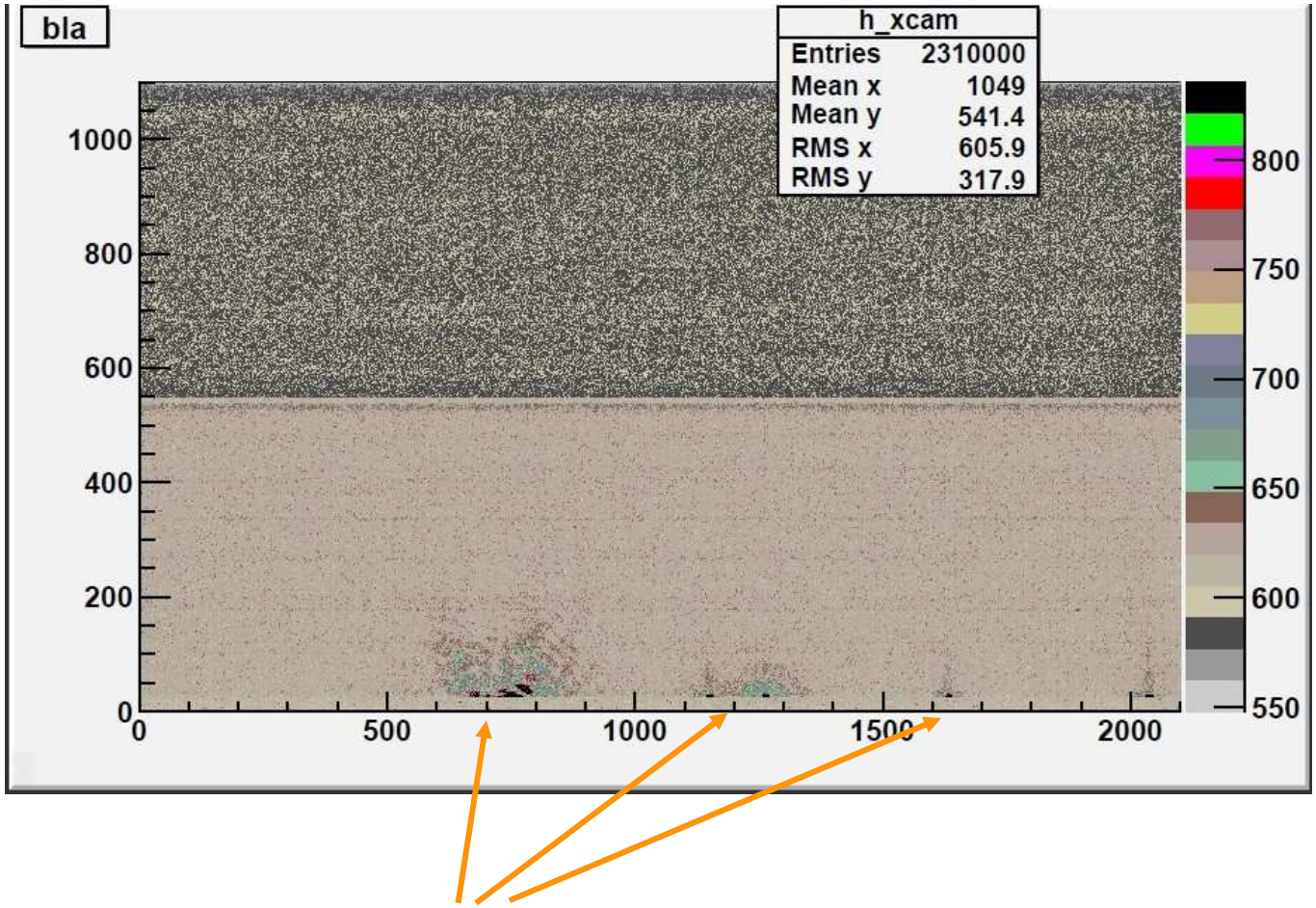
XCAM – typical picture

Image for 1 CCD



1 image contains multiple target hits = synchronization problem

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XCAM conclusions – not exhaustive

- XCAM currently only active WP76 “test” detector
  - requested permanent availability of detector (H.Chapman)
    - ➔ continue using system as development platform
  - Next running period March 2011
- Aimed at changes for next running period
  - DAQ and control:
    - ➔ Use XMS throughout - C or C++ bindings.
    - ➔ Separate data online data viewer
    - ➔ Improvements: JC … GUI …
    - ➔ Use of improved configuration mechanisms
  - DM
    - ➔ HDF5 handling support (rewrite) needed
    - ➔ Catalogue and metadata of data taking
- i.e. use as test bed for our ideas

Next running period in March 2010

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AGIPD FEE micro-processor and slow control

- Dana and Peter Jan-Mar. 2010
  - Selected micro-processor evaluation system
  - Network booted Linux OS
  - Benchmarked network and process context switching
  - WP76 work with the microcontroller will resume once AGIPD resumes work on it.
- Slow control
  - Work on the HV and LV systems (if still required) is pending implementation decision from AGIPD
  - Other systems (e.g. interlock, IO…) can now probably use DAMC2 boards in xTCA crates. Plan needs developing

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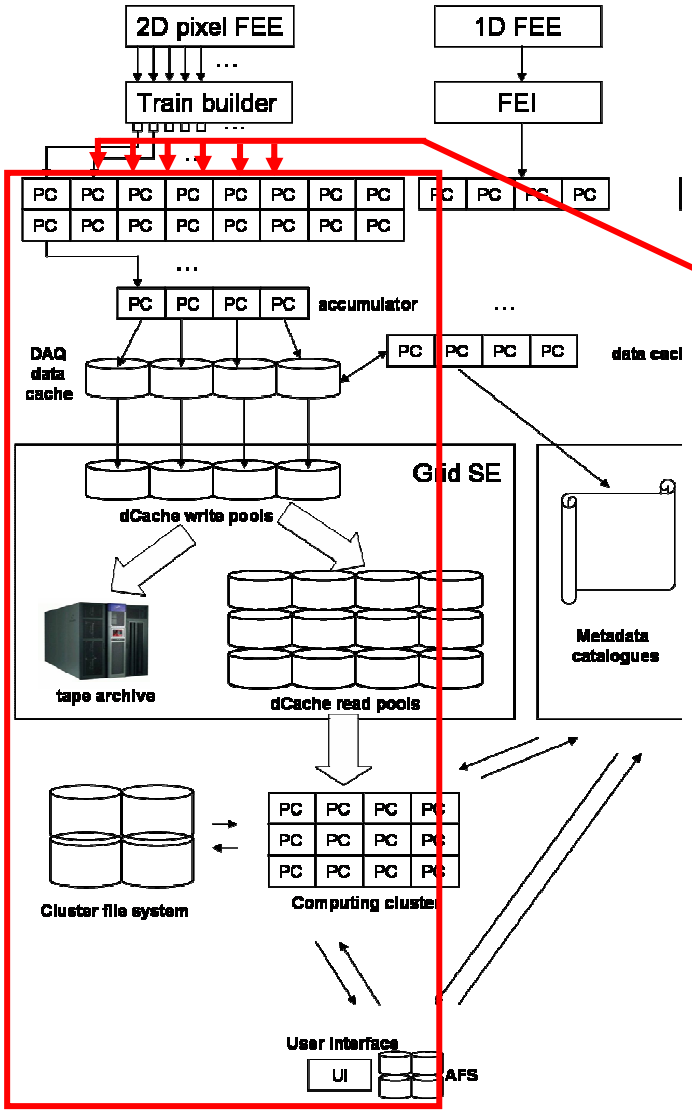
DM, test hardware related news



- Test of DAQ/DM architecture slice in 2011
  - purchasing of equipment stated (just!)
- Idea is to test slice feasibility
  - e.g. use rack CPU blades to feed data into system
  - e.g. take data through PClayer to Data Cache and archive layers
  - e.g. test meta data handling
  - e.g. test data caching and archiving performance

Not explicitly mentioned DM work by Krzysztof et. al. – you should expect great things at the coming XDAC !!

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Conclusion

- No show stoppers seen in the electronics development or DAQ and control software
- Challenging ideas by involvement in data taking experiments
- Should review time schedules
  - have to update for coming XDAC
  - thought to be OK.