Capacitance calculations in p^+n silicon pixel sensors using three dimensional TCAD simulation approach

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Abstract—Science at the European XFEL (x-ray Free Electron Laser) requires precision p^+n Si pixel detectors as a first choice which need to withstand a dose of up to 1 GGy of 12 keV X-ray (10^{16} γ/cm^3/pixel) for three years operation. The sensors design is an important issue for the satisfactory performance at the XFEL and the noise in the readout electronics of the detector system is crucial parameters that should be minimized so for this we have proposed design of sensor pixel array with an optimum gap for the interpixel and backplane capacitance calculations using Synopsys TCAD commercial simulation program 2010.03. In this letter, we have compared the normalized 2-D and 3-D simulation results on p^+n Si pixel detectors with analytical calculations and the observations are presented.

Index Terms— Device simulation, interpixel capacitance, back-plane capacitance, radiation damage effects.

1. Introduction

At XFEL experiment, sensors should have high voltage stability up to 500 V to avoid charge explosion effect [1] with some safety margin and should have low interpixel capacitance up to 0.5 pF [2]. In our previous simulation approach, we have proposed the optimum gap for the low interpixel capacitance [3]. Here we have used the optimum gap spacing between the adjacent p^+ pixels for the capacitance calculations. The cross-talk effect is not taken into considerations.

The capacitance calculations using ISE TCAD software, HSPICE [4], and analytical calculations using 3D Laplace equation [5] is already performed for the rectangular and square type of pixels.

Here we have also shown the capacitance calculations for 3x3 sensor pixel array and the results are presented.

2. Device design and simulation technique

The p^+n Si pixel sensor is made on 500 µm thick n-type high resistivity Si material (3-4 kΩ-cm) which is an equivalent to substrate doping concentration of $1x10^{12}$ cm^{-3}. The p^+ impurity profile is approximated by assuming a Gaussian profile with a peak concentration of 5×10^{19}/cm^3 at surface and at junction 1×10^{15}/cm^3. The same doping profile is assumed in all p^+ pixel regions. The backside is implanted with n^+ of thickness 1µm and then metallized with Aluminium (Al) of thickness 1µm to take ohmic contact. . It is assumed that lateral diffusion depth at the curvature of the p-region is equal to 0.8 times the vertical junction depth. p^+ pixel implants are grounded through an ohmic contact (not shown in the figure) and are DC-coupled to the Al metal. Fig.1 is showing the top view of the 5x5 sensor pixel array and the floating guard rings surrounds the pixels but 3x3 portions of 400x 680 x 500 µm^3 is simulated here because the effect of second neighbours is not important in the square pixel geometry. In the fig.1, d_{gap} is showing the distance between the pixels, W is the width of the pixel. The rest symbols used in the fig.1 are shown below:

The capacitances are as follows:

C_0 – Back-plane capacitance,

C_1- Capacitance between adjacent pixel,

and C_{diag}- Diagonal capacitance.

The sensor is simulated using Synopsys TCAD 2010.03 [6] commercial device simulation program.

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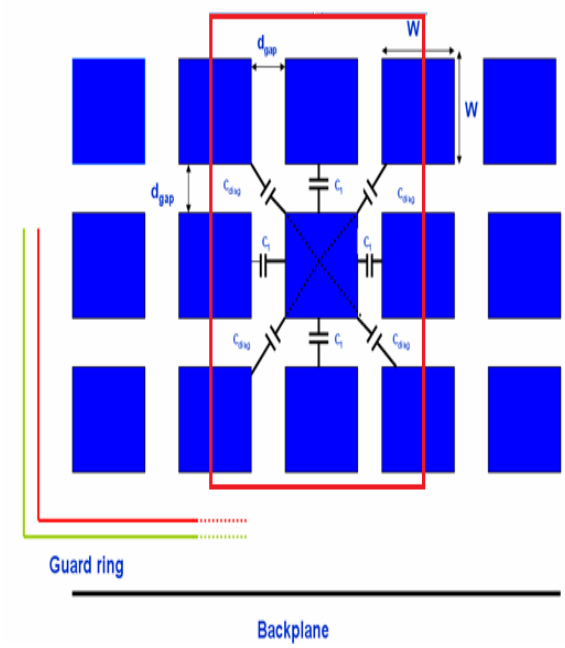


Figure.1: Layout of 5x5 sensor pixel array. The simulated portion is marked by red colour.

The SRH (Shockley Read-Hall Recombination) recombination, Auger recombination, Impact ionization, doping dependent mobility, high field saturation physical models are used to initiate the device simulation program. The default Dirichlet and Neumann Boundary condition is applied at contacted and non-contacted edge of the sensor pixel array. The small signal AC analysis is performed for the capacitance calculations at 1 MHZ frequency to measure the real and imaginary part of the admittance at different voltages in between the different resistive electrodes. For the comparison with published analytical calculations, an ideal condition of the sensors is used.

3. Physics of the pixel capacitances

A crucial factor in evaluating the noise contribution of DC coupled p^+n Si pixels sensor is the sum of the value of the direct capacitances between adjacent and diagonal electrodes called interpixel capacitance (C_{int}). The total capacitive load for sensor pixel array can be approximated by C_0+4 C_1+4 C_{diag}. The effect of other long placed pixels on the center pixel can be neglected.

The relation of equivalent noise charge (ENC) with total detector capacitance (C_D) is by $ENC^2 \propto 24kT(C_D+C_{FET})^2/(3g_m)$, where C_D consists of two terms backplane capacitance and interpixel capacitance, C_{FET} is the capacitance associated with the input FET of the preamplifier, k is the Boltzmann constant, T is the absolute temperature and g_m is the transconductance of the input FET. The significance of studying C_{int} *is further attributed to its creation of cross talk [7-8]*. The cross-talk can be calculated by $C_1/C_{bump.bonded}+C_{pre-amp}+C_{total}$. The cross talk can reduced by increasing the total capacitance like an addition of some metal on ground routing between the pixels. Thus, for the above reasons it is important to investigate the characteristics of the Si pixel sensor in terms of the interpixel capacitance. The present work is an attempt in this direction. In this paper, 2-D numerical device simulation using Synopsy TCAD 2010.03 has been exploited in order to evaluate the mutual capacitance between two facing strips. Through small signal AC-analysis, the admittance matrix of the network shown in Fig.1 and it can be solved at an arbitrary bias point, from which mutual capacitance and conductance between the facing and diagonal pixels can be estimated. In AC coupled Si pixel sensor, the contribution to interstrip capacitance (C_{int}) between adjacent and diagonal strips mainly comes from four components: (1) The capacitance between metal of *i*th and *j*th strips (C_{Mi-Mj}), (2) the capacitance between the implanted strips (C_{Ii-Ij}), (3) the capacitances between a metal and adjacent strip's implant (C_{Mi-Ij}, C_{Mj-Ii}) and (4) the coupling capacitances between a metal strip and implanted strip (C_{Mi-Ii}, C_{Mj-Ij}). However, it should be noted that the coupling capacitances C_{Mi-Ii} and C_{Mj-Ij} are usually much larger than the remaining parasitic components in order to avoid spreading of the signals on the pixels, so that we can consider their impedance to vanish in the high frequency range of interest. Thus, to first order approximation, we can assume that the total interpixel capacitance between two facing and diagonal pixels is given by C_{int}= C_{Mi-Mj} +C_{Ii-Ij} +C_{Mi-Ij} , *wh*ere, C_{Mi-Ij} includes the contribution of both the capacitances between M_i–I_j and M_j–I_i. The value of the capacitance between the read out electrodes C_{Mi-M} is usually smaller than other two capacitances because of the air dielectric capacitances. The shape of the CV (capacitance-voltage) curve for the different capacitances between the electrodes is depends upon the several parameters like width by pitch ratio, metal over hand width, surface irradiation doses, bulk related deep trap effects after hadronic irradiations etc. At XFEL experiment, the surface damage effects (N_{ox}, D_{it}) in silicon pixel sensors is dominant therefore two lumped, three lumped model or several can be drawn in order to understand the shape the C/V curve. Here, we have

proposed the two lumped models for two facing pixels (see Fig.2).

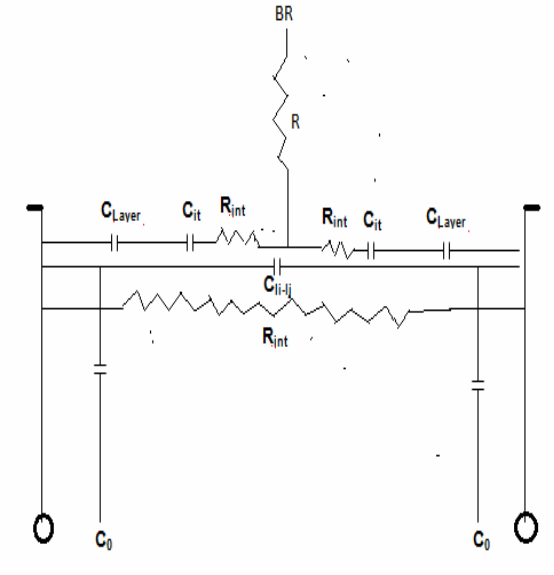
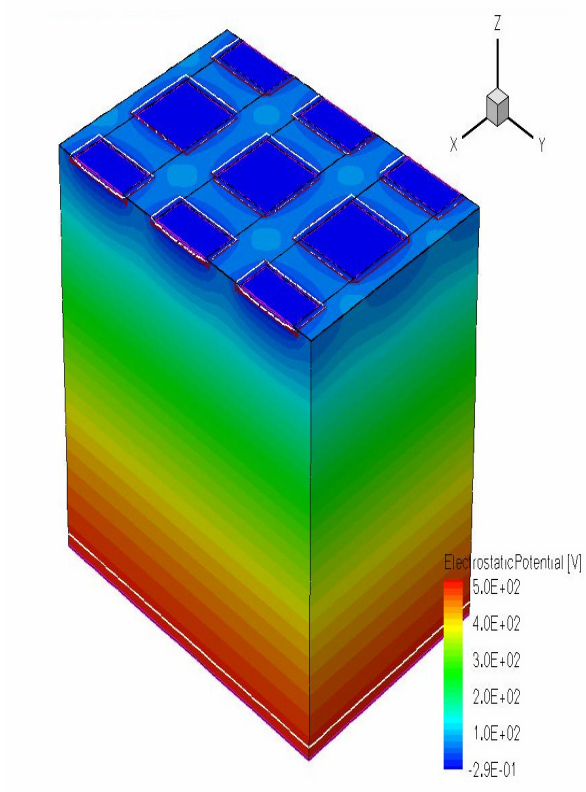


Figure.2: Two lumped model for the C/V curve description of two adjacent strip/pixel sensor.

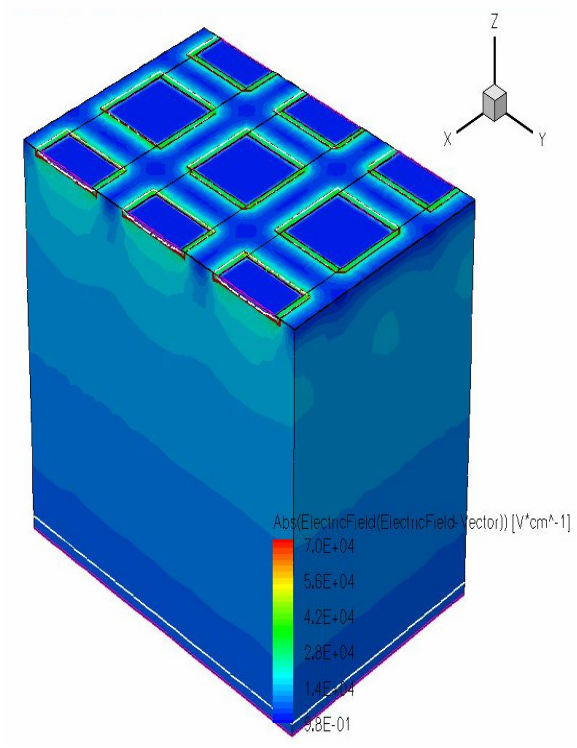
In the presence of surface charge effects, an accumulation layer of fixed oxide positive charge and interface trap at Si-SiO_2 interface will be developed. In fig.2, it can be see that the net list of RC network of physical parameters in two strip-pixel subset of sensors. In Fig.2, C_{Layer} is the capacitance between the pixel and accumulation layer of free electrons, R is the resistance of the accumulation layer and C_{it}, R_{it} is the capacitance and resistance of the interface trap.
The interpixel resistance is represented here by symbol R_{int}. The left and right part of the fig .2 can be expressed as C', and C'' and the C' is serial combination of C_{int}, C_{it}, and C_{Layer} and similarly the second right part of the Fig.2. The total parallel capacitance is the sum of the serial combination of C', and C'' and the conductance is the sum of all inverse resistances

4. Results

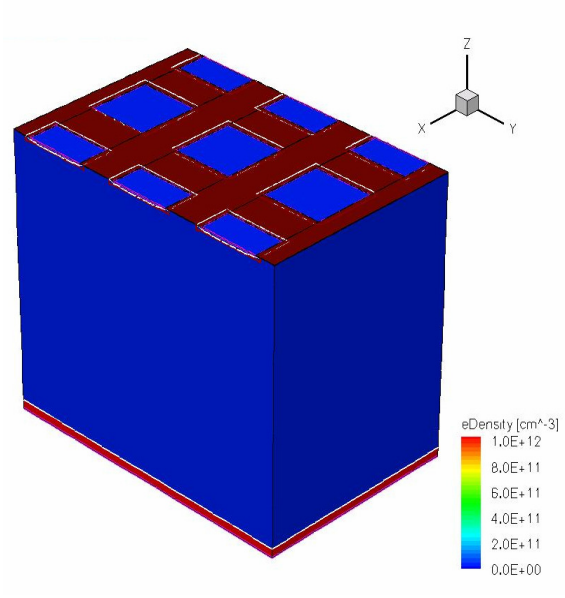
In this work, sensors pixel array is simulated using Synopsys TCAD for the capacitance calculations. The electrostatic potential distribution, E-field, and e-concentration is shown in order to see the depletion behaviour and magnitude of the E-field inside the sensor (see Fig.3).



(a)



(b)



(c)

Figure.3: (a) Electrostatic potential (b) E-field (c) e-concentration inside sensor pixel array at 500 V bias voltage and 1 MHz frequency.

The change of the interpixel capacitance in between the different adjacent electrodes and diagonal with applied bias voltage is shown in the Fig.4. The initial decrease of the capacitance with voltage is due to the capacitance contribution from the back- plane of the sensor and for further an increase of the voltage the capacitance increases because of the contribution of the capacitance from the backplane into the direct interpixel capacitance because of the small ac signal is coupled to the back-plane (see Fig.2 for explanation). Table.1 shows the simulated back-plane and 1st neighbour's capacitance, and diagonal capacitance. In an irradiated sensor, frequency effects can be easily explained from the model shown in Fig.2 with the C_{Layer}, and C_{it} parameter..

Table.1: Comparison of 3-D simulated capacitances with analytical expressions for 80 µm p^+ pixel gap.

Capacitances	Analytical calculation [4] in fF	Simulation [S] in fF	Error [%]
C_0	7.68	8	5
C_1	5.099	5.48	22
C_{diag}	1.355	1.94	34

It has been found that the there is an agreement with 5 % with back-plane capacitance whereas in the capacitance for the first neighbours is within 22% and 34% in diagonal capacitance.

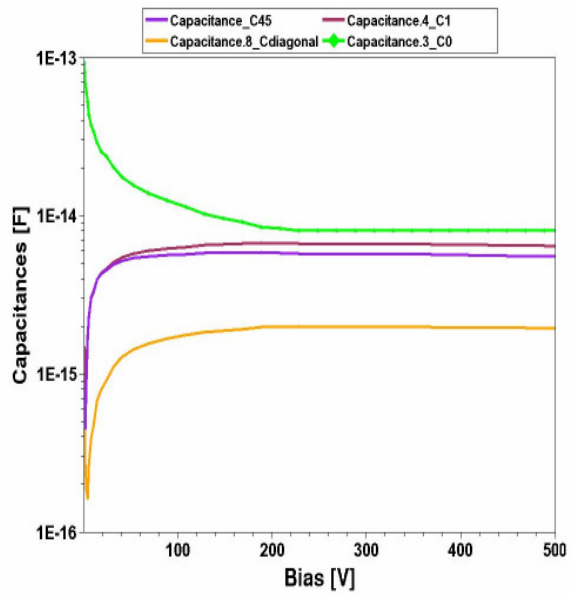


Figure.4: Interpixel capacitance as a function of the applied voltage at 1 MHz.

Table.2: Comparison of 2-D and 3-D simulated back-plane and interpixel capacitances with analytical expressions for 80 µm p^+ pixel gap.

Capacitances	Analytical calculation in fF		C_{Sim}-Synopsys (2D) in fF	C_{Sim}-Synopsys (3D) in fF	Implications
Back-plane capacitance (C_0)	$C_{pixel}=C_{strip}$*Length Cstrip is in good agreement with theoretical calculations [9]	[5]	8.28	8	~ 100 % good agreement in 2-D and 3-D simulation result and [3]
	8.3	7.68			Analytical calculation result [1] and with [3] and 3-D simulation, agreement within 4 %
Total capacitive load (Without approx 100 fF from bump bonding +preamp load)	33.438 [5]		53	39.9	Agreement between 2- D and 3-D simulations within 25 % and analytical calculations within 16% - Results are consistent with [2]

It has been found that the simulated back-plane capacitance using 2-D (normalized for 200x 200 μm^2) and 3-D Synopsys TCAD simulation is in almost 100% good agreement with the analytical expressions [3] where from [1], the agreement is in within 5 %. The agreement within 25 % for 2-D and 3-D simulated total capacitive load and within 16 % with analytical expressions given in [1]. The results are consistent with previous published work [2].

5. Conclusion

The first AGIPD pixel sensor prototype fabricated by Hamamtschu (HPK), JAPAN will consist of p^+ pixels in the n- bulk because of the successful operation up to 500 V without any avalanche breakdown and low fabrication cost, easy fabrication technique and expertise has expected no problem of sparking at the edge of the sensors due to the guard- ring biasing scheme. This optimized technology with 80 µm optimum gap ensures low total capacitive load up to 140 fF including contribution from bump bond (can be estimated) and charge sensitive pre amp load at the readout of ASIC electronics and the observed results are consistent with the previous published work.
In our previous work we have already optimized the sensor design using 2-D simulation approach with sufficient radiation hard hardness up to 5 MGy x-ray dose (annealed 60 min 80^0C). Therefore from the present analysis, total capacitive load of 250 fF is estimated in the breakdown protection field plated sensor array structure irradiated by 5 MGy x-ray dose (annealed 60 min 80^0C).

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