Interface electronic

Peter Göttlicher, DESY, 07.April 2009

Outline

- News from clock and control, train builder
- Defining interface to ASIC
- FPGA estimations and status
- Getting to “16x16” system: Fast

News from Clock and control

A clock and control meeting for all 2D took place

To XFEL-responsible:

Question: “Is there a stable clock of around 100MHz”

Answer : “No only at 1.3GHz” well before train (10-20ms)

on that level synchronized to German power system.

Consequences:

- PLL’s will have to resynchronize

… serializing ADC’s (like our’s)

… higher speed digital logic

- my request to 2D-clock&control: only elongated pulses

My Option: should be avoided, **Yours, ASIC?**

News from Train builder

- Next meeting April 23rd, 2009
- Up to 16 module/1MPixel, each with one10Gbit-Ethernet
  OK, we combine from backplane onwards
  2x8 ASIC's to one module…. 16 Modules
- Prototype module available (I.Sheviakov)
  under test with an 10G-PC-environment
- Common data protocols with
  checksum and redundancy under discussion
  2Bytes per Pixel: For us: 14bits-ADC+2Gain

Defining interface to ASIC

Last meeting: Effort to DESY- shoulders:

Document now distributing

… written by “interface”

… Please comment from ASIC/HDI a.s.a.p.

… No board level development before

Major points on next transparencies

… analogue I/O

… Slow control

… pattern generators

… power and HV

Defining interface to ASIC analogue I/O

One input to ASIC:

- default 0.5V: For calibration 0 to 1V
  0.1%-f.s. accuracy for 1/256
  Relative to a delivered GND-ref (around GND-LV)

Four differential output

- up to 50MS/s: same or n/m for analogue, gain
- -1V to +1V for pedestal to full scale
- common mode [0.8,1.2]V
- load differential 100Ω, common mode 1kΩ/2
- Frequency: 10bit settling in 50ns, Interface low pass

Gain and references: onto analogue lines as analogue

Pin count: 128 pins to HDI

Defining interface to ASIC Slow control

"**I2C like**", we talked always about that

- 1MHz (3 second for complete load with 2Byte/pixel)
- ASIC specific command and "common" command

  4 bits ASIC-address but 5 bit command-address

  remaining command-addresses for interface
- no termination, which loads????

2 pins from backplane to HDI

Defining interface to ASIC Pattern generators

4 differential pairs

100MHz-system

For Pipeline: Sampling clock, increment/reject

calib.trigger

2 single ended

Read/write-bar, standby

Hard definitions open questions

Protocols to reduce pin count: Have a look

ASIC reset from I2C and from pattern generator

Debug information

Pin count: 10 pins

Defining interface to ASIC Power

Quite open parameters,

… but essential to do any development

… first start: laboratory supplies

List of parameters:

… voltage

… stability

… accuracy

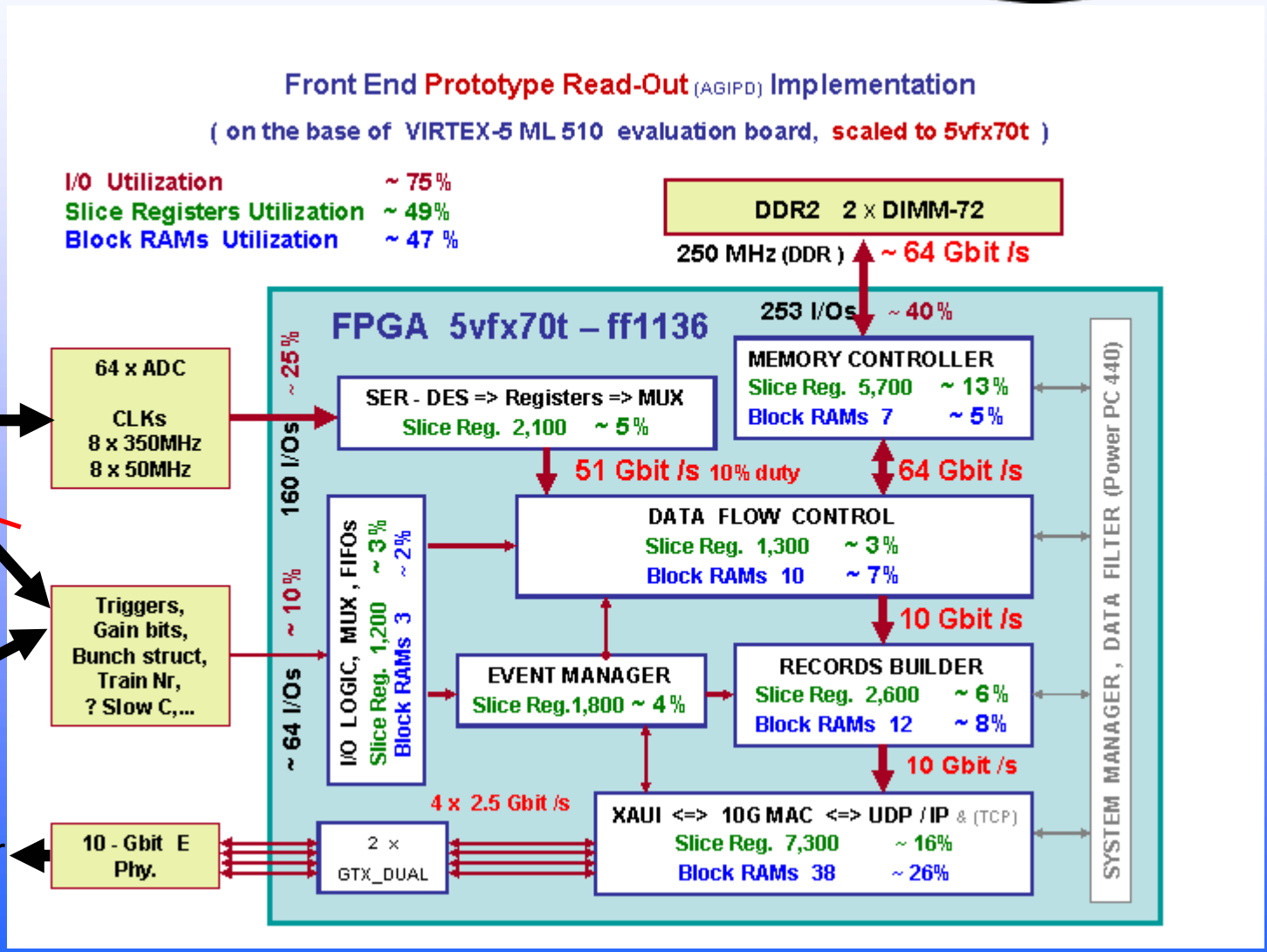
… ripple

… current

… current, what changes in operation?

High voltage:

FPGA estimations and status



FGPA - numbers

FPGA 5VFX70T-ff1136 Resources Utilization

for Front End Read-Out (AGIPD) Prototype Design

5VFX70T-ff1136	Bonded IO	Block RAM	Slice Registers	
144 bits DDR2 Controller	253	7	5670	
ADC interface	160	0	2120	
10G MAC+XAUI+UDP	0	38	7260	
Trigg, SC,..interfaces	64	3	1160	
Event/Data Logic	0	22	5720	
Utilized	477	25	21930	
Available	640	148	44800	
Utilized(%)	75%	47%	49%	

Getting to “16x16” system: Fast, “no definitions”

We have

- 10Gbit development
- ADC evaluation

In production

- Interface ADC-evaluation to 10Gbit-development

…….. **That is the basics as specialties**

But no common program

But not:

- analogue signal filter:… Need specifications not in beginning?, experience
- pattern generator…… **Buy for PXI** (control system) or VHDL on evaluation
- I2C..... No definitions

Just to keep the template