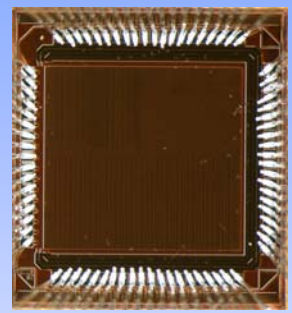
HPAD 0.1



Test & Irradiation Campaign Report

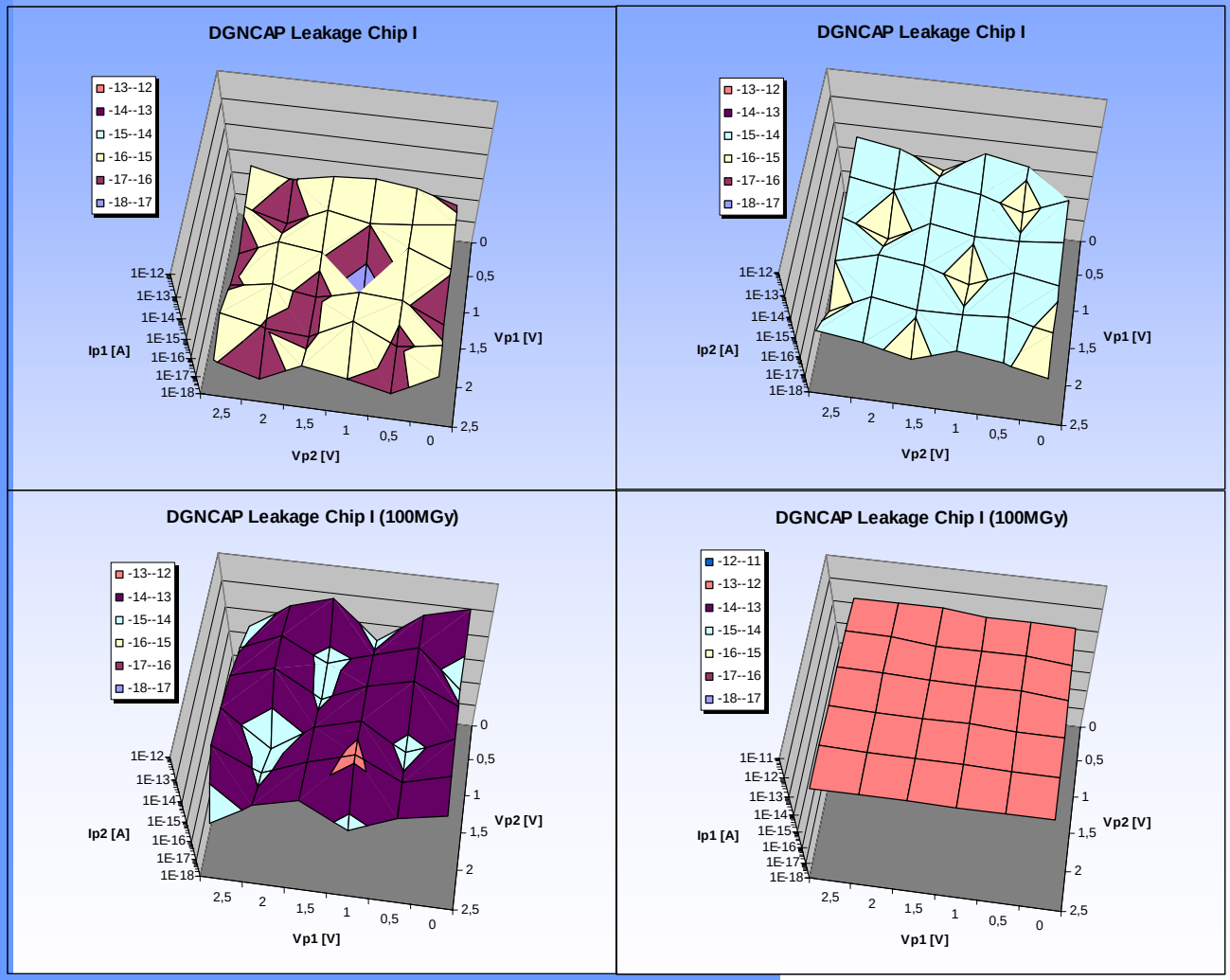
Outline

- Characterisation of
  - DGNCAP, MIMCAP & DMIMCAP capacitors
  - DGPMOS, DGNMOS & ZVTDGNMOS FETs
  - Storage Cells and Amps
- At
  - 0Gy, 1MGy, 10MGy and 100MGy
  - -30°C, 20°C and 70°C

Test Campaign

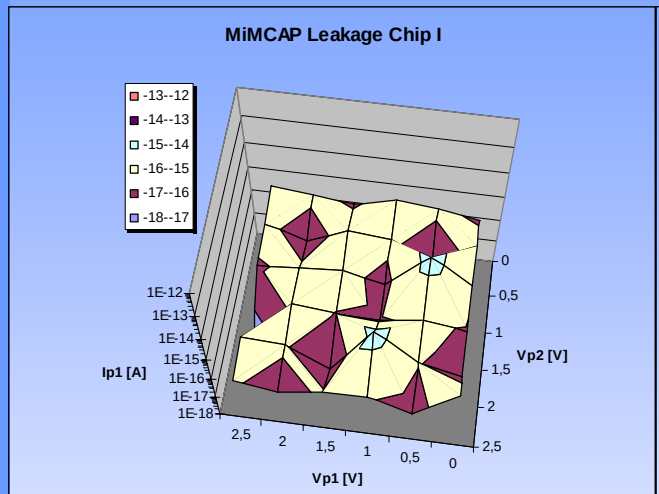
- Test of one HPAD 0.1 chip in a
  - climatic exposure test cabinet at
  - -30°C, 20°C, 70°C
- Irradiation of two HPAD 0.1 chips up to
  - 100MGy
  - @ DORIS F4 with
  - 5.4kGy/s from
  - 16.-21.12.2008
- Test with an HP4156A semiconductor parameter tester

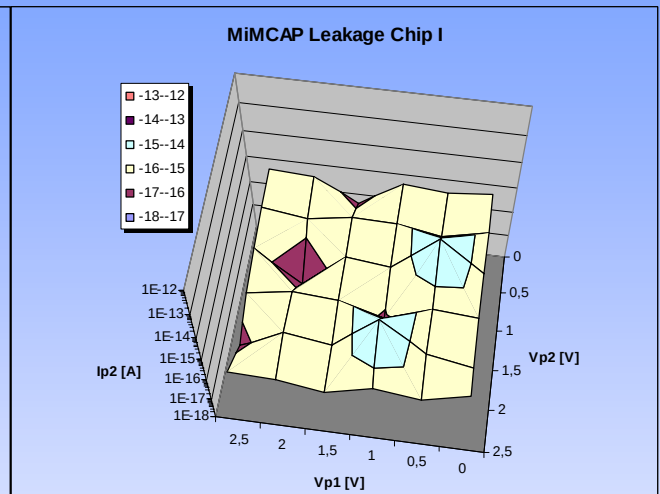
DGNCAP Capacitors

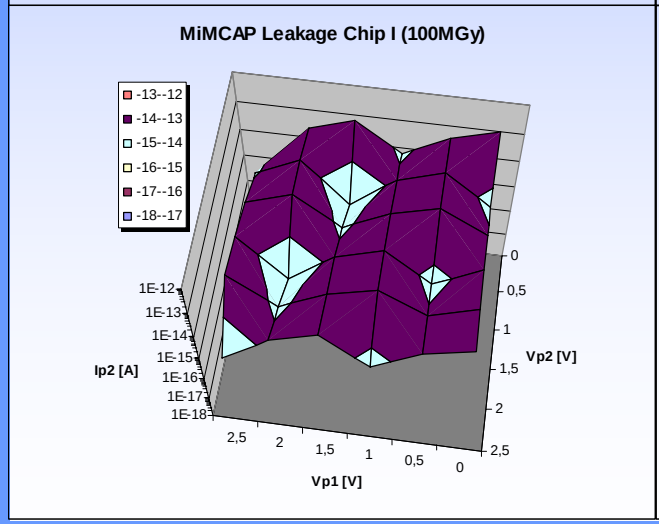


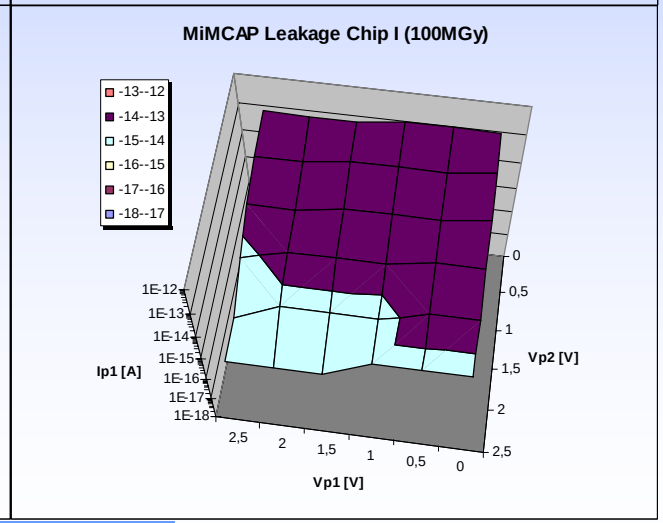
- Left: poly plate
  - o(10^{-16}A) @0Gy
  - o(10^{-14}A) @100MGy
- Right: diffusion plate
  - o(10^{-15}A) @0Gy
  - o(10^{-13}A) @100MGy

MIMCAP Capacitors



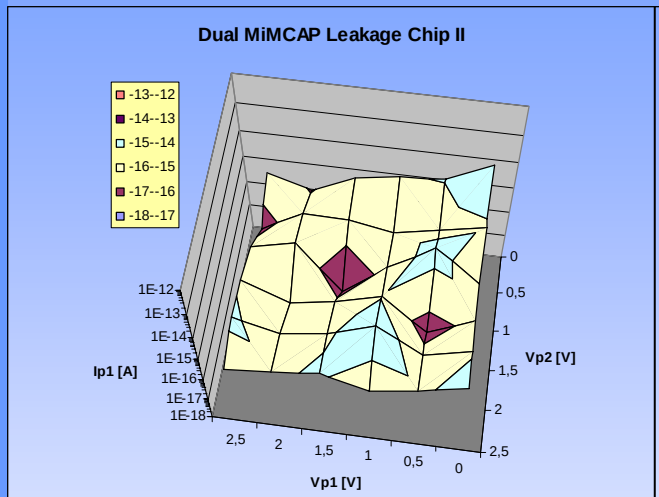


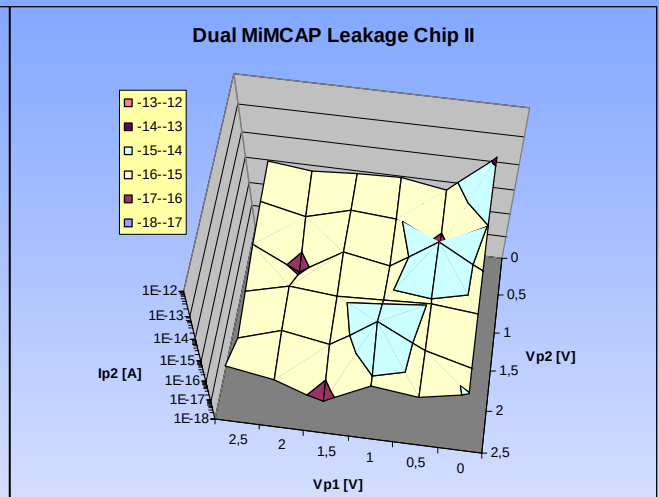


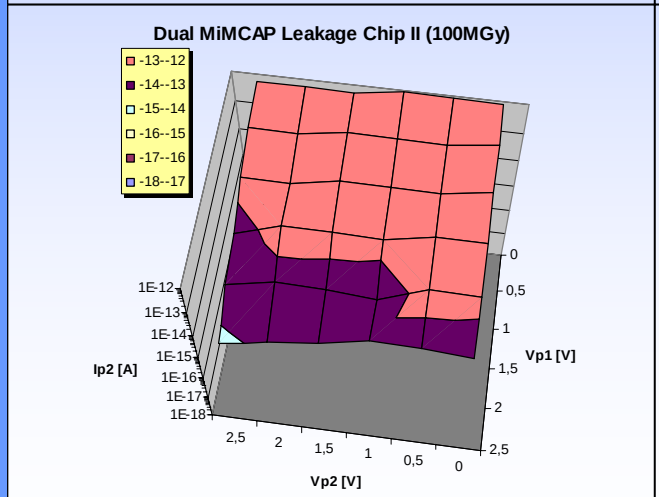


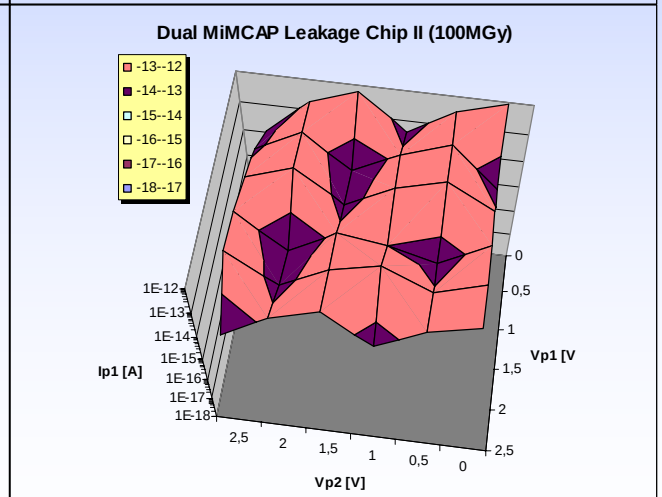
- o(10^{-16}A) @0Gy
- o(10^{-14}A) @100MGy

DualMIMCAP Capacitors









- o(10^{-16}A) @0Gy
- o(10^{-13}A) @100MGy

Capacitors-Summary

- Increase of leakage by ~10^2 for all caps
- Dependency of leakage from node voltage
- No correlation of Leakage with plate-plate voltage
- DGNCAP leakage dependent on diffusion area

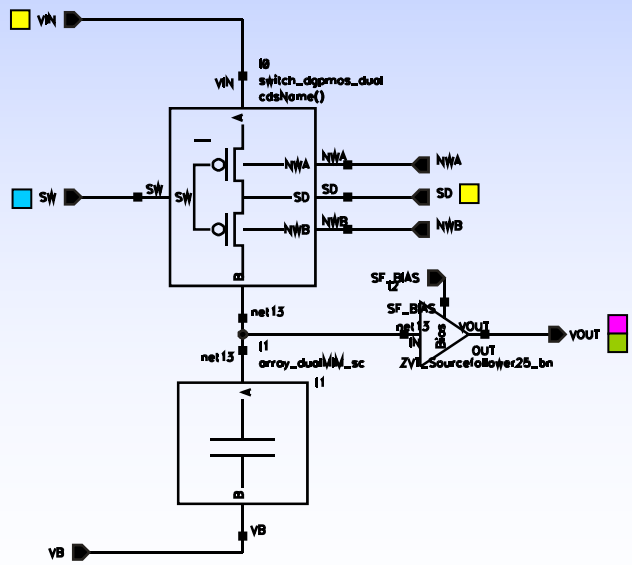
=> P-N junction leakage dominated

- Theory: no mechanism for radiation induced oxide leakage

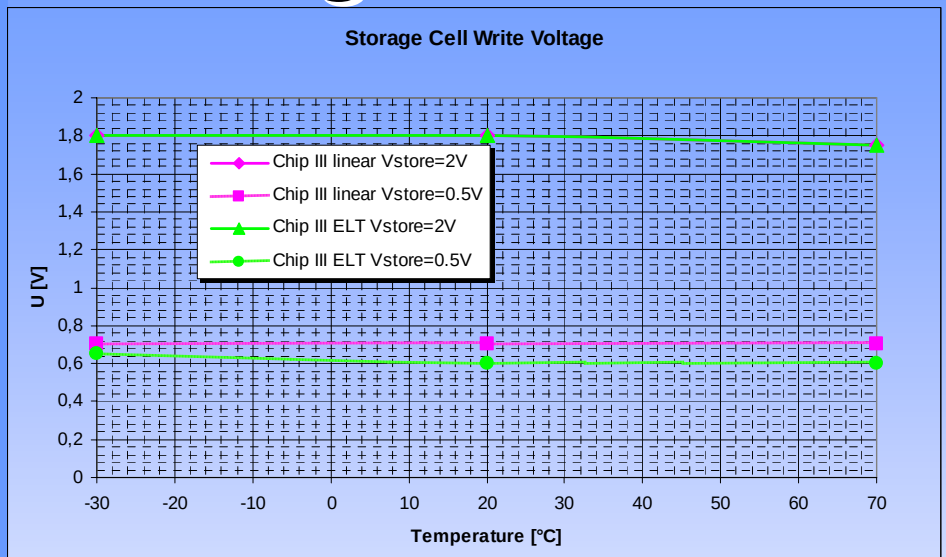
Storage Cell

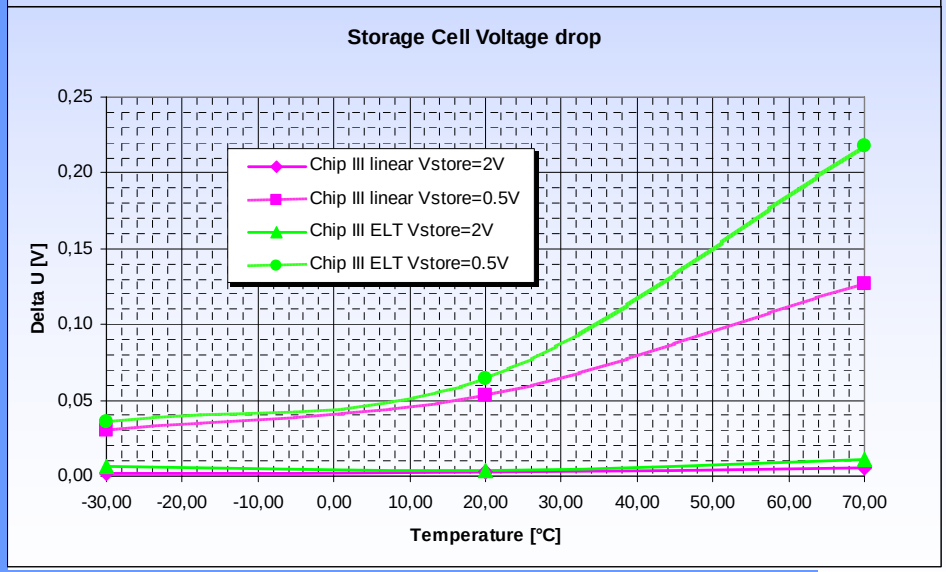
- Double DGPMOS switch
- DMIM storage capacitor
- ZVTDGNMOS source follower readout

Pattern:
- Write (0.08Hz)
- Read (cont.)
- Measure voltage drop over 10s



Storage Cell





Thermal Efffects

Linear DGPMOS:

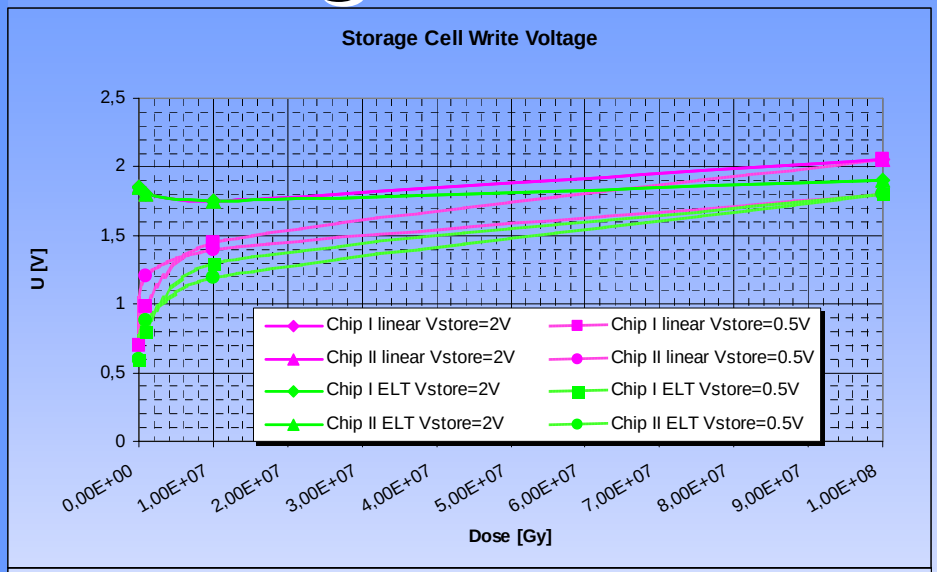
- Higher on-resistance

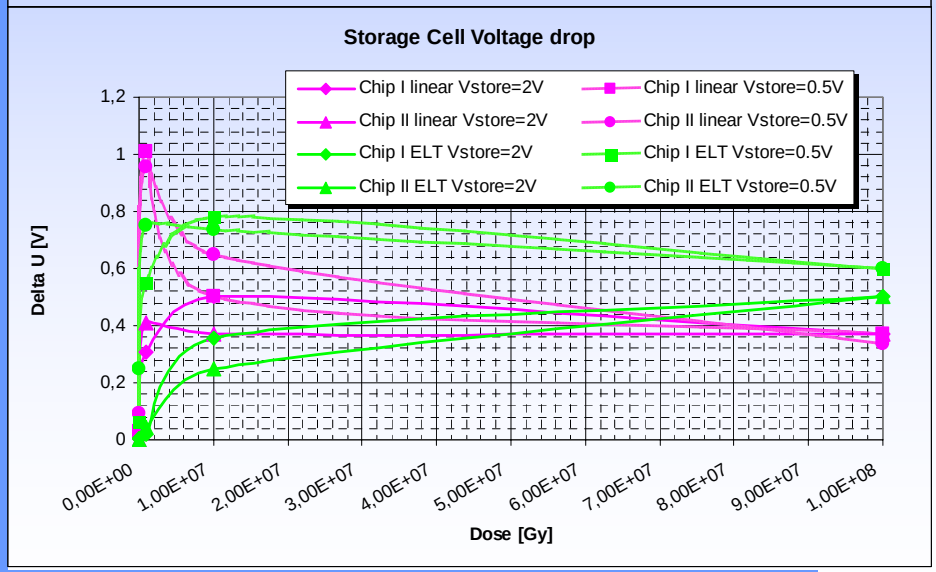
Enclosed DGPMOS

- Higher leakage

- W/L-ratio

Storage Cell

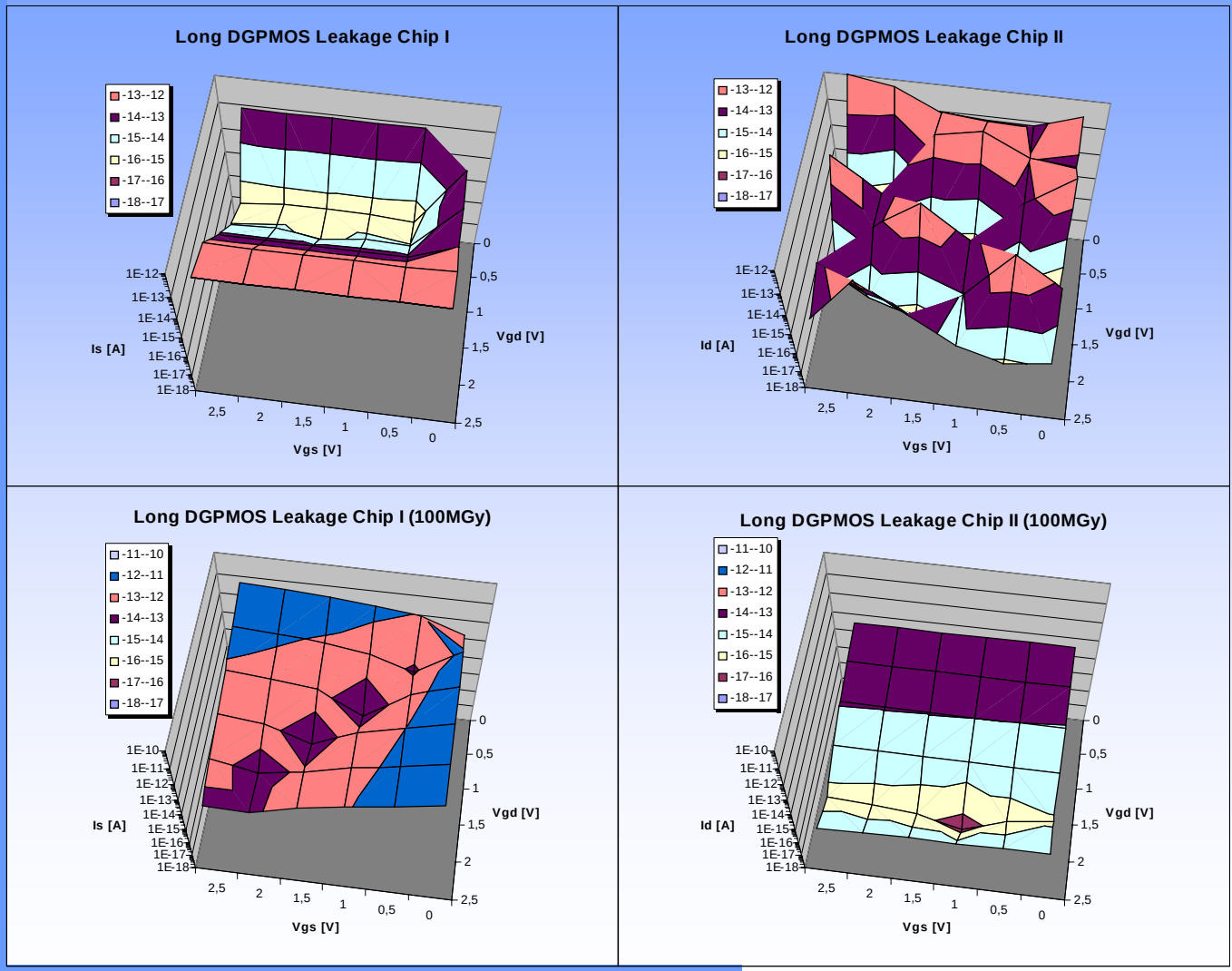




Irradiation Effects

- Circuit dies between 1MGy and 10MGy due to insufficient write voltage
- Enclosed layout favourable due to lower leakage
- ZVTDGNMOS source follower still working perfectly after 100MGy!

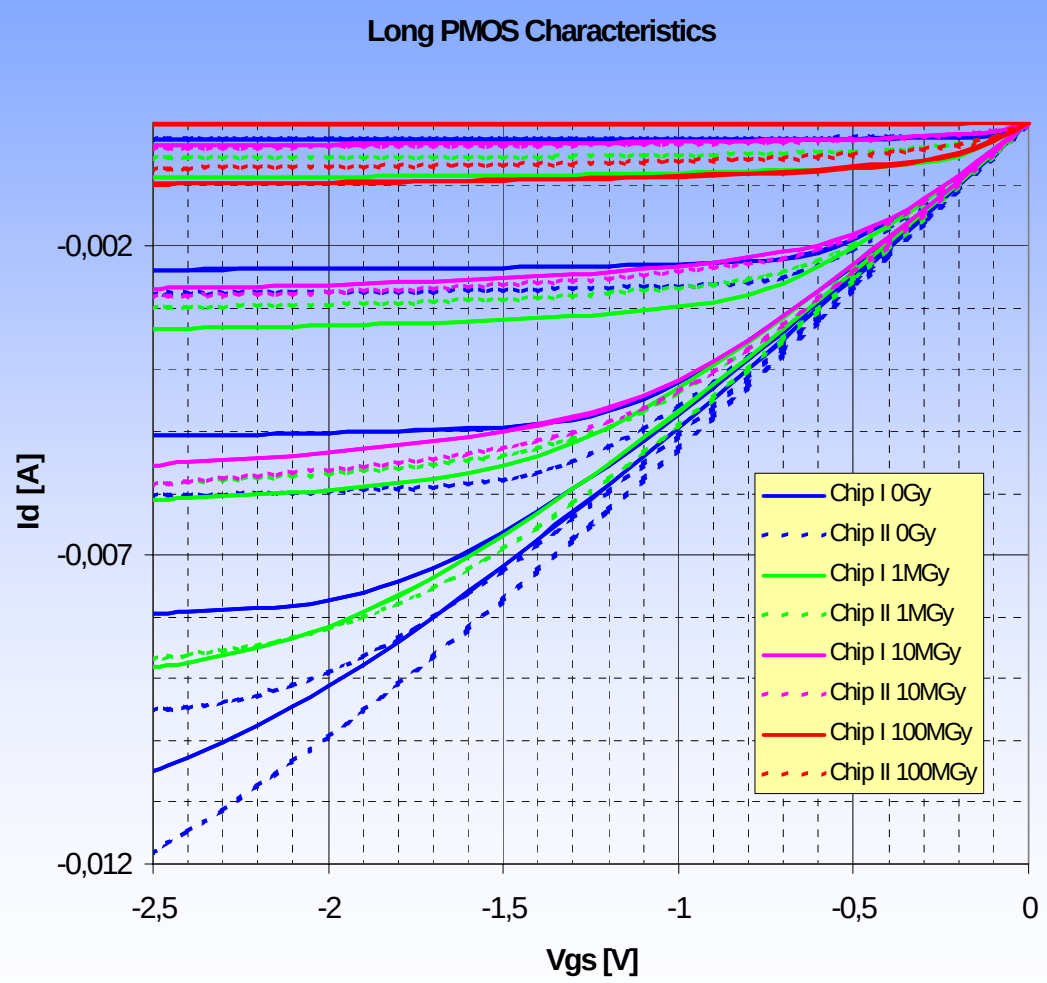
DGPMOS

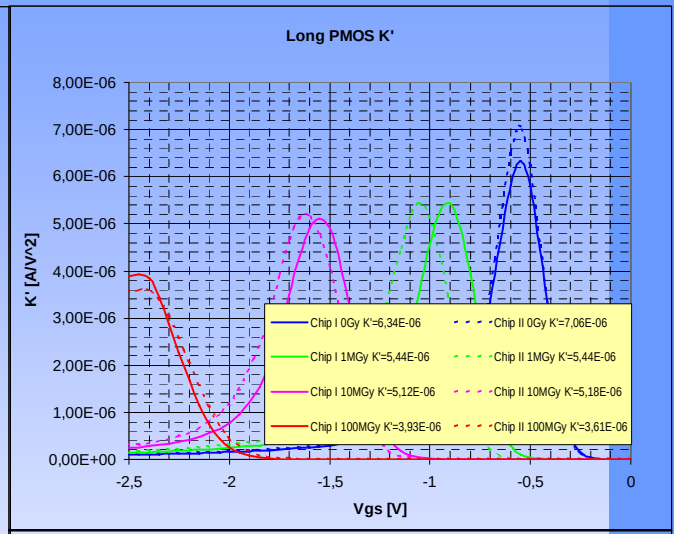


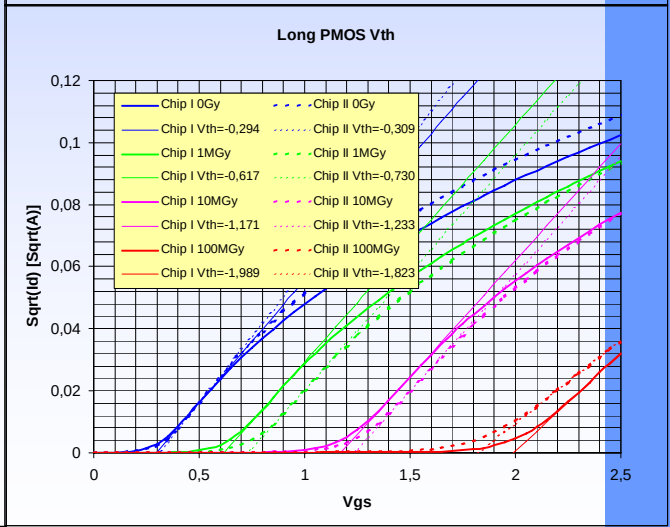
Irradiation Effects

- Reproducibly
- Inconsistent
- Results

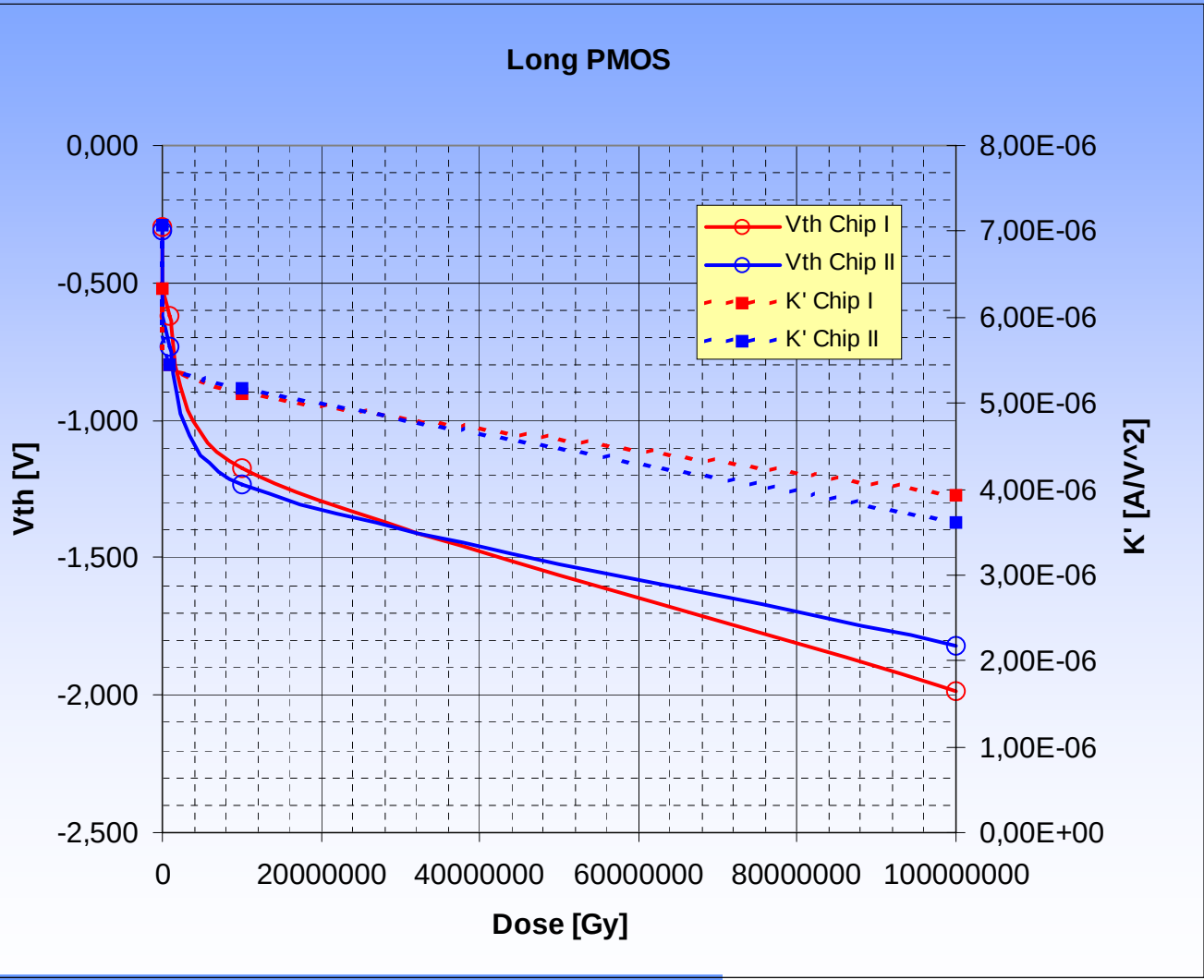
DGPMOS


Long PMOS Characteristics
Id [A]
-0,002
-0,007
-0,012
-2,5
-2
-1,5
-1
-0,5
0
Vgs [V]
Chip I 0Gy
Chip II 0Gy
Chip I 1MGy
Chip II 1MGy
Chip I 10MGy
Chip II 10MGy
Chip I 100MGy
Chip II 100MGy


Long PMOS K'
K' [A/V^2]
8,00E-06
7,00E-06
6,00E-06
5,00E-06
4,00E-06
3,00E-06
2,00E-06
1,00E-06
0,00E+00
-2,5
-2
-1,5
-1
-0,5
0
Vgs [V]
Chip I 0Gy K'=6,34E-06
Chip II 0Gy K'=7,06E-06
Chip I 1MGy K'=5,44E-06
Chip II 1MGy K'=5,44E-06
Chip I 10MGy K'=5,12E-06
Chip II 10MGy K'=5,18E-06
Chip I 100MGy K'=3,93E-06
Chip II 100MGy K'=3,61E-06


Long PMOS Vth
Sqrt(Id) [Sqrt(A)]
0,12
0,1
0,08
0,06
0,04
0,02
0
0
0,5
1
1,5
2
2,5
Vgs
Chip I 0Gy
Chip II 0Gy
Chip I Vth=-0,294
Chip II Vth=-0,309
Chip I 1MGy
Chip II 1MGy
Chip I Vth=-0,617
Chip II Vth=-0,730
Chip I 10MGy
Chip II 10MGy
Chip I Vth=-1,171
Chip II Vth=-1,233
Chip I 100MGy
Chip II 100MGy
Chip I Vth=-1,989
Chip II Vth=-1,823

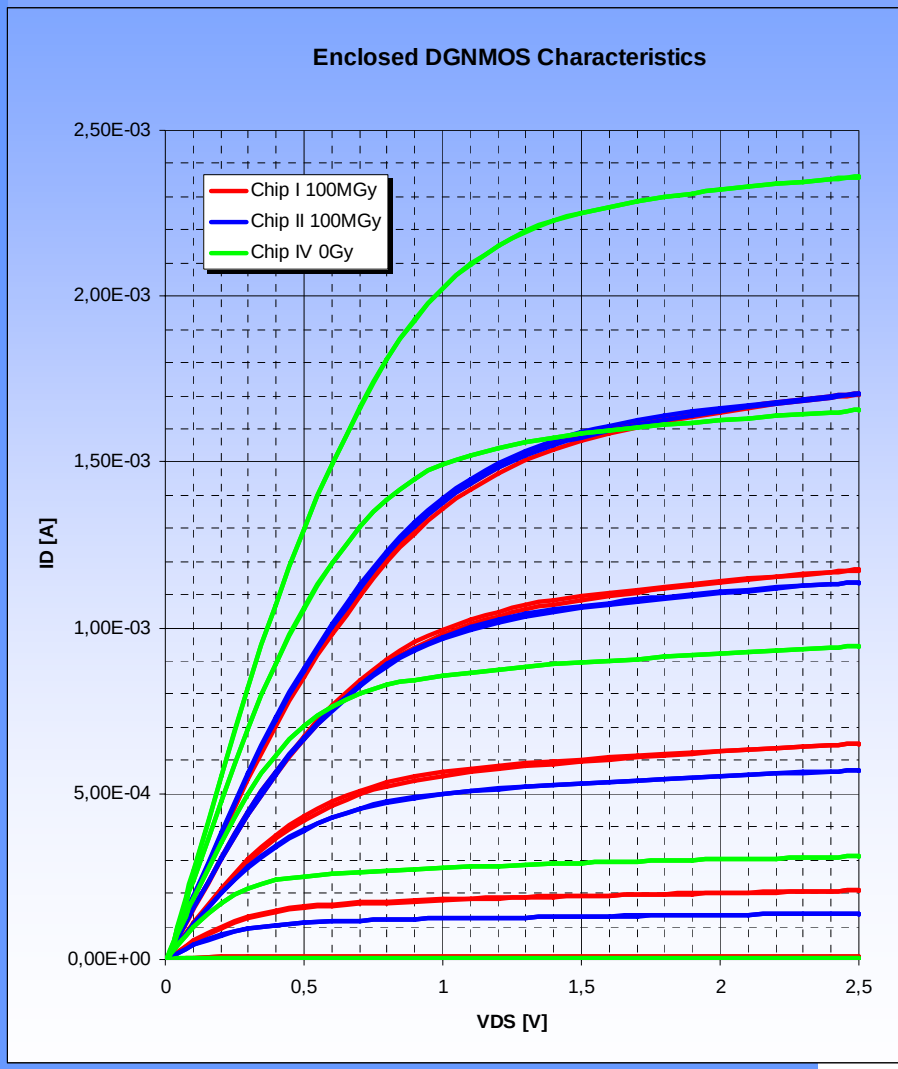
DGPMOS

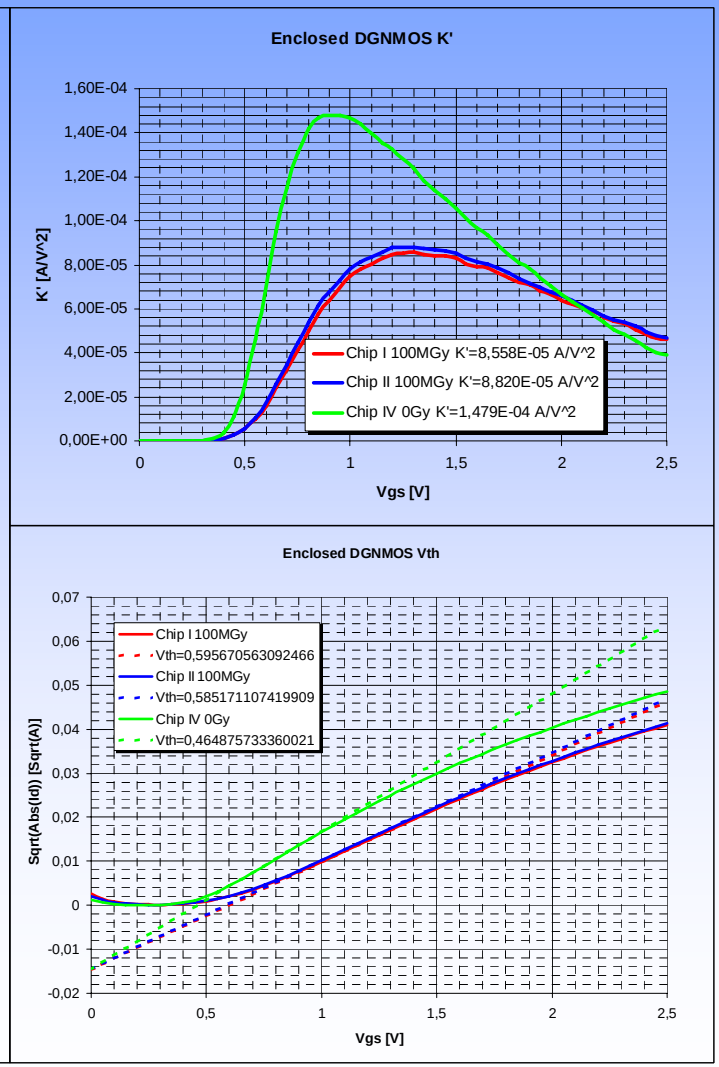


Irradiation Effects

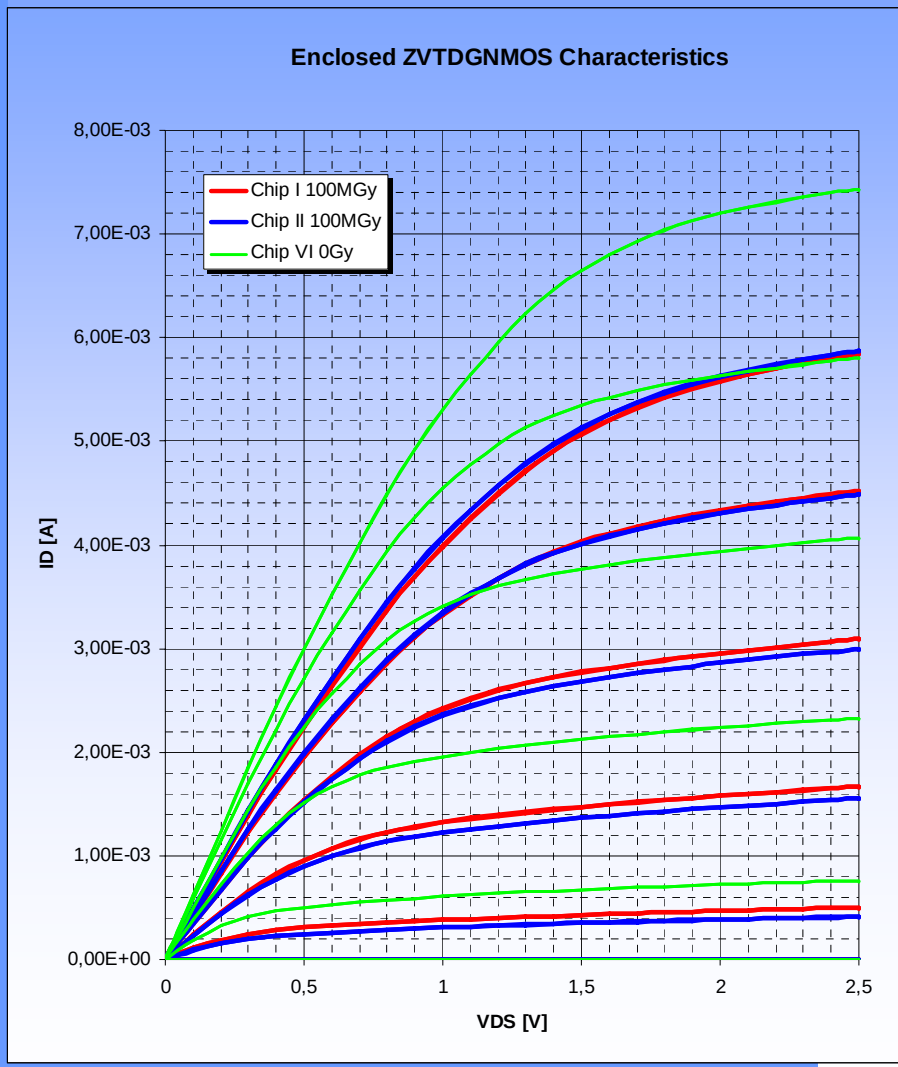
- *K'* almost halves
- V_{th} rises to almost -2V @ 100MGy

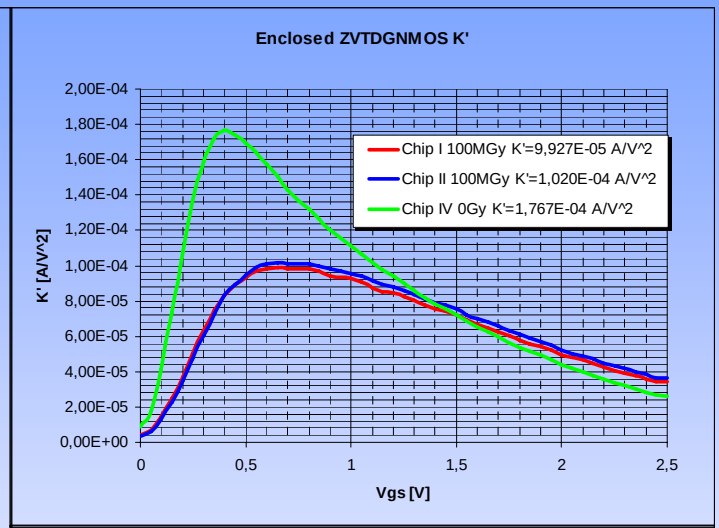
DGNMOS

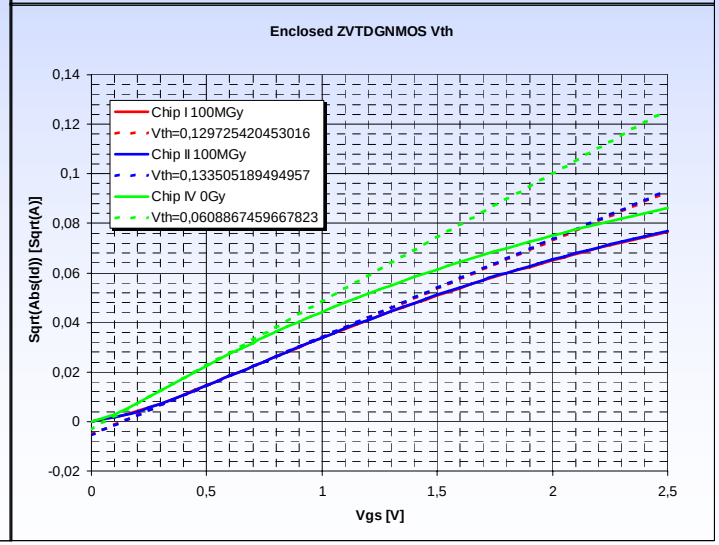

Enclosed DGNMOS Characteristics
Chip I 100MGy
Chip II 100MGy
Chip IV 0Gy
ID [A]
VDS [V]
2,50E-03
2,00E-03
1,50E-03
1,00E-03
5,00E-04
0,00E+00
0
0,5
1
1,5
2
2,5


Enclosed DGNMOS K'
K' [A/V^2]
Vgs [V]
Chip I 100MGy K'=8,558E-05 A/V^2
Chip II 100MGy K'=8,820E-05 A/V^2
Chip IV 0Gy K'=1,479E-04 A/V^2
1,60E-04
1,40E-04
1,20E-04
1,00E-04
8,00E-05
6,00E-05
4,00E-05
2,00E-05
0,00E+00
0
0,5
1
1,5
2
2,5
Enclosed DGNMOS Vth
Sqrt(Abs(Id)) [Sqrt(A)]
Vgs [V]
Chip I 100MGy
Vth=0,595670563092466
Chip II 100MGy
Vth=0,585171107419909
Chip IV 0Gy
Vth=0,464875733360021
0,07
0,06
0,05
0,04
0,03
0,02
0,01
0
-0,01
-0,02
0
0,5
1
1,5
2
2,5

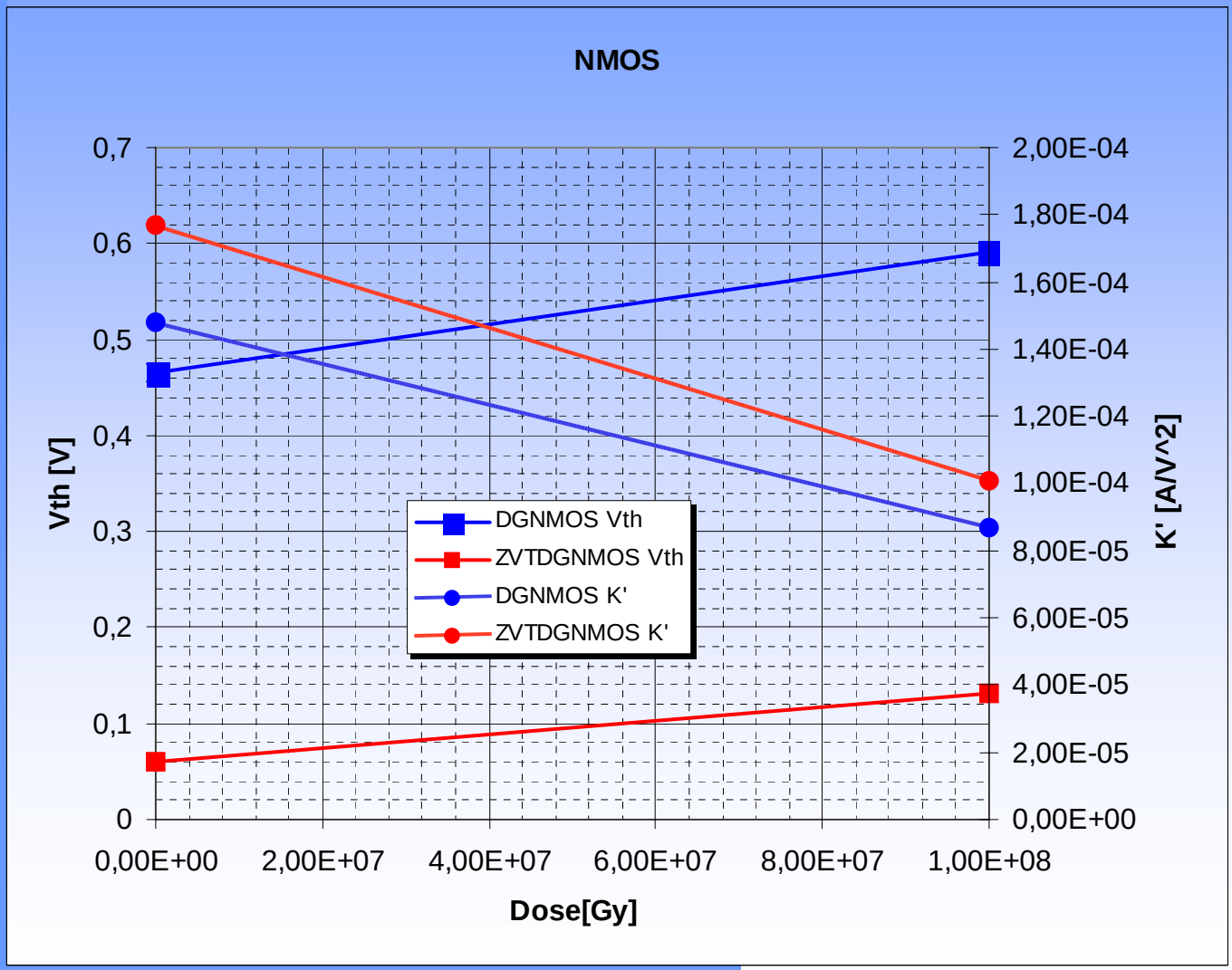
ZVTDGNMOS


Enclosed ZVTDGNMOS Characteristics
ID [A]
VDS [V]
Chip I 100MGy
Chip II 100MGy
Chip VI 0Gy
8,00E-03
7,00E-03
6,00E-03
5,00E-03
4,00E-03
3,00E-03
2,00E-03
1,00E-03
0,00E+00
0
0,5
1
1,5
2
2,5


Enclosed ZVTDGNMOS K'
K' [A/V^2]
Vgs [V]
Chip I 100MGy K'=9,927E-05 A/V^2
Chip II 100MGy K'=1,020E-04 A/V^2
Chip IV 0Gy K'=1,767E-04 A/V^2
2,00E-04
1,80E-04
1,60E-04
1,40E-04
1,20E-04
1,00E-04
8,00E-05
6,00E-05
4,00E-05
2,00E-05
0,00E+00
0
0,5
1
1,5
2
2,5


Enclosed ZVTDGNMOS Vth
Sqrt(Abs(Id)) [Sqrt(A)]
Vgs [V]
Chip I 100MGy
Vth=0,129725420453016
Chip II 100MGy
Vth=0,133505189494957
Chip IV 0Gy
Vth=0,0608867459667823
0,14
0,12
0,1
0,08
0,06
0,04
0,02
0
-0,02
0
0,5
1
1,5
2
2,5

DGNMOS & ZVTDGNMOS



ZVTDGNMOS

- V_{th} =0.06V @ 0Gy
- V_{th} = 0.13V @ 100MGy
- K'=147µa/V² @ 0Gy
- K'=86.8µa/V² @ 0Gy

DGNMOS

- V_{th} =0.46V @ 0Gy
- V_{th} = 0.59V @ 100MGy
- K'=177µa/V² @ 0Gy
- K'=100µa/V² @ 0Gy

Summary

- Any Cap will do!
  - Results are dominated by P-N junction leakage
  - No known mechanism for radiation-induced oxide leakage
- FETs
  - DGPMOS usable to ≈1MGy(…10MGy)
  - DGNMOS to ≥100MGy
  - ZVTDGNMOS to ≥ 100MGy
- Cooling helps!
  - Cooling from 20°C to –30°C reduces leakage by ≈46%

For details see test report