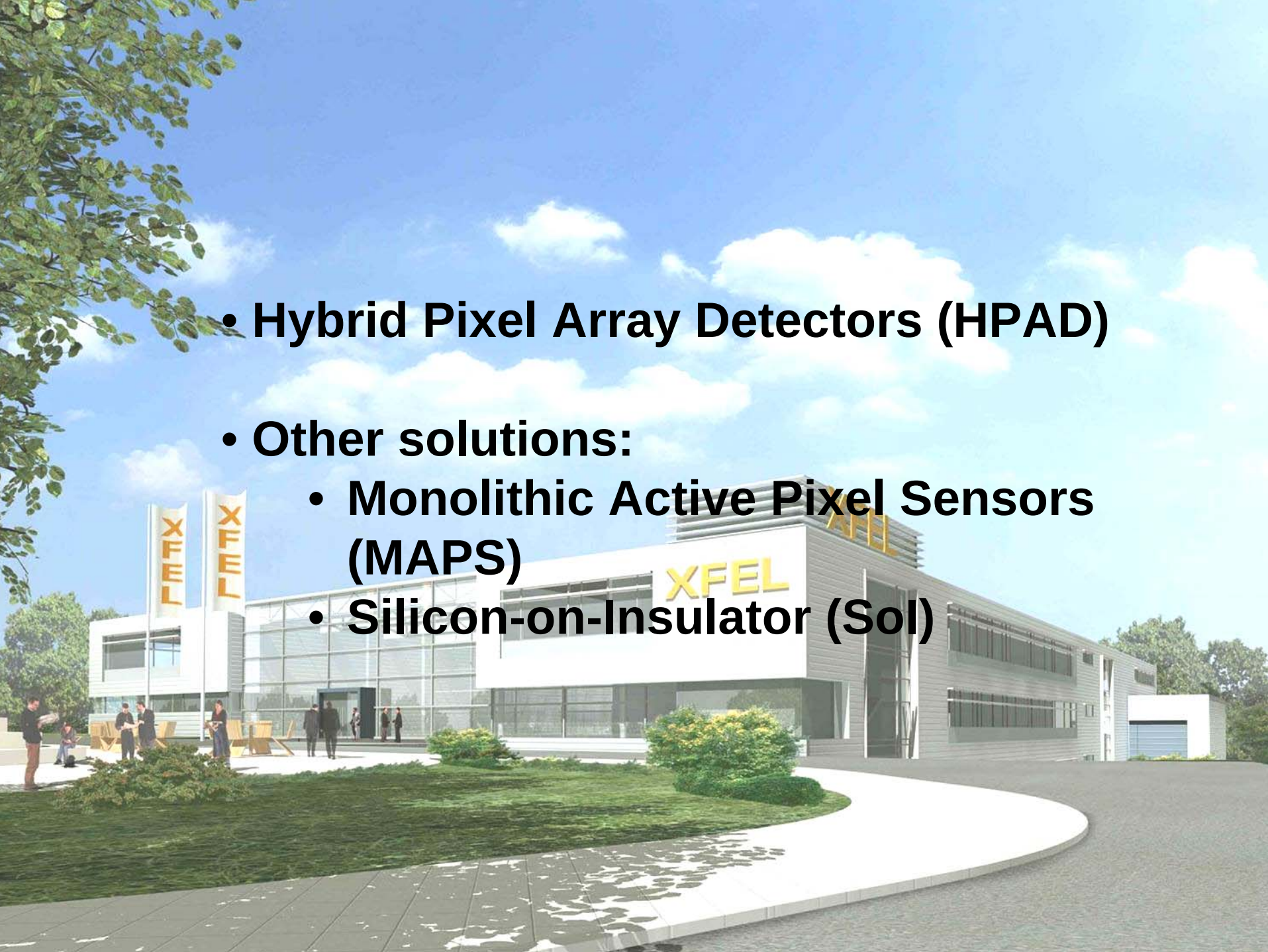
"Future Developments and Challenges of Pixel Detectors"

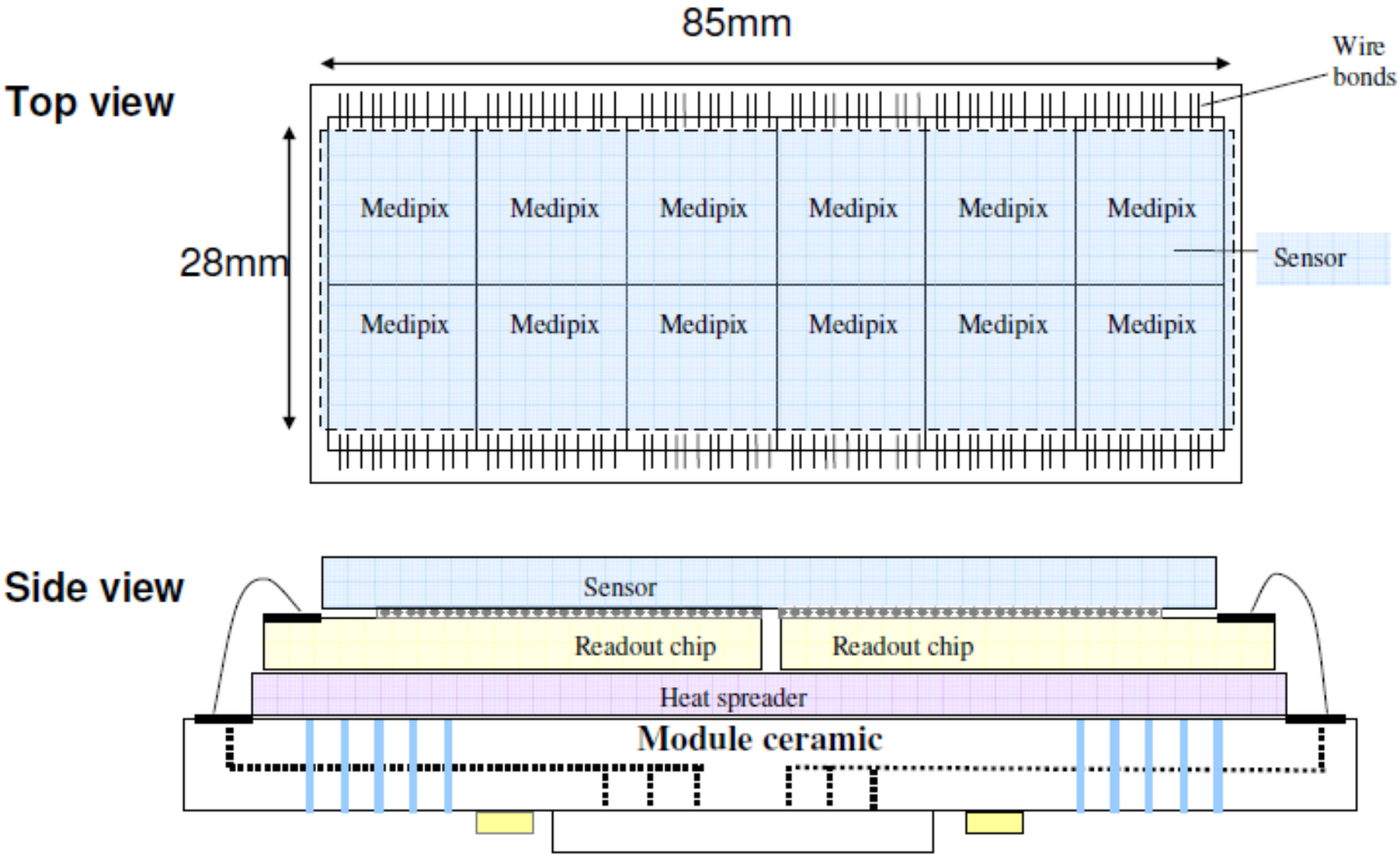
HELMHOLTZ ASSOCIATION

DESY



- **Hybrid Pixel Array Detectors (HPAD)**
- **Other solutions:**
  - **Monolithic Active Pixel Sensors (MAPS)**
  - **Silicon-on-Insulator (Sol)**

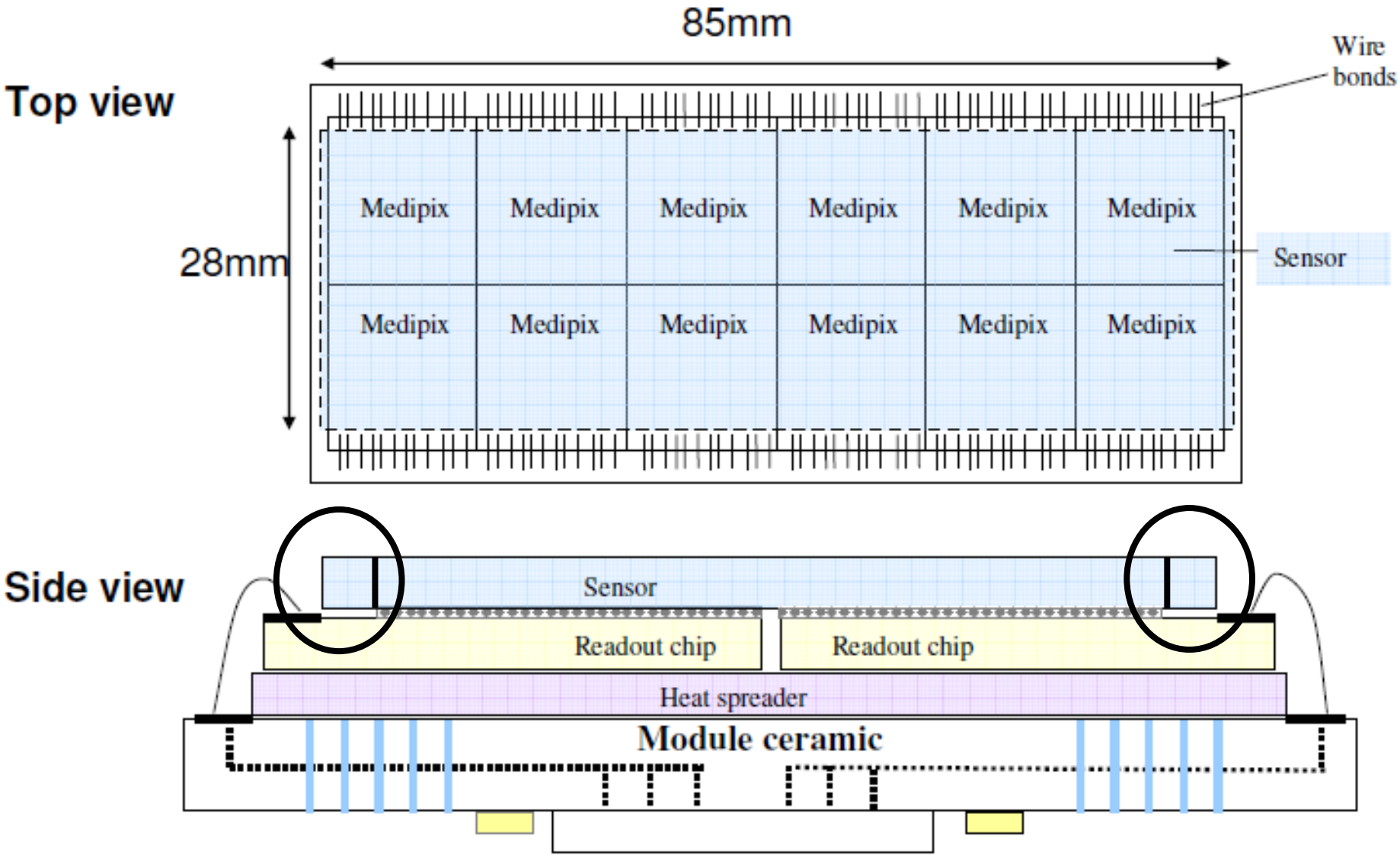
Schematic layout of a Hybrid Pixel Array Detector (HPAD)



Step 1: Sensor

- Current sensors have insensitive areas around the edges (why?) ➔ loss of data.
- Current sensors: simple diodes (why?) ➔ function absorb energy from the particle and create electron-hole pairs.
- Current sensors are made of silicon (why?)
- Could we do better? How?

Schematic layout of a Hybrid Pixel Array Detector (HPAD)

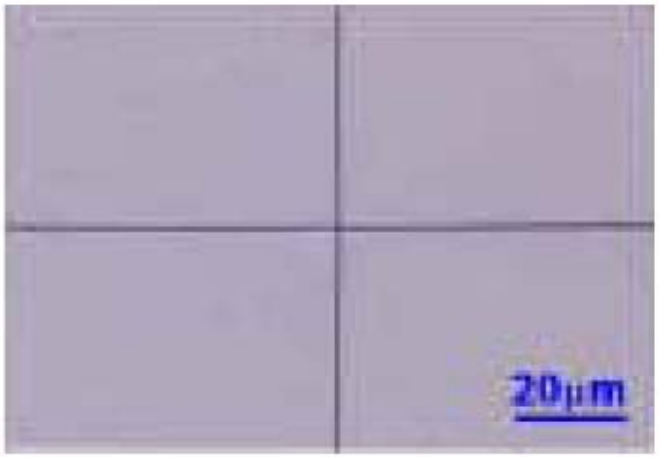


Active edge or stealth dicing

3D active edge

❖ planar detector + dopant diffused in D-RIE etched edge then doped
(C. Kenney 1997).

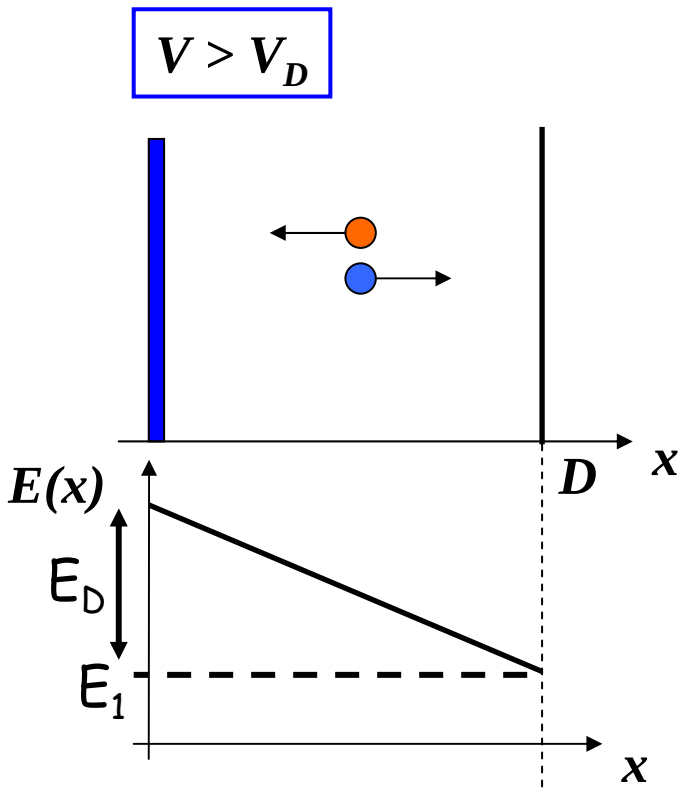
❖ Back plane physically extends at the edge.



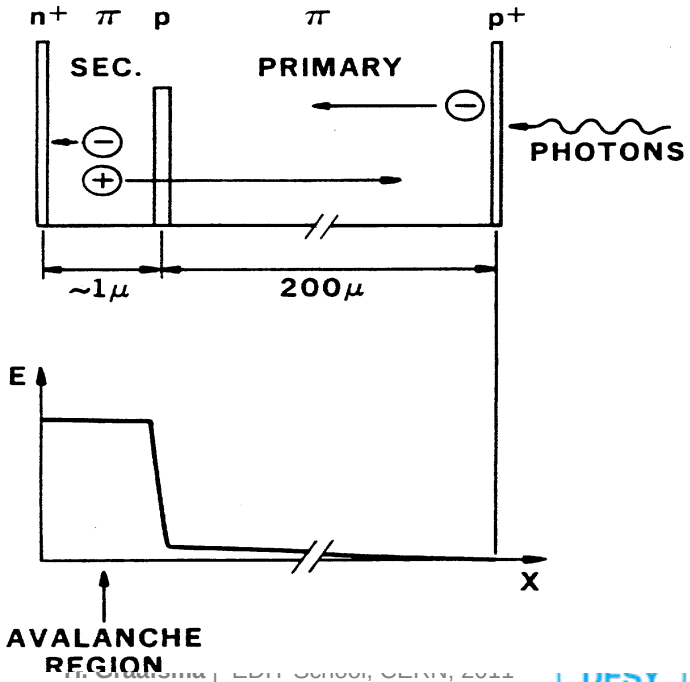
❖ Active volume enclosed by an electrode: “active edge”

Sensors: Active or Smart

1. Increase the signal; amplifying sensors:
   - > Gas filled detectors (GEM foils, MicroMegas, etc.)
   - > Avalanche Photo-Diode arrays and Silicon PMTs



Creation of a particular multiplication zone:



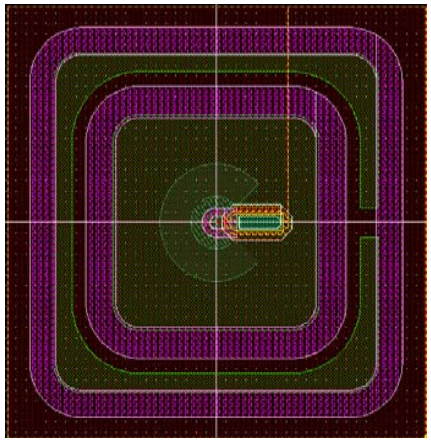
Sensors: Active or Smart

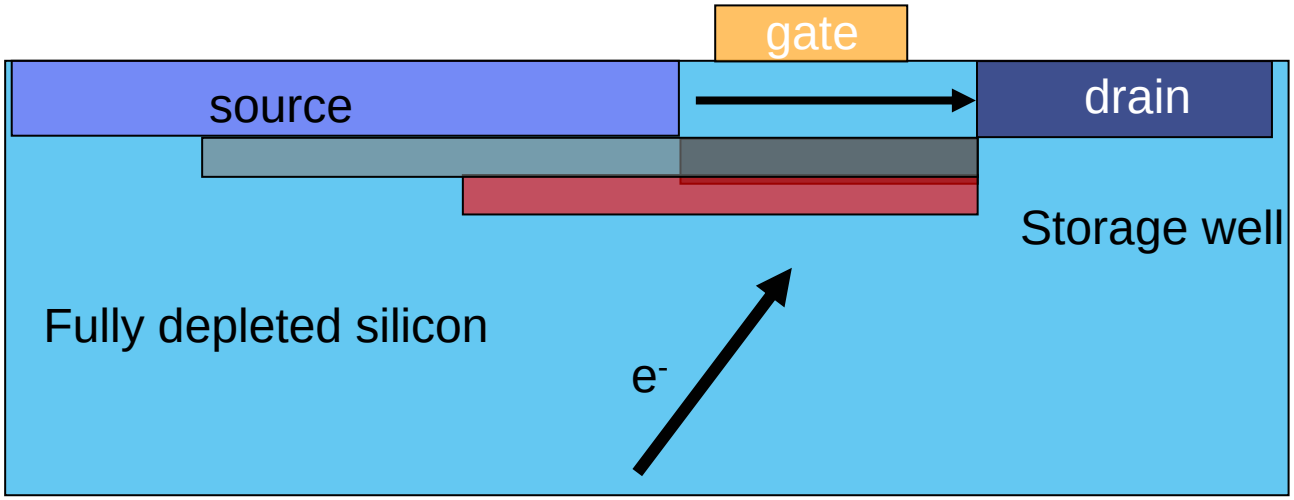
2. Decrease the noise:
   - > Example DEPFET (with signal compression)

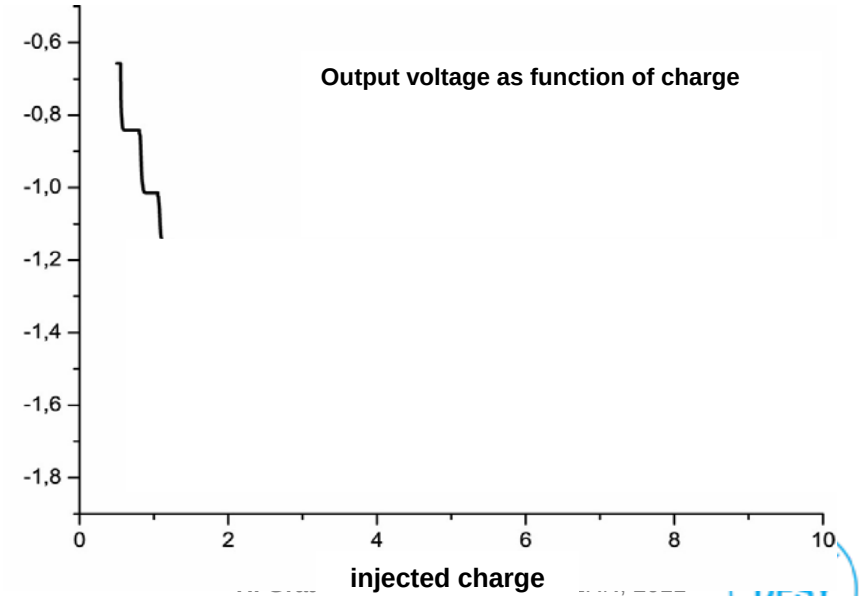
DEPMOS Sensor with Signal Compression

DEPFET: Electrons are collected in a storage well

⇒Influence current from source to drain







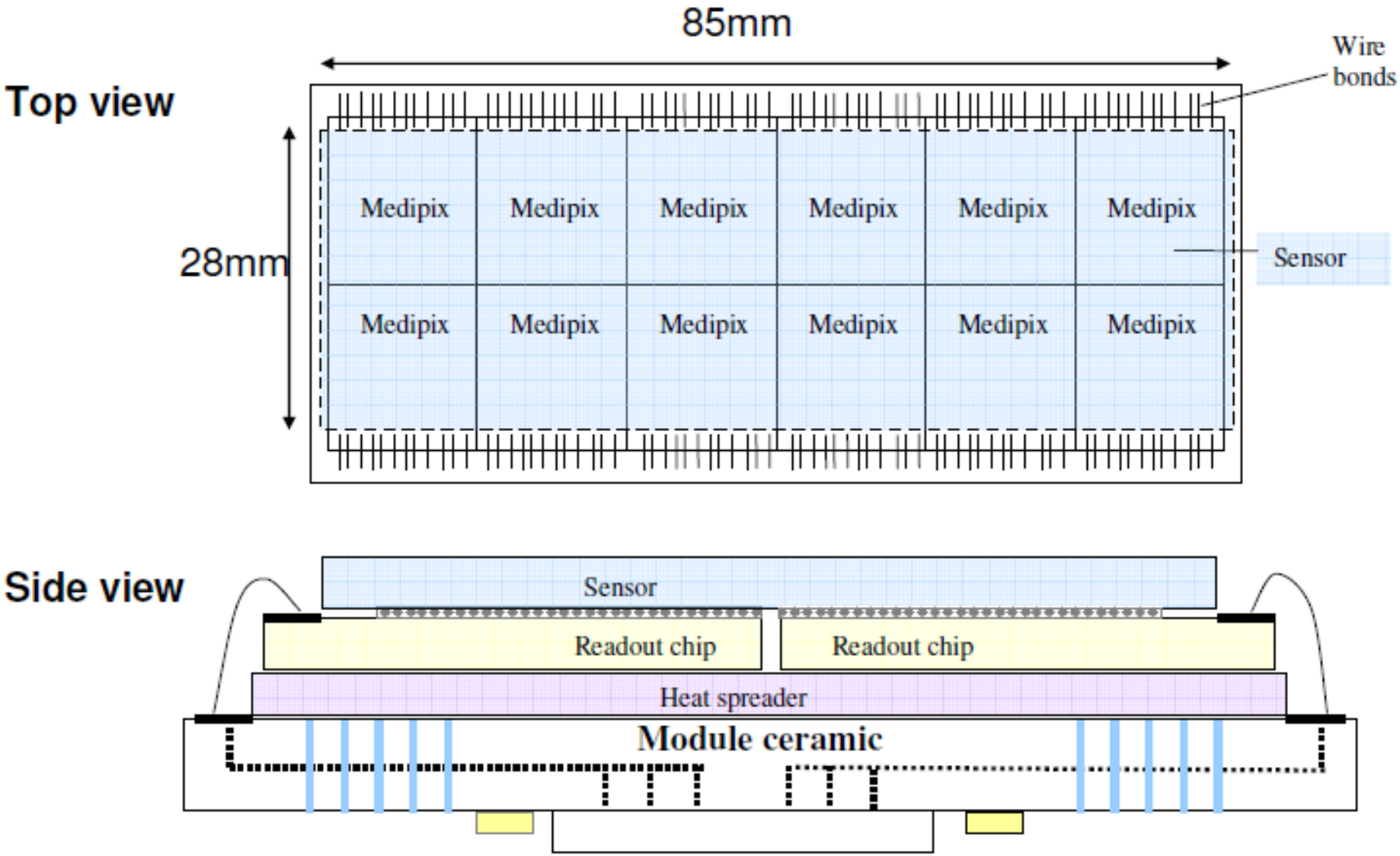
Output voltage as function of charge

injected charge

Summary Sensors

- Silicon is “perfect” material and therefore hard to beat, also large industry behind.
- New sensors with no dead areas around edges (edgeless, or edge-sensitive), or with 3D-structures ➔ no more dead areas.
- New materials:
  - DIAMOND (large bandgap ➔ no need for cooling. Also more radiation hard.
  - High-Z sensors (Cd(Zn)Te; Ge) for photon science (medical)
- Smart sensors: Amplifying for higher signal; or low capacitance for lower noise.

Schematic layout of a Hybrid Pixel Array Detector (HPAD)



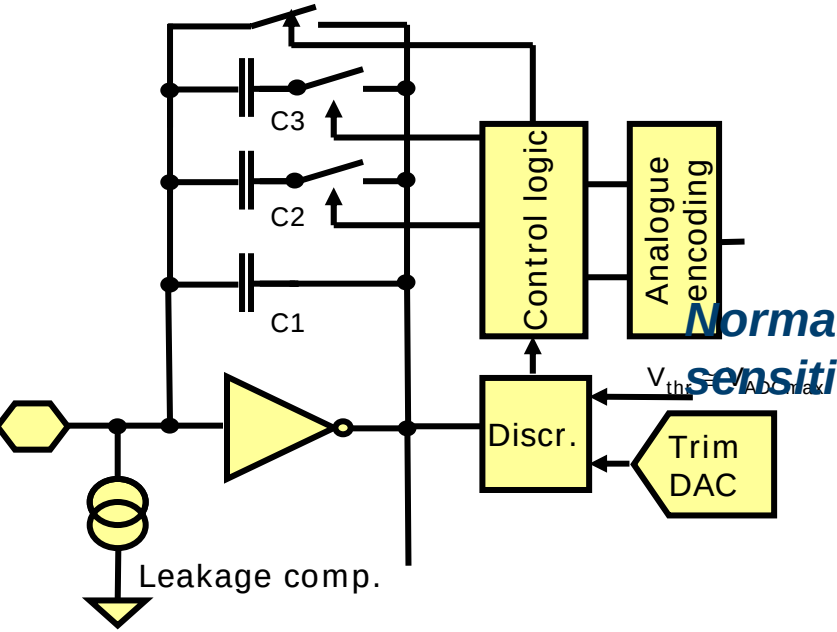
Step 2: Readout ASIC for HPADs

- Most ASICs have limited or no “intelligence” in the pixel.
- Current ASICs treat pixels as independent detectors/channels.
- Conflict between small pixel size and large functionality.
- Conflict between power consumption (=heat production) and speed and functionality.
- Can we do better?

The Adaptive Gain Integrating Pixel Detector

High dynamic range:

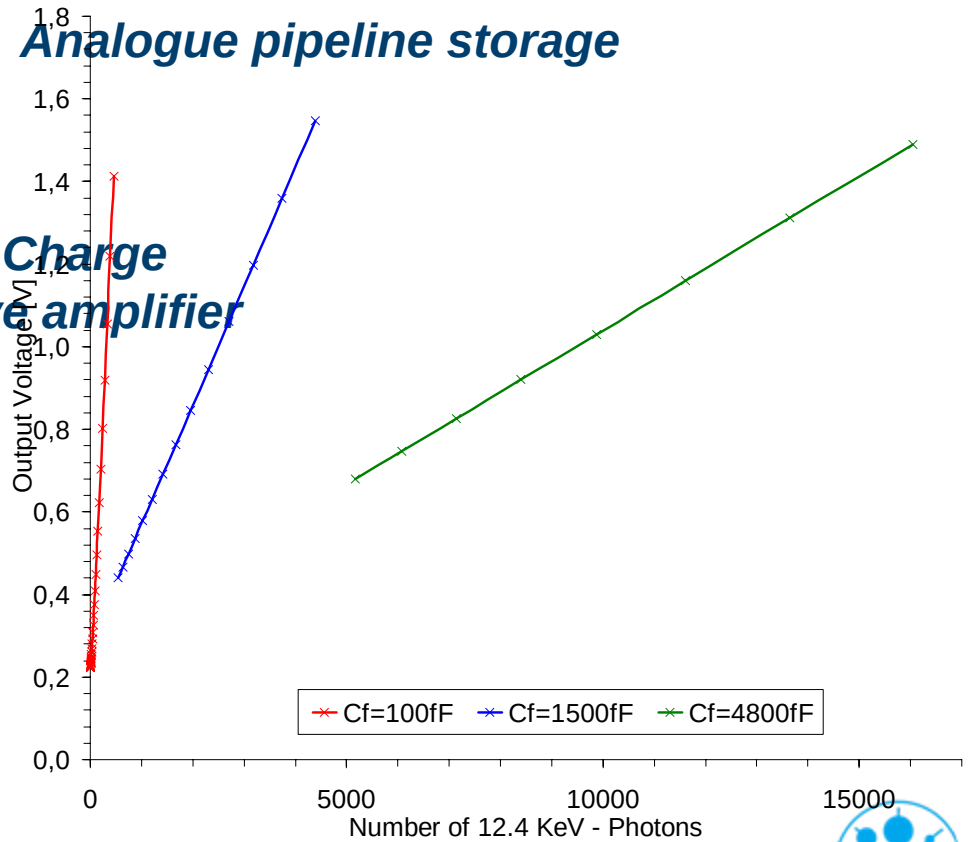
Dynamically gain switching system



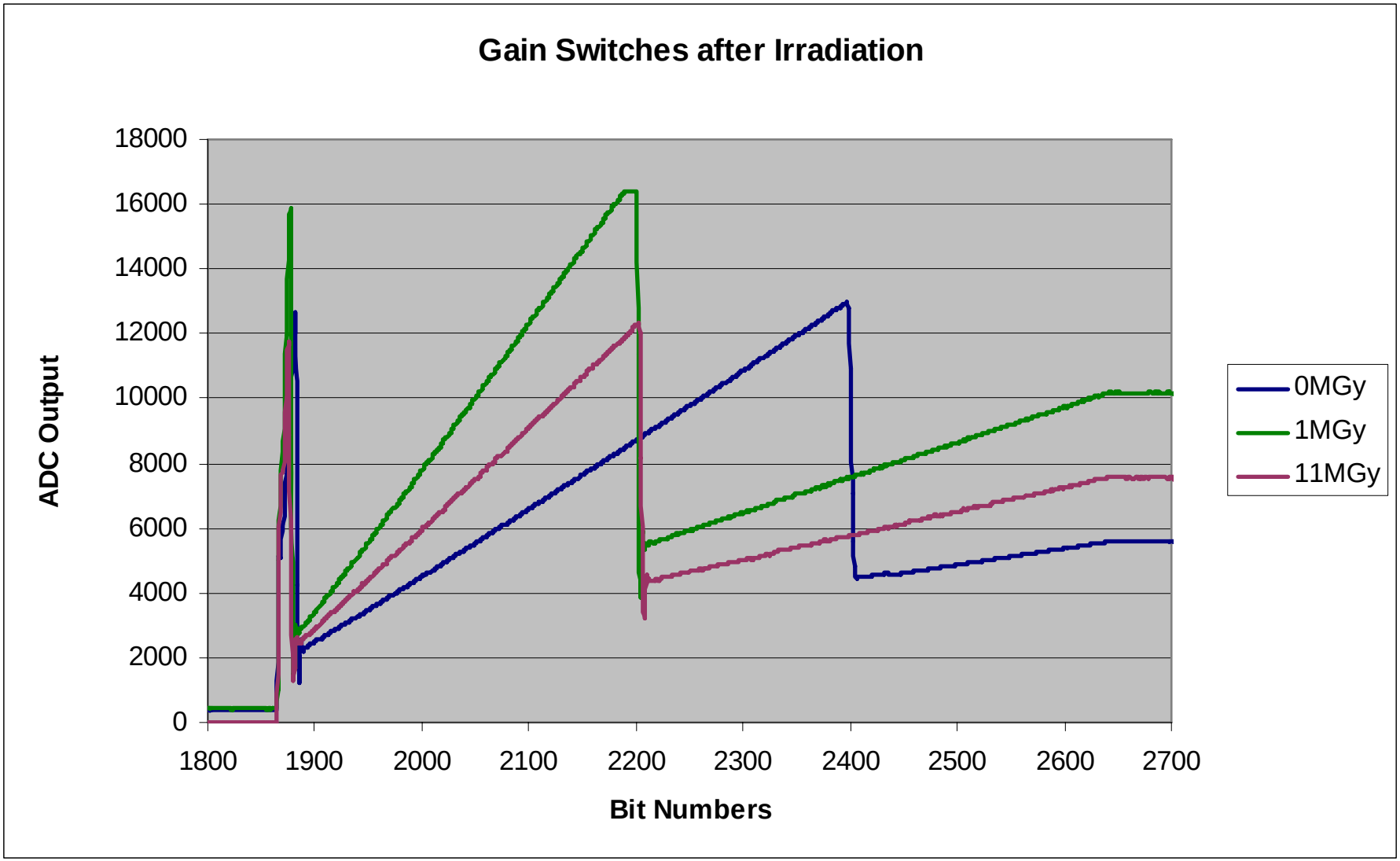
Extremely fast readout (200ns):

Analogue pipeline storage

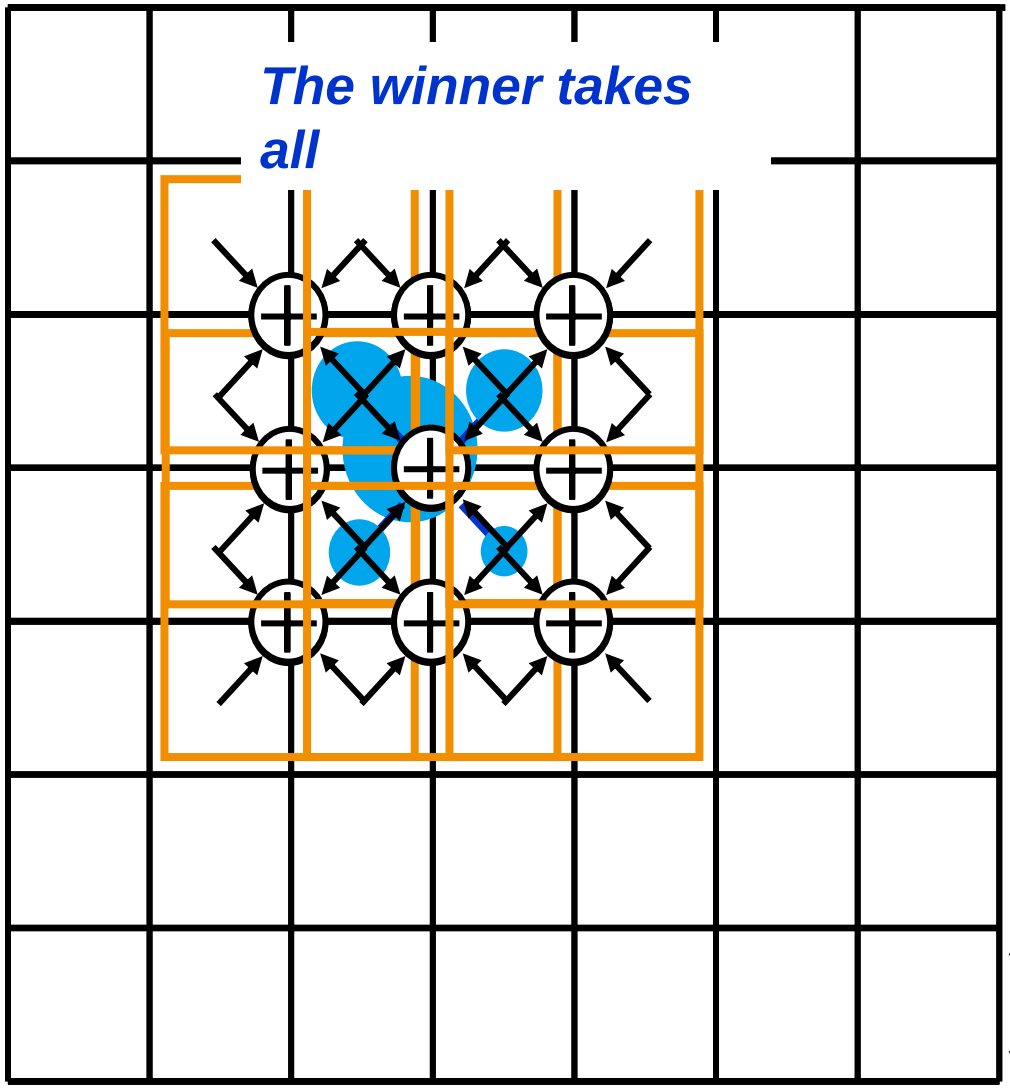
Normal Charge sensitive amplifier



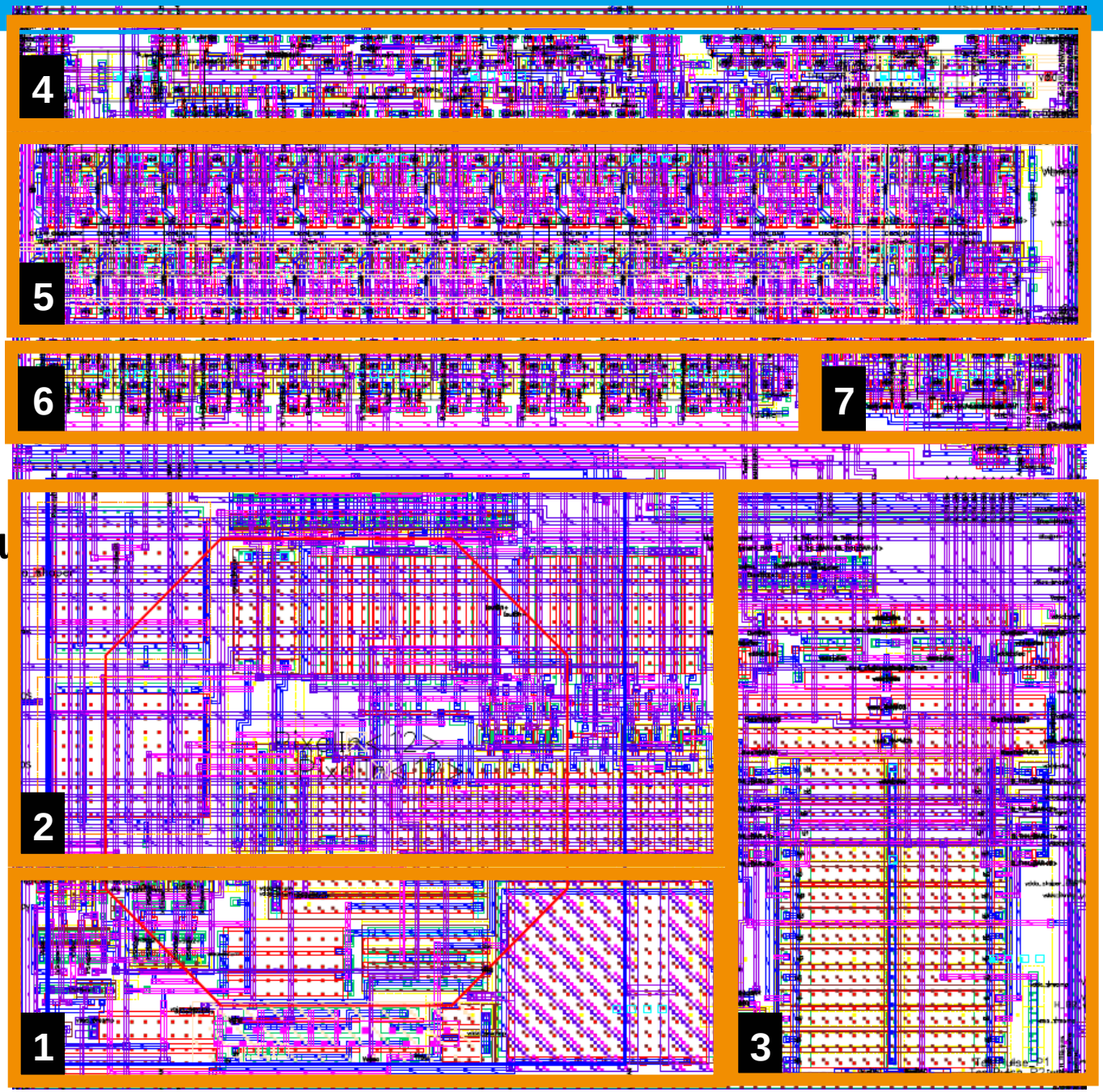
Dynamic Gain Switching works!



Medipix3 – charge summing concept



- *The incoming charge processed is summed in every pixel cluster on an event-by-event basis*
- *The charge is assigned as a single hit*



DIGITAL CIRCUITRY

4. Control logic (124)
5. 2x15bit counters / shift registers (480)
6. Configuration latches (152)
7. Arbitration circuits (100)

Total digital 856

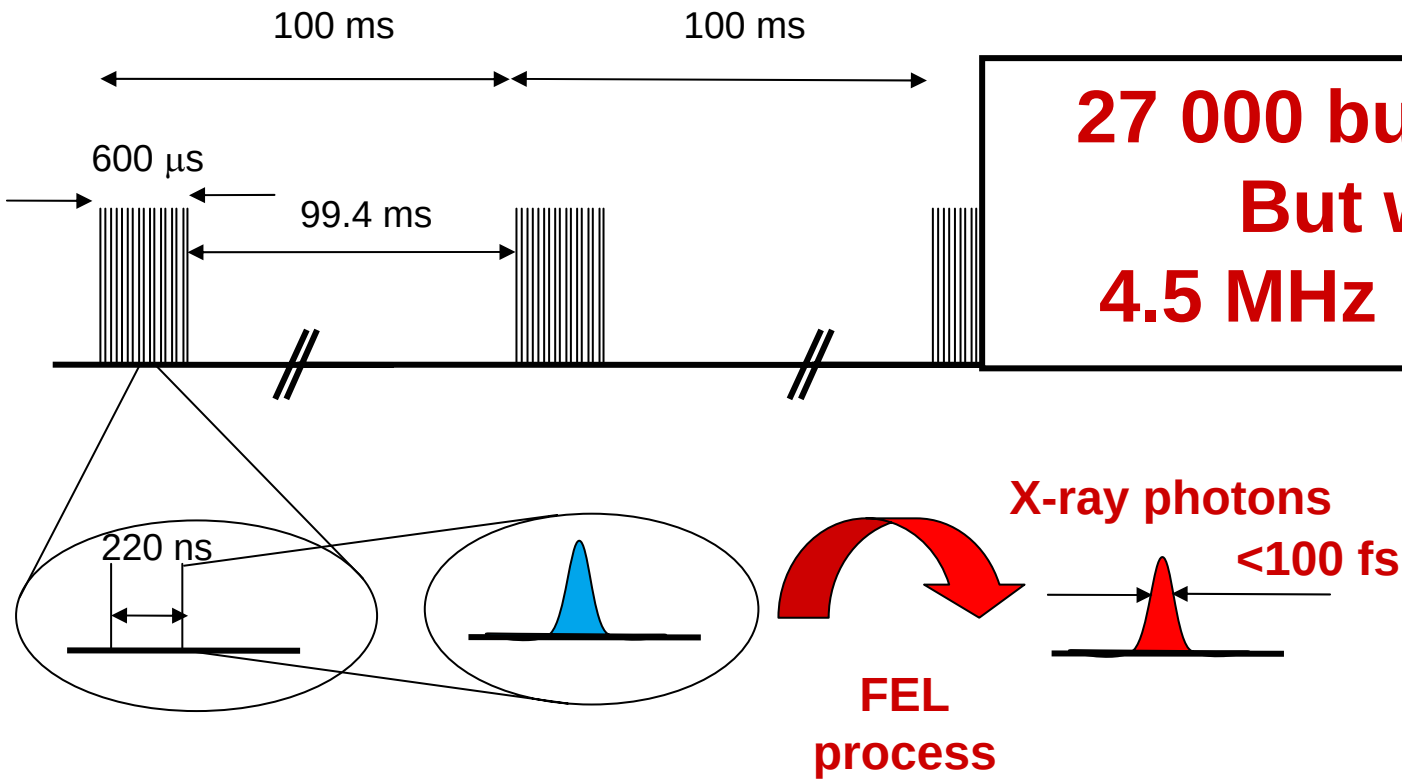
ANALOG CIRCUITRY

1. Preamplifier (24)
2. Shaper (134)
3. Discriminators and Threshold Adjustment Circuits (72)

Total analog 230

E-XFEL Challenge: Time structure = difference with “others”

Electron bunch trains; up to 2700 bunches in 600 μsec, repeated 10 times per second.
Producing 100 fsec X-ray pulses (up to 27 000 bunches per second).



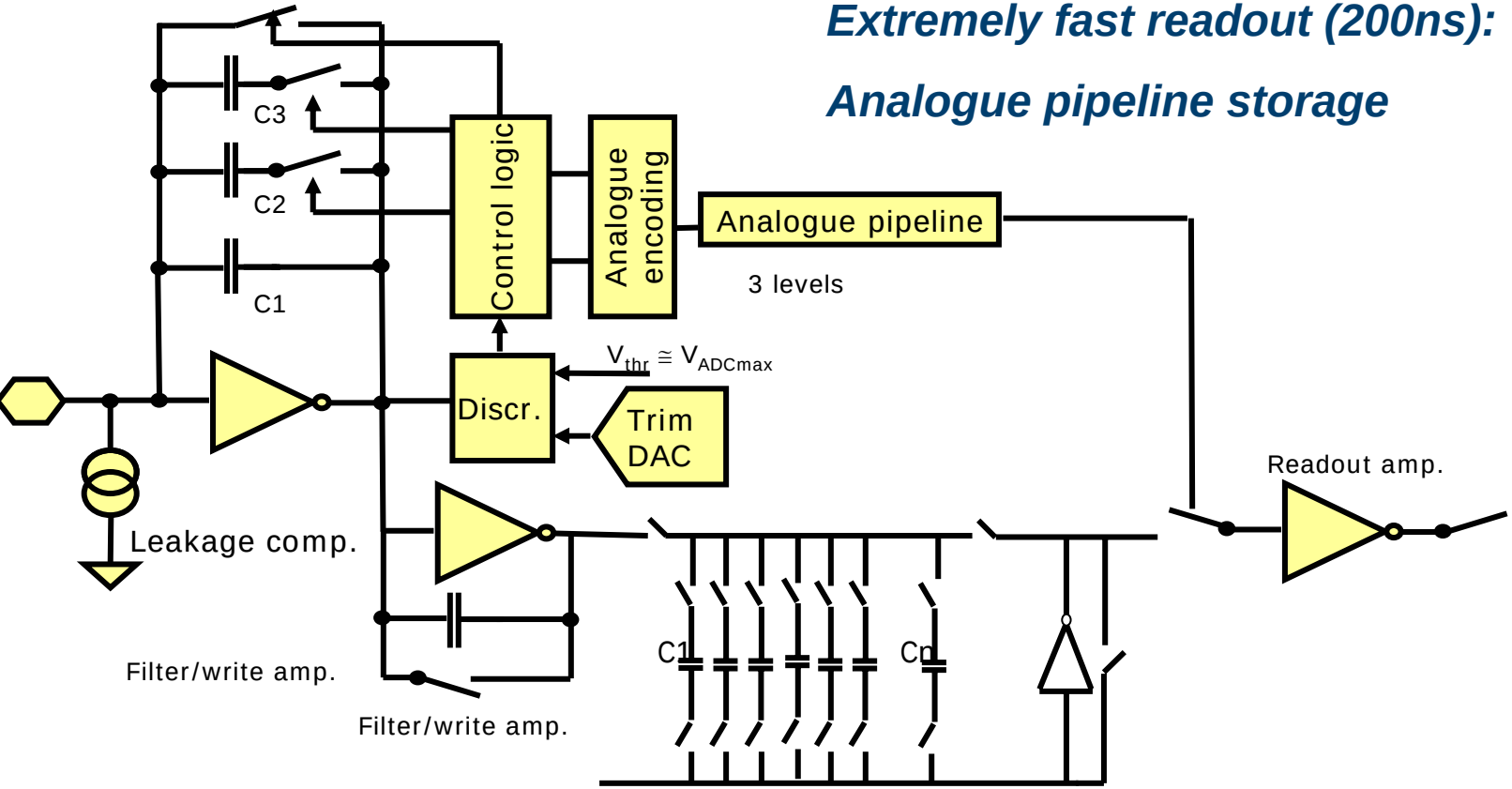
The Adaptive Gain Integrating Pixel Detector

High dynamic range:

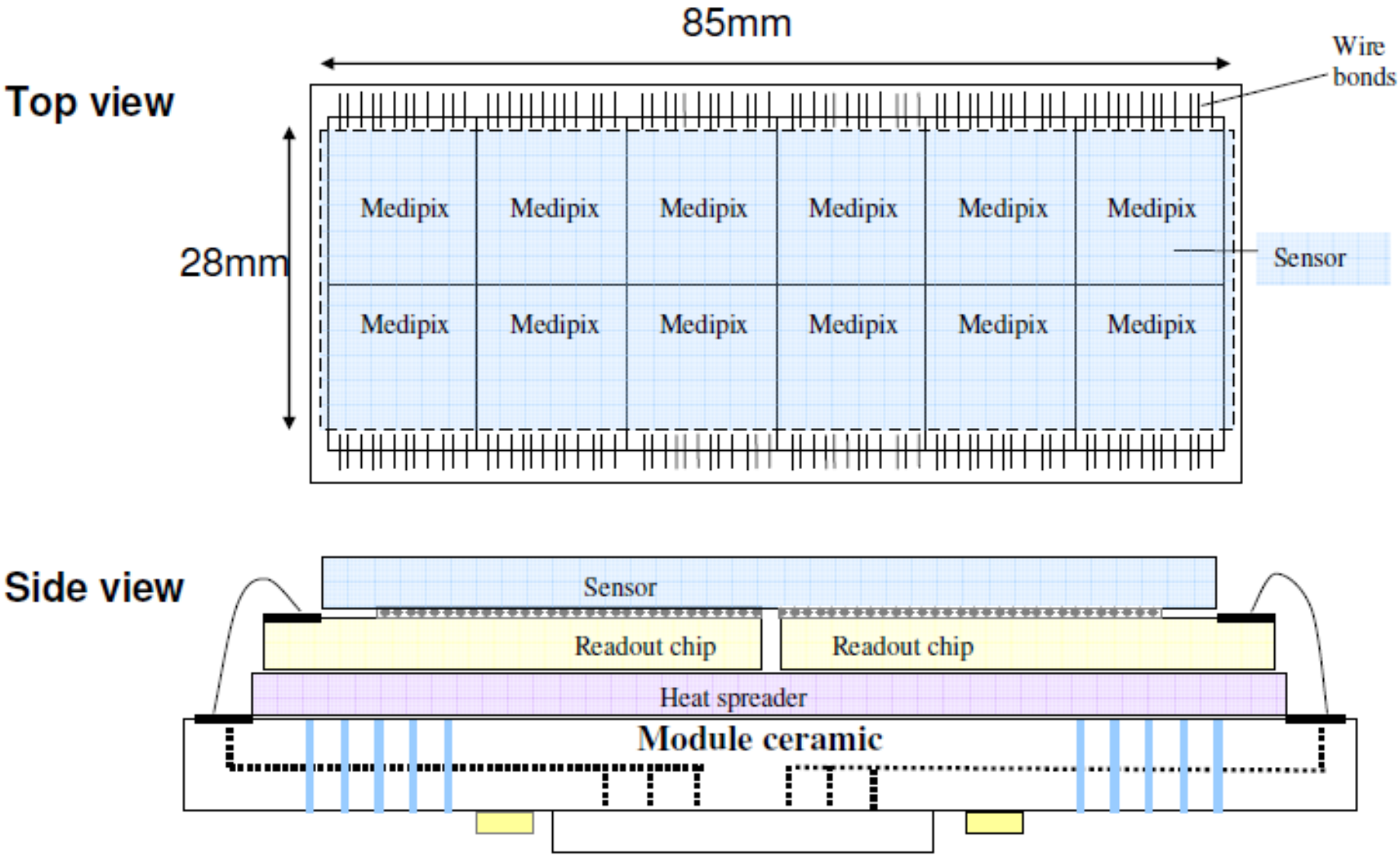
Dynamically gain switching system

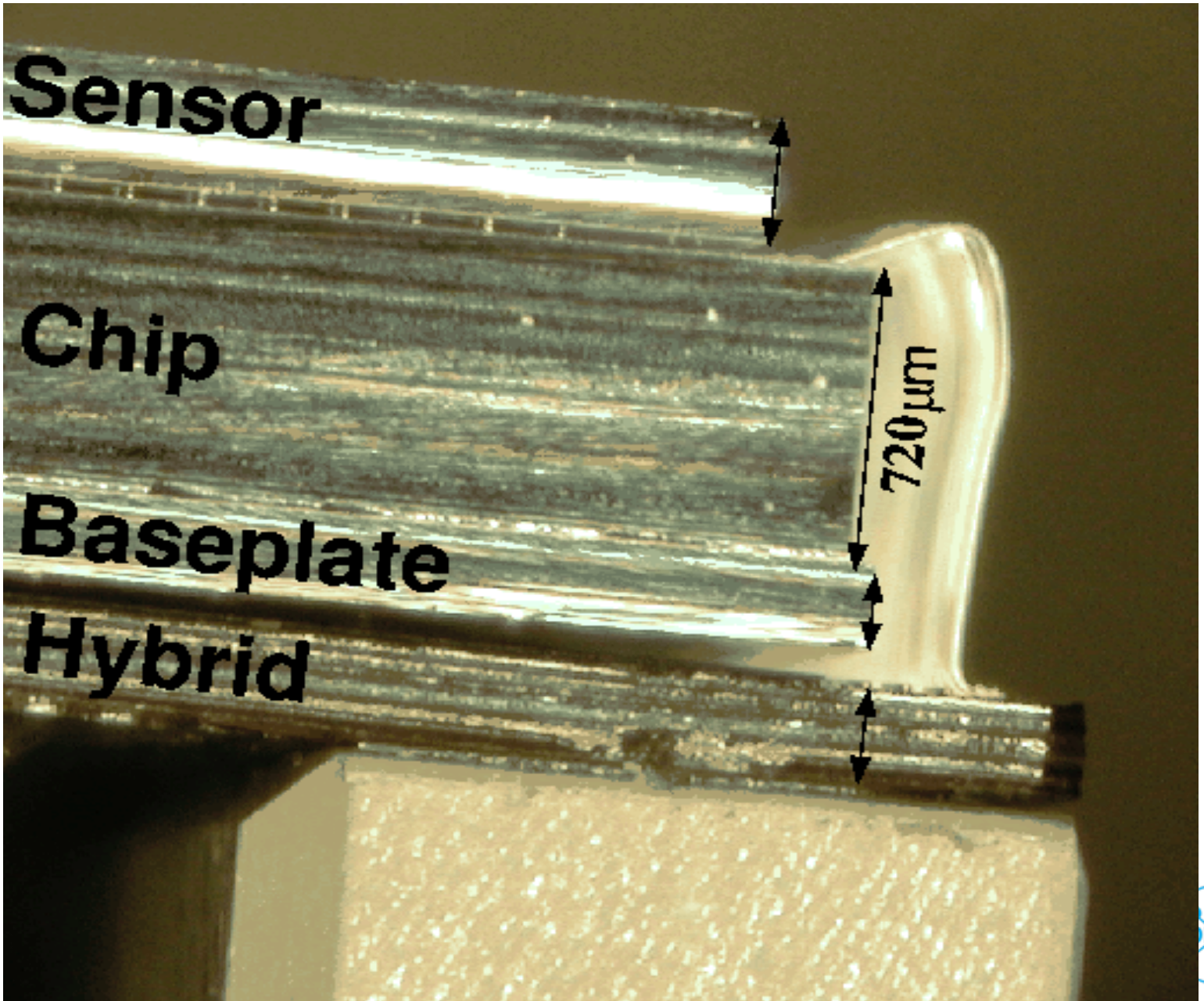
Extremely fast readout (200ns):

Analogue pipeline storage

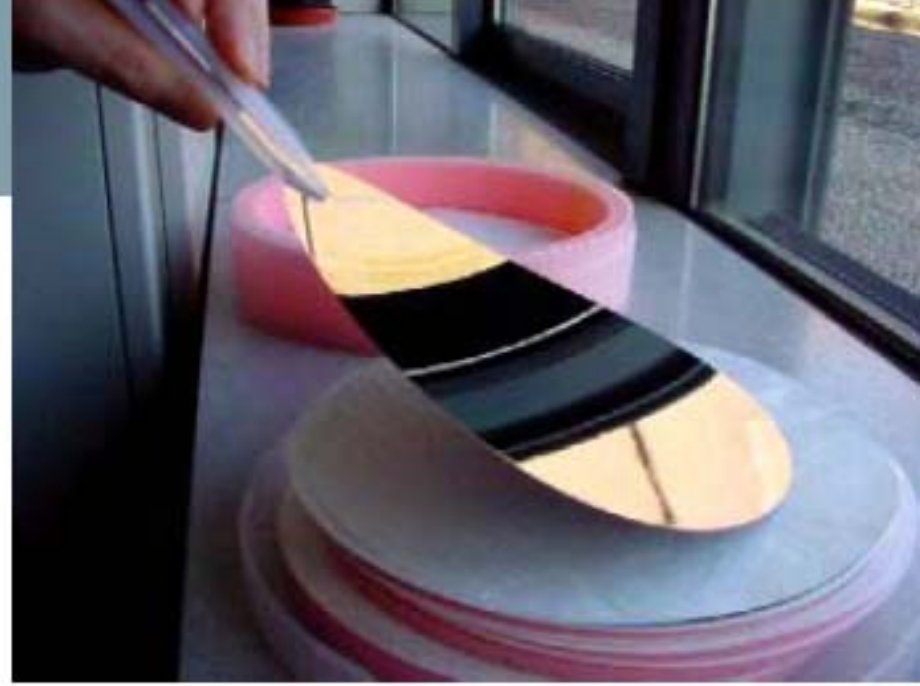


Schematic layout of a Hybrid Pixel Array Detector (HPAD)

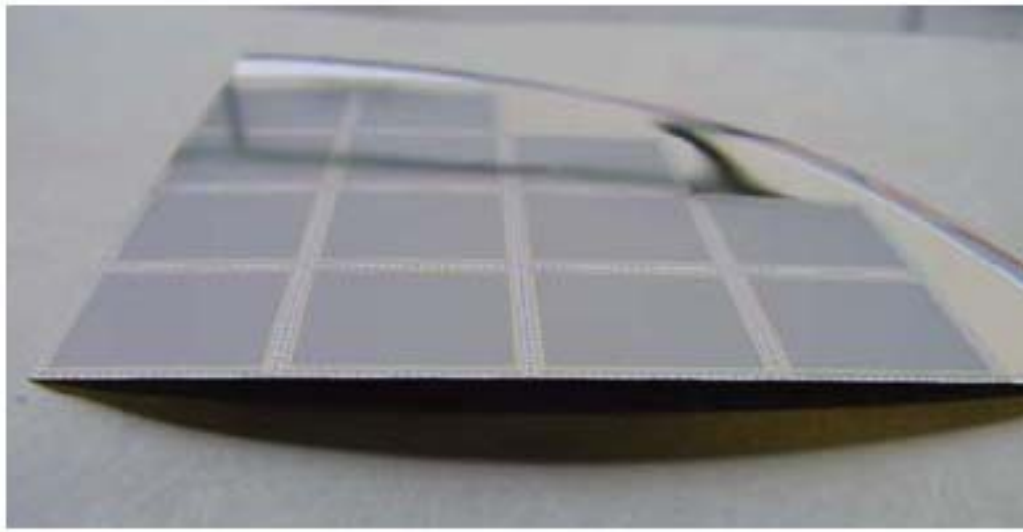



Sensor
Chip
Baseplate
Hybrid
720µm

Technology enablers: Wafer thinning



- Technology:
  - rough/fine grinding, dry/wet etch at wafer level
  - Si, glass, GaAs, …
  - critical: thinning damage, impact on devices
  - very thin wafers (< 100 um): use of carrier wafers and temporary (de-)bonding technology
- Features:
  - thinning down to 15 um
  - total thickness variation < 1 um
- Advantages/Applications:
  - thin (3D) integration
  - embedding in flexible substrates
  - backside illuminated imagers
  - ultra low X_0 -> tracking detectors



Technology enablers:
TSV processing during CMOS process

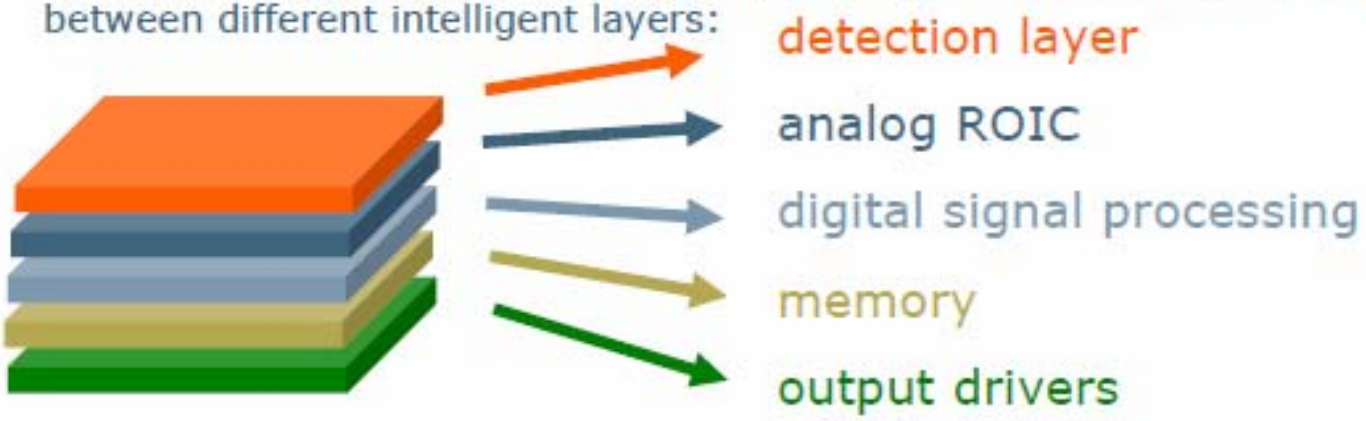
- Technology:
  - fabrication at device level, i.e. as a part of (CMOS) flow
  - after FEOL, before BEOL
  - will become established in advanced CMOS foundries (core partners, e.g. TSMC, Matsushita, Intel, Micron, …) participate in 3D IC work at IMEC

- Specifications:
  - Si thickness: 10 – 20 um
  - via diameter: 3 – 5 um
  - via pitch: 10 um

- Applications:
  - Pixel level interconnect
  - imager/processor/logic/memory stacking

Conclusions & outlook II

- High **sensitivity** by extreme thinning and backside illumination
- **3D integration technology** will allow manufacturing of **advanced detection systems**:
  - **complex** imaging detectors using high density 3D interconnects (≥1 per pixel) between different intelligent layers:



- Economical aspects:
  - (large) commercial foundries will offer 3D in (near) future
  - But: typically large volume
  - Solution: IMEC prototyping/small scale production "CMORE"

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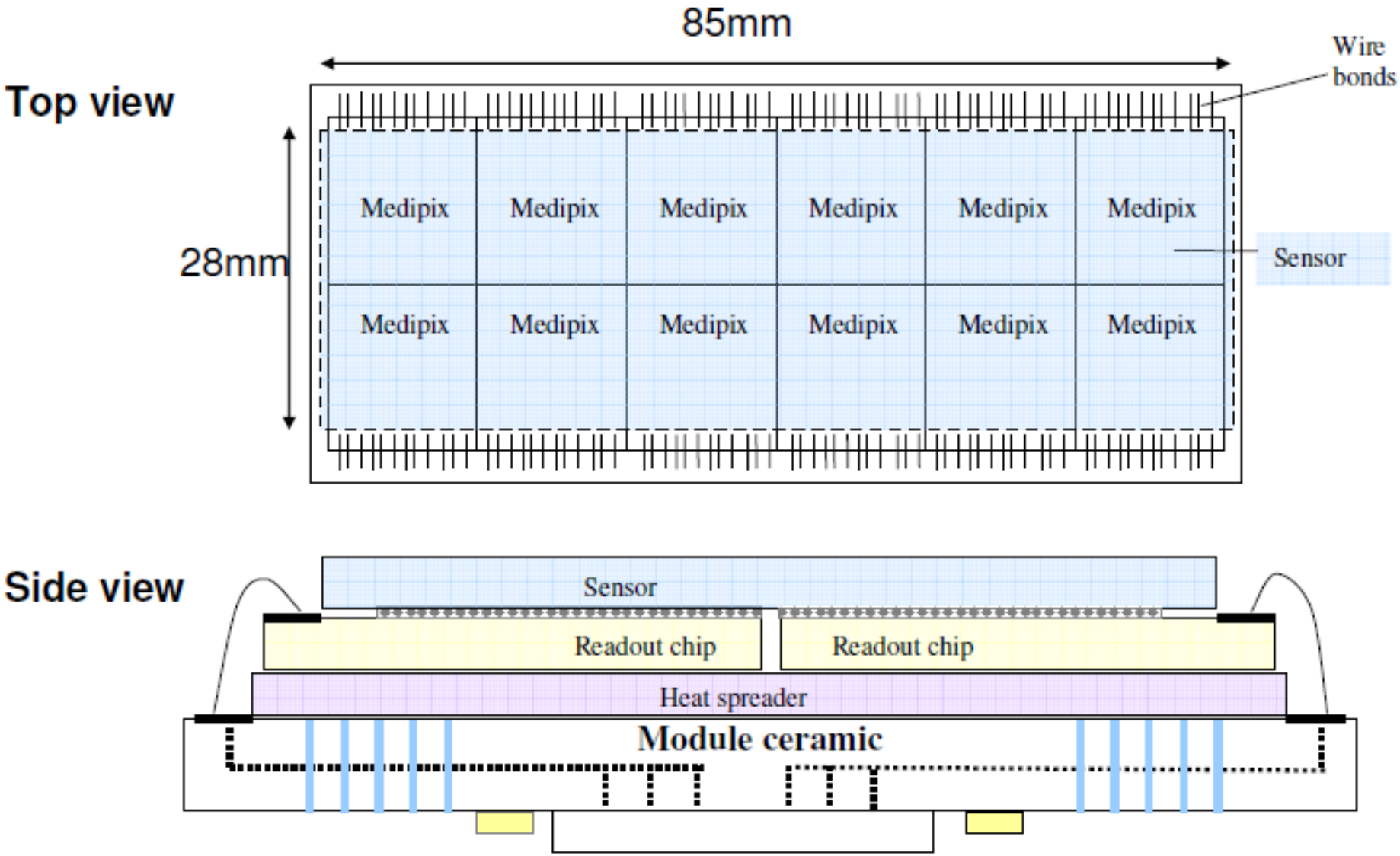
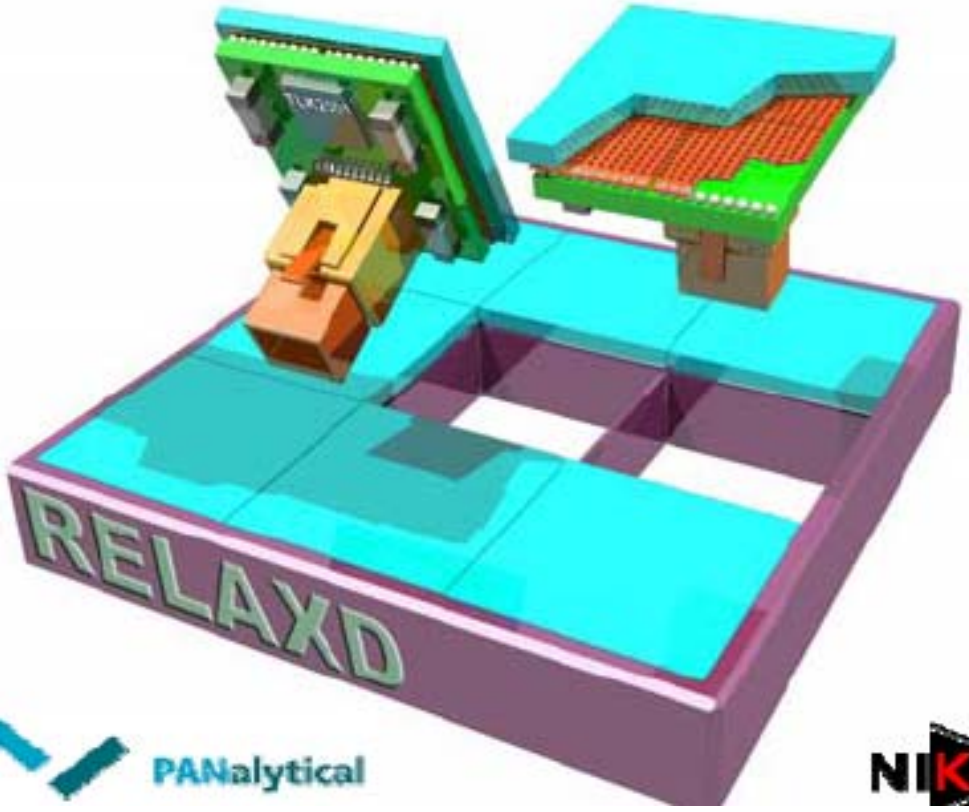
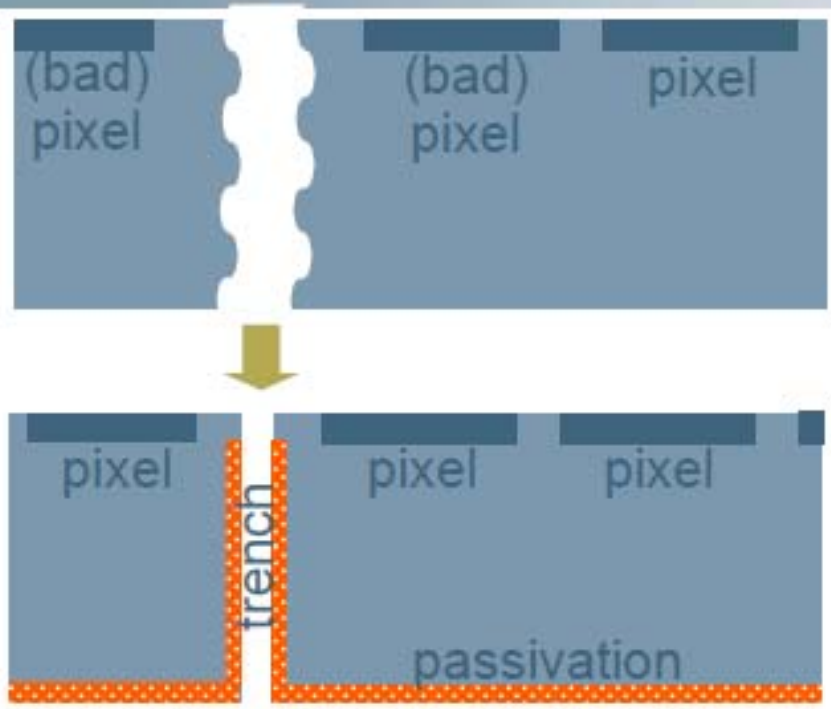


Detector systems:
RelaxD: tilable X-ray imagers

- Issue: bad pixels at imager boundary due to damage by dicing
- Solution: edgeless detector concept:
  - Replace dicing by trench etching and proper passivation





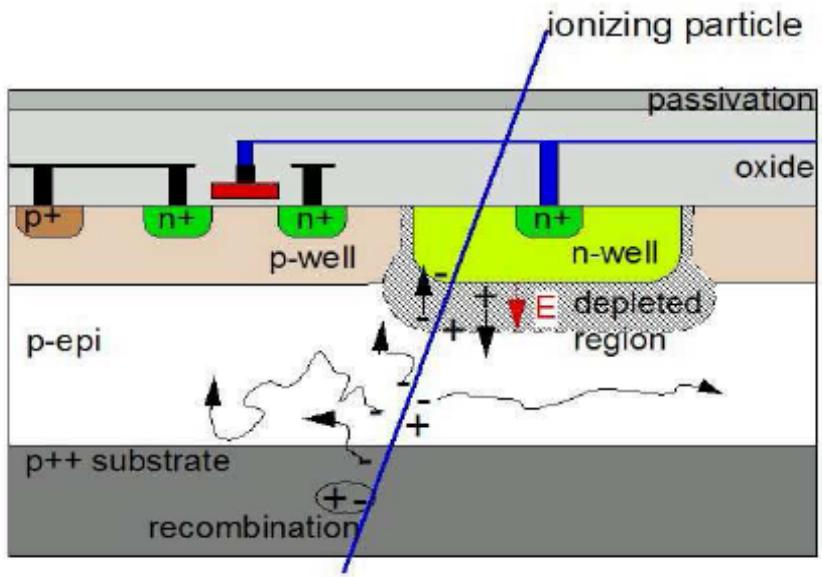
- Status:
  - 3D integration ongoing
  - minimal dead area by trench singulation and in situ passivation

PANalytical NIKHEF CANBERRA

Other very promising options: CMOS (MAPS)

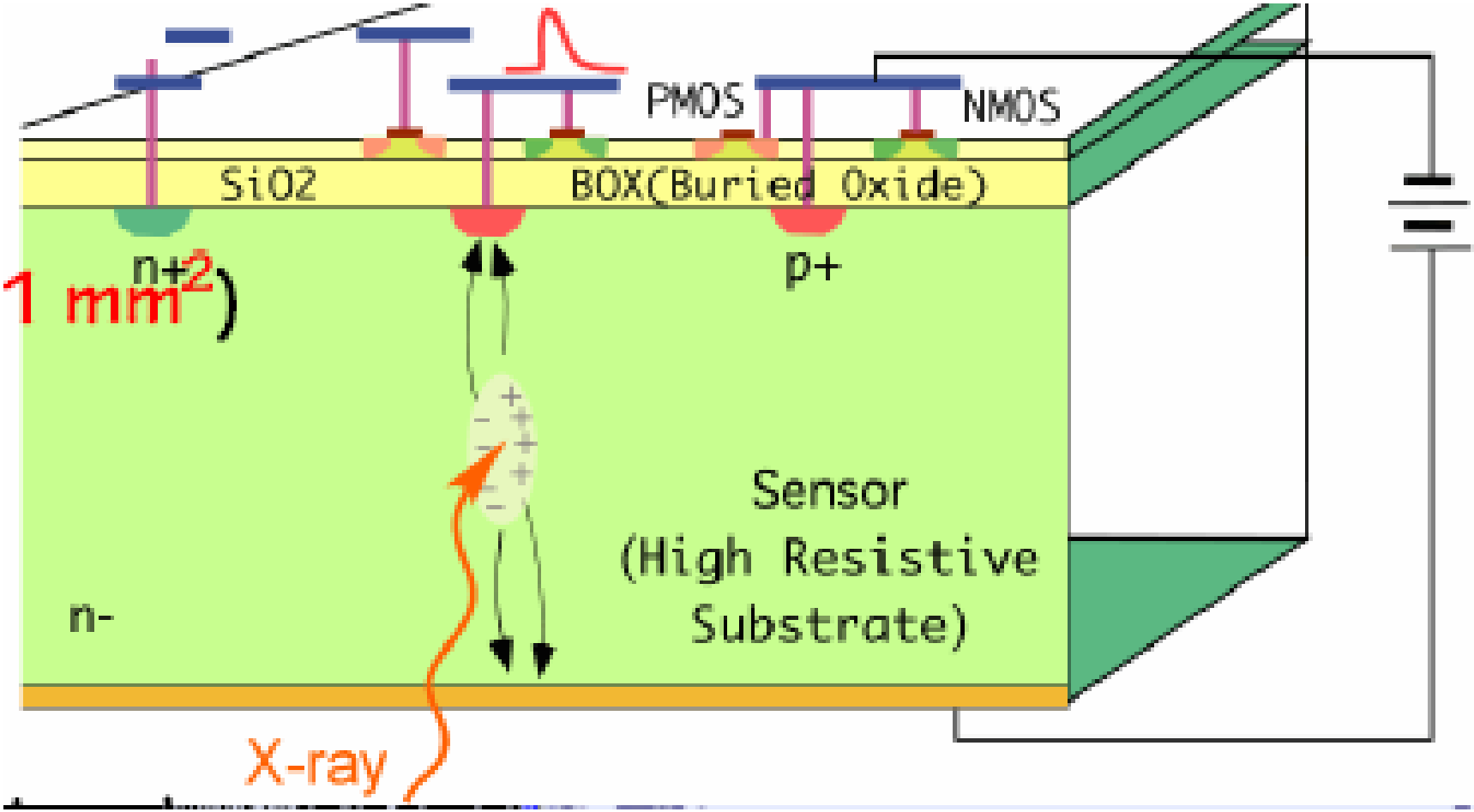
Pixel Sensors for HEP - **CMOS Sensors: Main Features**

- **p-type low-resistivity Si hosting n-type "charge collectors"**
  - *signal created in epitaxial layer (low doping):*
    $Q \sim 80$ e-h / $\mu m \mapsto$ signal $\lesssim 1000\ e^-$
  - *charge sensing through n-well/p-epi junction*
  - *excess carriers propagate (thermally) to diode with help of reflection on boundaries with p-well and substrate (high doping)*



- **Specific advantages of CMOS sensors:**
  - ◇ *Signal processing μcircuits integrated on sensor substrate (system-on-chip) $\mapsto$ compact, flexible*
  - ◇ *Sensitive volume ($\sim$ epitaxial layer) is $\sim$ 10–15 μm thick $\longrightarrow$ thinning to $\sim$ 30–40 μm permitted*
  - ◇ *Standard, massive production, fabrication technology $\longrightarrow$ cheap, fast turn-over*
  - ◇ *Room temperature operation*
  - ◇ Attractive balance between granularity, mat. budget, rad. tolerance, r.o. speed and power dissipation
    - ⋈ *Very thin sensitive volume $\rightarrowtail$ impact on signal magnitude (mV !)*
    - ⋈ *Sensitive volume almost undepleted $\rightarrowtail$ impact on radiation tolerance & speed*
    - ⋈ *Commercial fabrication (parameters) $\rightarrowtail$ impact on sensing performances & radiation tolerance*

Other very promising options: Silicon-on-Insulators (SoI)



Summary Future and Challenges Pixel Detectors.

- New sensor materials (diamond, High-Z).
- New sensor structures: 3D, edgeless, …
- 3D ASICs (staking ASICs together): increased functionality per area.
- 3D intergration to avoid dead areas.
- Monolithic Active Pixel Sensors (MAPS/CMOS)
- Silicon-on-Insulator (SoI)
- Maybe more exotic electronics: nano-tubes, organics?
- But challenges: thermal management, affordability, radiation tollerance, ..

The Future depends on you !