The FEL detector development program at DESY

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WorkPackage Detectors for XFEL
### Hard X-ray SASE Free Electron Lasers

#### LINAC COHERENT LIGHT SOURCE
**LCLS**
2009

- **FLASH**: 5 Hz, 10 Hz and 5 MHz
- **LCLS**: 120 Hz
- **SCSS**: 60 Hz
- **XFEL**: 5 Hz, 10 Hz and 5 MHz

**European XFEL Facility**
2013

**FLASH**
in operation
pnCCD: 1024 x 512, 30 cm$^2$

for 1 keV X-rays the system delivers 2k x 2k resolution points

Imaging
7.8 x 3.7 cm$^2$ = 29.6 cm$^2$
75 x 75 μm$^2$
1024 parallel read nodes
2 e$^-$ @ 250 fps
### Requirements of the FLASH, LCLS and XFEL

**Photon Counting and Integrating X-ray Imaging Detectors**

<table>
<thead>
<tr>
<th>Feature</th>
<th>FLASH, LCLS + XFEL</th>
<th>pnCCD system</th>
</tr>
</thead>
<tbody>
<tr>
<td>single photon resolution</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>energy range</td>
<td>$0.05 &lt; E &lt; 24$ (keV)</td>
<td>$0.05 &lt; E &lt; 25$ [keV]</td>
</tr>
<tr>
<td>pixel size ($\mu$m)</td>
<td>100</td>
<td>75</td>
</tr>
<tr>
<td>sig.rate/pixel/bunch</td>
<td>$10^3$ ($10^5$)</td>
<td>$10^3$ - $10^4$</td>
</tr>
<tr>
<td>quantum efficiency</td>
<td>$&gt; 0.8$</td>
<td>$&gt; 0.8$ from 0.6 to 12 keV</td>
</tr>
<tr>
<td>number of pixels</td>
<td>512 x 512 (min.)</td>
<td>1024 x 1024 and 2048 x 2048</td>
</tr>
<tr>
<td>frame rate/repetition rate</td>
<td>10 Hz - 120 Hz</td>
<td>up to 250 Hz</td>
</tr>
<tr>
<td>Readout noise</td>
<td>$&lt; 50$ e$^-$ (rms)</td>
<td>$&lt; 5$ e$^-$ (rms) (2 e$^-$ possible)</td>
</tr>
<tr>
<td>cooling</td>
<td>possible</td>
<td>around - $80^\circ$ C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>room temperature possible</td>
</tr>
<tr>
<td>vacuum compatibility</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>preprocessing</td>
<td>no (yes) ?</td>
<td>possible upon request</td>
</tr>
</tbody>
</table>
CCD basics

- full depletion (50 µm to 500 µm)
- back side illumination
- radiation hardness
- high readout speed
- pixel sizes from 36 µm to 650 µm
- charge handling: more than $10^6$ e⁻/pixel
- high quantum efficiency
What is limiting the quantum efficiency?

The thickness of Silicon !!

Q.E. = 99% @ 8 keV
d = 0.5 mm

Q.E. = 22% @ 24 keV

d = 0.5 mm
Monolithic Integration of optical blocking filters

Silicon entrance window with $x$ nm of SiO$_2$ and $y$ nm of Si$_3$N$_4$ plus $z$ nm of Al (optical shield)

optical light attenuation: $5 \times 10^6$

Thin entrance window

Quantum Efficiency

Energy [keV]

50 eV

500 eV

800 eV

2000 eV
Detectors for FLASH+LCLS+XFEL+Petra III

Device fabrication is finished now.

The full sensitive area of the system is 59 cm² with 75 µm pixels, 1024 x 1024.

Chip 1: area 29.5 cm²
format: 1024 x 512

Chip 2: area 29.5 cm²
format: 1024 x 512

Transfer of signal charges
Insensitive gaps: ≈ 800 µm

Hole diameter: 3 mm

Full Frame imaging area per chip: 512 x 1024

Pixel size: 75x75 µm²

Total area per chip: 29.5 cm²

Readout time per frame: 4 ms
i.e. 250 fps
Can be triggered externally.

Total sensitive system area: 59 cm²

16 ADC outputs

EUROEFL-2009
ASG Chamber

View on detector I+II, two systems 1k x 1k each. Detector 1 is movable, Detector 2 is fix.

System alignment:
Detector 1 is movable in Y, Z and X (limited), 400 mm Ø
Detector 2 is fixed, 250 mm Ø
2048 x 2048 CCD array
(resolution points:
  at least 4x4k @ 1 keV)

pixel size: 75 x 75 µm²

total area: 236 cm²

readout time: < 8 ms

read noise < 15 electrons

Charge handling capacity:
  > 1000 photons pp

Energy 0.1<E<24 keV

thickness: 500 µm

operation temperature: -40°C
European XFEL: where is the challenge?

**Challenges:**
- up to 30,000 bunches per second
- very high intensities (up to $10^{12}$/bunch)
- "instantaneous" energy deposition
- very high repetition rates (up to 5 MHz)
- large variability
  - pulse patterns
  - pulse to pulse variations
Thinking ahead...

- It is difficult to think over 9 orders of magnitude.
Some Requirements and Specifications

Requirements:
• 1k x 1k (4k x 4k) pixels
• “no noise”
• $10^4$ ph/pixel/pulse
• Few 100 images/train
• …

Consequences:
• Integration detectors
• Low noise
• In-pixel frame storage
• Multiple gains or
• Non-linear gain
The Large Pixel Detector (LPD) Project (STFC)

Multi-Gain Concept
Dynamic Range Compression required
Experience with calorimetry at CERN
Relaxes ADC requirements
Fits with CMOS complexity

Threefold analogue pipeline
On-chip ADC

Sensor
Preamplifier
Multiple Gains
Pipeline

STFC/RAL
University of Glasgow
The Large Pixel Detector (LPD) Project (STFC)

Sensor tile detail (exploded view)

- Hidden wire bonds permit ‘edge-to-edge’ sensors
- Sensor bias communicated via ASC and interposer

- Sensor tile
- Silicon interposer
- ASIC Die
- Moly Metal Mount

128 x 32 pixels of 500 x 500 μm
The Large Pixel Detector (LPD) Project (STFC)

Super modules:
8 x 2 tiles
(256 x 256 pixels)
DSSC - DEPMOS Sensor with Signal Compression (MPI-HLL)

DEPFET per pixel

- Very low noise (good for soft X-rays)
- Non linear gain (good for dynamic range)
- Per pixel ADC
- Digital storage pipeline

200μm × 200μm pixel

Combines DEPFET with small area drift detector (scaleable)

MPI-HLL, Munich
Universität Heidelberg
Universität Siegen
Politecnico di Milano
Università di Bergamo
DESY, Hamburg

(L. Strüder, MPI-HLL)
DSSC - DEPMOS Sensor with Signal Compression (MPI-HLL)

Source follower readout
source load 0.5pF in parallel to 100kOhm

Output voltage as function of charge

Signal charge collection in Internal Gate

channel region
inner source region
outer source region
DSSC - DEPMOS Sensor with Signal Compression (MPI-HLL)

Block Diagram

- Pad
- Amp
- Filter
- S&H Buf
- ADC
- Latches
- Digital Memory
- Control, Refresh
- Pixel Control, Bias, Trim
- (Voltage Regulation)
- Memory Control, Refresh
- Slow Control
- Address, Strobes
- Data Readout, Serializer
- IO Pads
- Test Injection
- Bias DACs
- Slow Control
- ADC Control (Logic, PLL, Gray Coder, Buffers)
- Global control (burst/gap, refresh, triggers)
- Regulation

(L. Strüder, MPI-HLL)
AGIPD - Adaptive Gain Integrating Pixel Detector (DESY)

Basic parameters
200 μm x 200 μm pixels
5 MHz framing speed
Single photon sensitivity at 12keV
2 x 10^4 dynamic range, using 3 switched gains
>200 images storage depth
128 x 256 monolithic tiles
Flat detector

The AGIPD consortium:
PSI/SLS - Villingen: chip design; interconnect and module assembly
Universität Bonn: chip design
Universität Hamburg: radiation damage tests, “charge explosion” studies; and sensor design
DESY-Hamburg: chip design, interface and control electronics, mechanics, cooling; overall coordination
AGIPD - Adaptive Gain Integrating Pixel Detector (DESY)

Concept
wide dynamic input range
multiple (3) scaled feedback capacitors
reduced ADC resolution (10 bit instead of 12bit)
analogue + analogue encoded (2 bit) pipeline
**AGIPD Dynamic Range (DESY)**

**Integrator gain requirements:**

Effective analogue resolution $\geq 8$ bit

Analogue resolution always better than “statistical noise” $\sqrt{n_{\text{ph}}}$

maximum signal $\geq 10^4$ photons

<table>
<thead>
<tr>
<th>range</th>
<th>norm. gain</th>
<th>$C_f$ [fF]</th>
<th>max $n_{\text{ph}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>100</td>
<td>256</td>
</tr>
<tr>
<td>2</td>
<td>1/16</td>
<td>1600</td>
<td>4096</td>
</tr>
<tr>
<td>3</td>
<td>1/64</td>
<td>6400</td>
<td>16384</td>
</tr>
</tbody>
</table>

![Graph showing output voltage vs. number of 12.4 KeV photons for different $C_f$ values](image)
AGIPD - Adaptive Gain Integrating Pixel Detector (DESY)

100 msec “loss free” Charge Storage in Analogue Pipeline
Thick oxide & MIM caps in IBM process are OK
Switch design is the challenge
AGIPD Adaptive Gain Integrating Pixel Detector (DESY)

64 x 64 pixel/chip
2 x 8 chips/sensor
1 x 4 sensors/quadrant
4 quadrants =
1024 x 1024 = 1048576 pixel
AGIPD: How things will look

The PILATUS 6M of the SLS@PSI

AGIPD mechanics will be based on the Pilatus XFS

Pilatus XFS Module

2x4 (8) Chips per Module.
~78 x 39 mm² (XFS)
~50 x 27 mm² (HPAD)
Detector response simulations (G. Potdevin)

bump bond  chip  sensor  wire bond
HDI  Base plate

Connector to interface electronics

~2mm  ~220mm
Simulation of the detector Performances (G. Potdevin)
The code is built on a modular structure

HORUS

Detector Geometry → Photon Absorption → Electron creation → Electron Drift → Electron collection → Amplification → Electron storage → Readout

Module Tiling → Thickness Material → Fano Factor → Charge spreading → Charge sharing → Amplificator noise → Leakage → ADC

Special pixels at asics border → Parallax → Charge Explosion → Dark current → Gain Switching

Implementation: IDL
DAQ architecture (C. Youngman-WP76)

- Front End Electronics (FEE)
- Front End Interface (FEI)
  - interface to Train Builder.
  - integrated in 2D
- Train builder layer
  - builds trains
  - simple data processing
- PC layer
  - interface to cache
  - additional train building
  - more complex data processing
- Data cache
  - hold, analyze, reduce and reject data
  - post processing
  - commit to silo
A sunny future in Hamburg