

Status of Calibration:

First Module Calibration of AGIPD

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Deutsches Electronen-Synchrotron (DESY)









Content

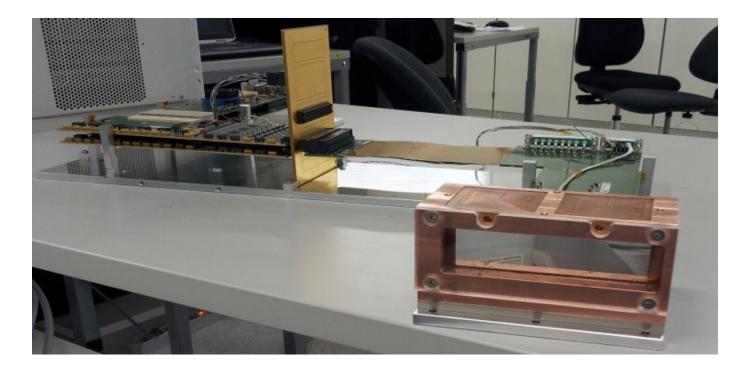


- Calibration infrastructure
- Methods and procedures for individual measurements
- Results from the 1st module
- Calibration "framework"
- Summary and future plan

Calibration infrastructure



• Single module system with water cooling



• <u>Quadrant</u> + <u>multi-purpose vacuum chamber</u> + <u>multi-module system</u> + <u>10 G</u> + <u>DAQ</u>

Timing and bias



• XFEL timing: 22 clocks + 100 MHz \rightarrow 220 ns per cycle

WRITE																								1			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22			LENGTH 2	2	
PRE Reset (min 60ns)																								RSTDLY	6	RSTGAT	14
CDS Reset																								DS1DLY	7	DS1GAT	12
Row Prech																								RPDLYW	C	RPGATW	19
Col Sel																								CSDLYW	0	CSGATW	19
Row Sel																								RSDLYW	C	RSGATW	18
En_ext_Gain																								EGSDLY	6	EGSGAT	14
Gain1ext																								G1SDLY	4	G1SGAT	16
Gain2ext																								G2SDLY	5	G2SGAT	15
TEST_Pulsed_C																								TSTDLY	9	TSTGAT	11
TEST_Current																								TSTDLY	9	TSTGAT	1
READ	-					\vdash		_									\vdash										
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22					
RESET_PXB																								PXBDLY	6		
Row Prech																								RPDLYR	8		
Col Sel																								CSDLYR	2		
Row Sel																								RSDLYR	9		

• Bias of ASICs (optimized): VRFCDS = 700 mV (140),

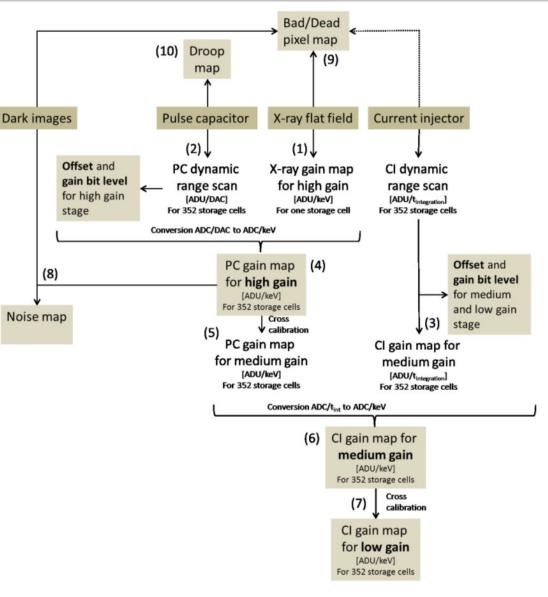
VRFPXB = 850 mV (166) for analog, 650 mV (130) for digital

• Sensor bias: 120 V and module cooled at 15 C

Methods



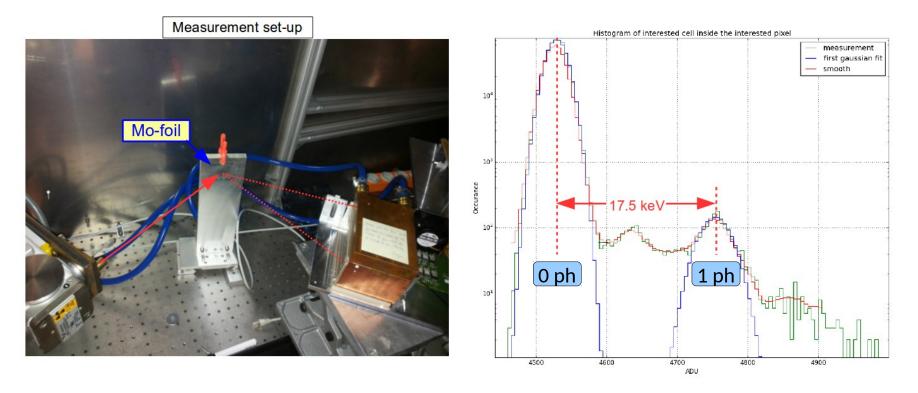
- To be calibrated:
 - Gain (H, M, L)
 - Offset (H, M, L)
 - Gain bit (H, M, L)
 - Noise
 - Dead pixel
 - Droop



Gain calibration



• High gain extraction with X-ray photons for a single memory cell (cell-175)

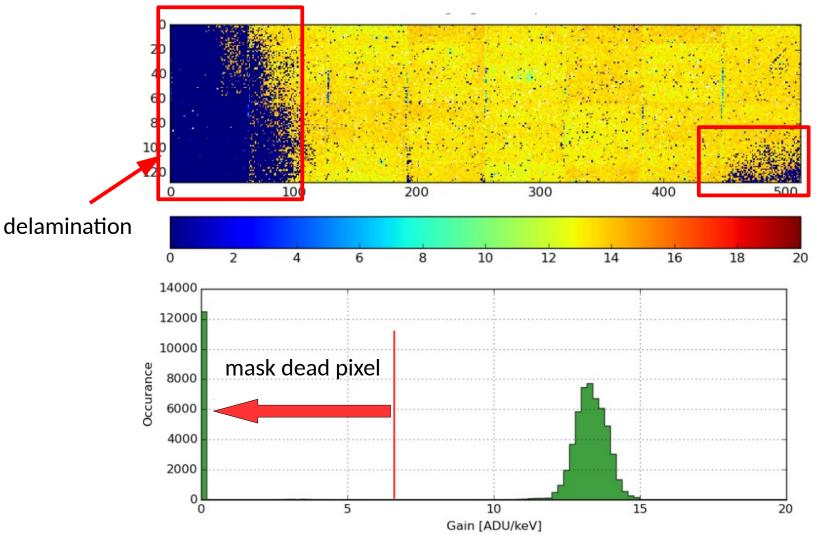


Gain(high) = Δ ADU/17.5 (ADU/keV)

Gain map from photons

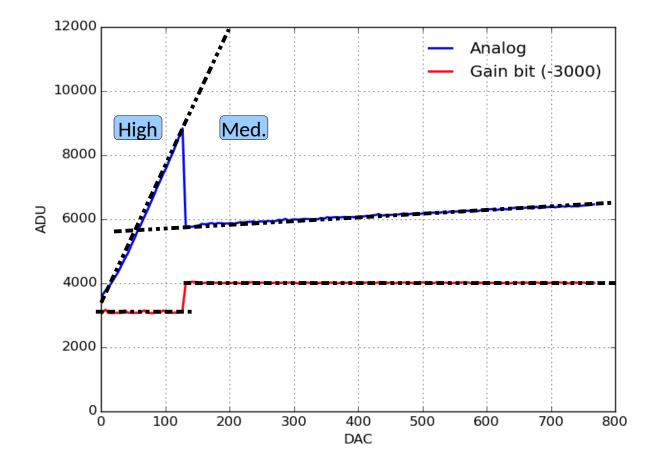


• High gain extraction with X-ray photons for a single memory cell (cell-175)



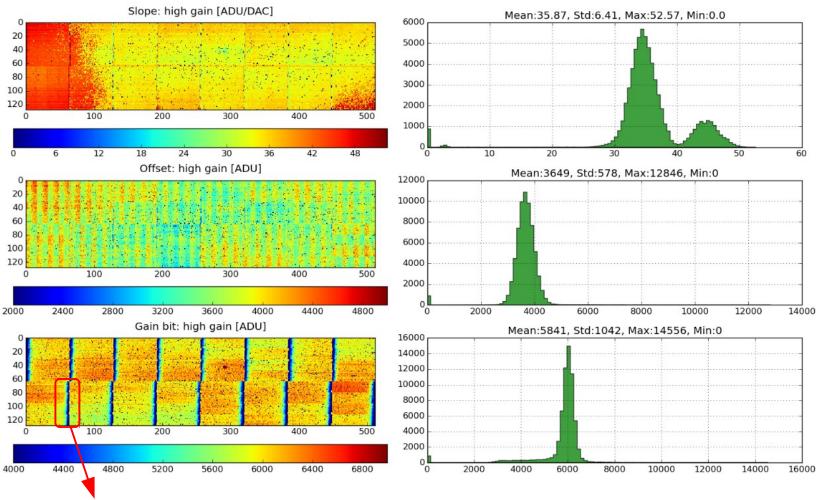


• Extraction of slope (H & M), offset (H & M) and gain bit (H & M)





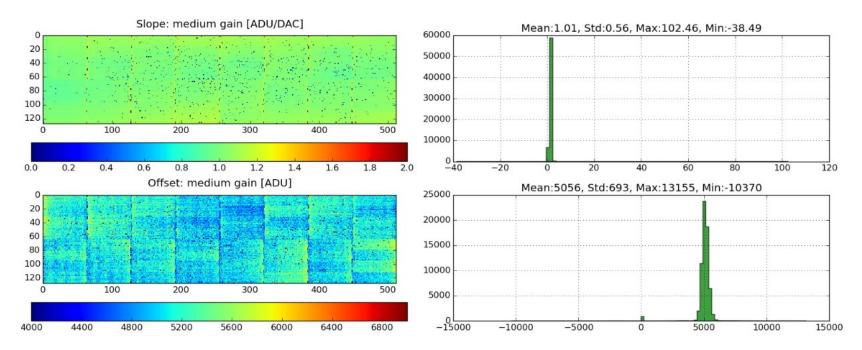
• Results of high gain stage (pixel map for cell-175)



Not enough settling time for VRFPXB \rightarrow can be improved by increasing settling time!

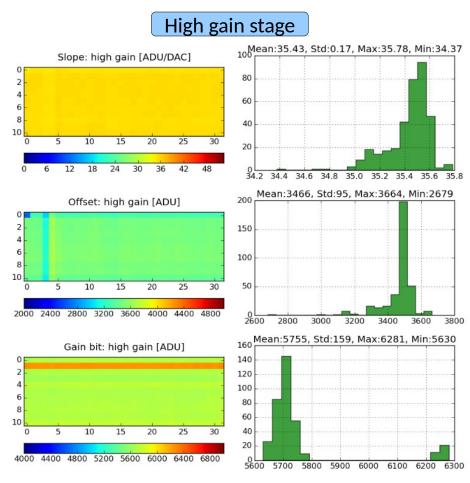


• Results of medium gain stage (pixel map for cell-175)



- Delaminated pixels influence the high-gain slope from PC (maskable)
- Uniform high and medium gain slopes over all pixels
- Gradient gain bit level over ASICs \rightarrow improvable by increasing settling time

Cell map of high & medium gain stage (pixel-[20,200])



Consistent results (slope) in high and medium gain stages for all memory cells

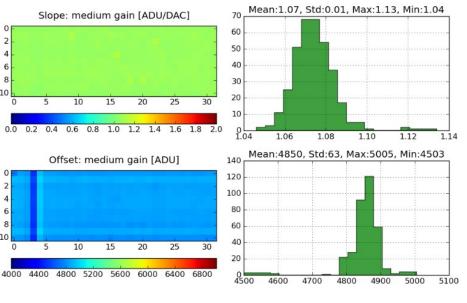
2

10

10

5

5

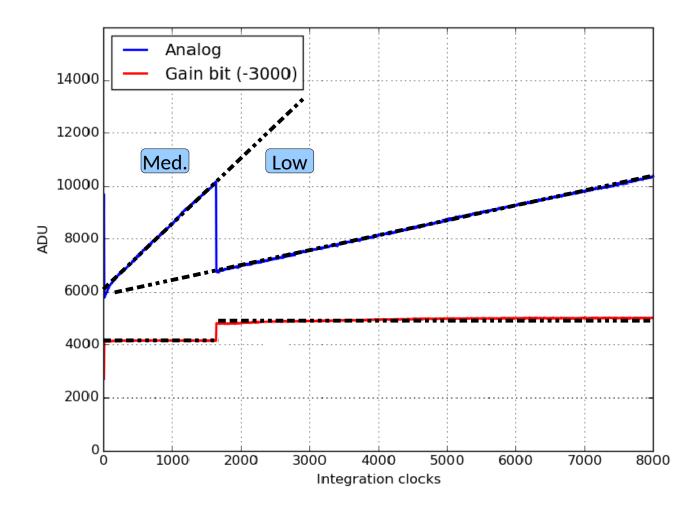


Medium gain stage



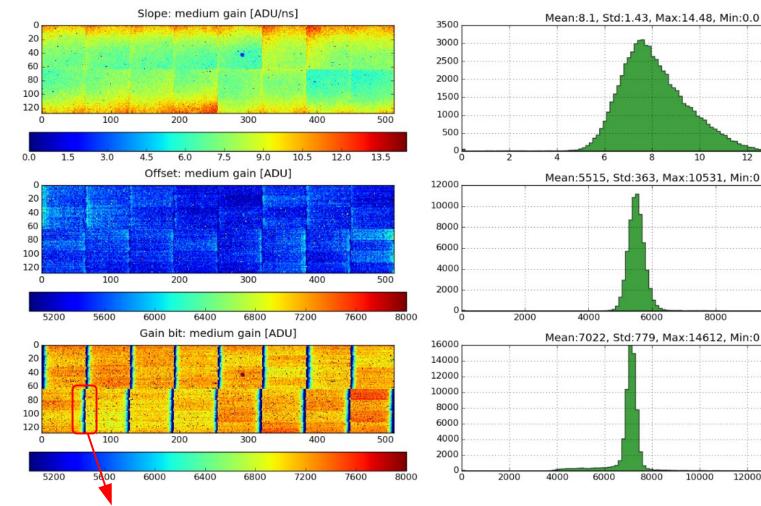


• Extraction of slope (M & L), offset (M & L) and gain bit (M & L)





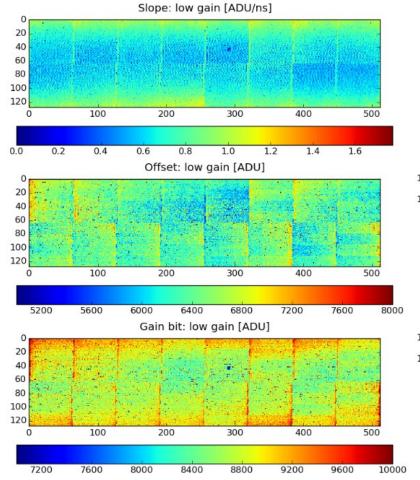
Medium gain stage (pixel map for cell-175) •

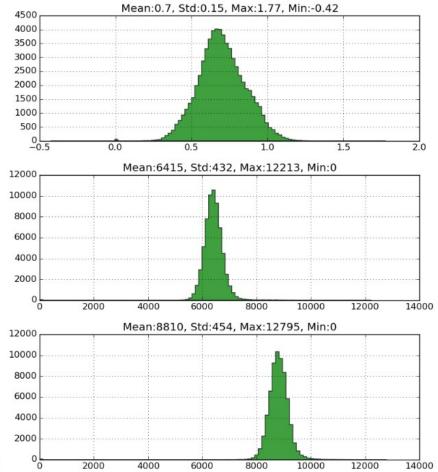


Not enough settling time for VRFPXB \rightarrow can be improved by increasing settling time!



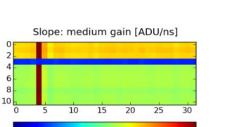
• Low gain stage (pixel map for cell-175)

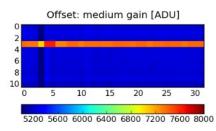




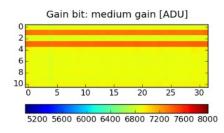
• Cell map of high & medium gain stage (pixel-[20,200])

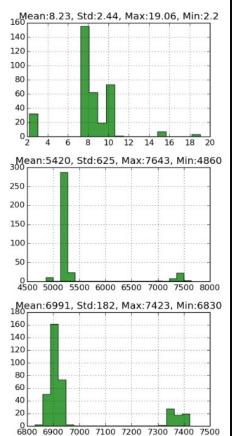
Medium gain stage

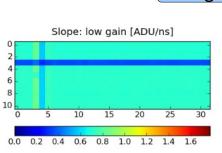




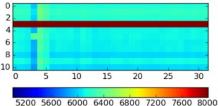
0.0 1.5 3.0 4.5 6.0 7.5 9.0 10.512.013.5

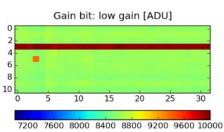




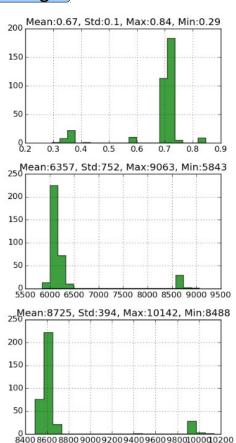


Offset: low gain [ADU]





low gain stage



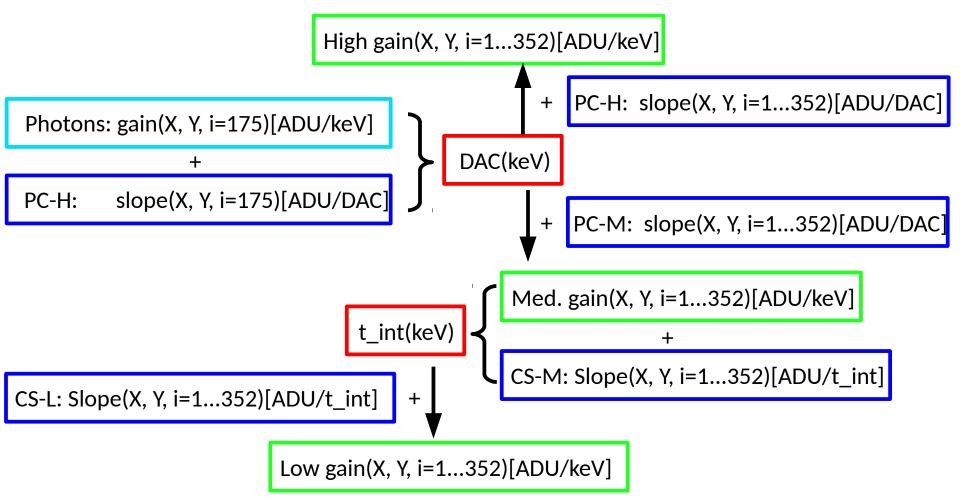
Memory cell row & column dependent ← cross talk



Gain conversion



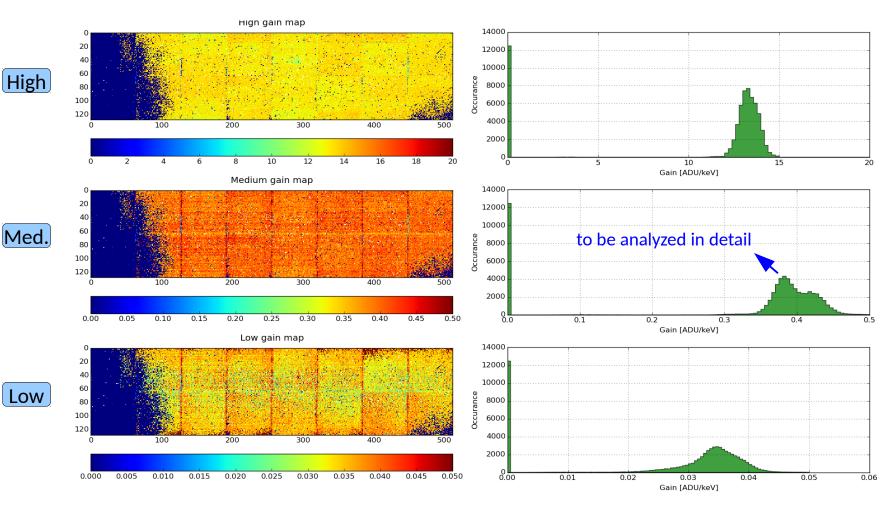
• DAC-to-keV and t_int-to-keV conversion:



Gain map



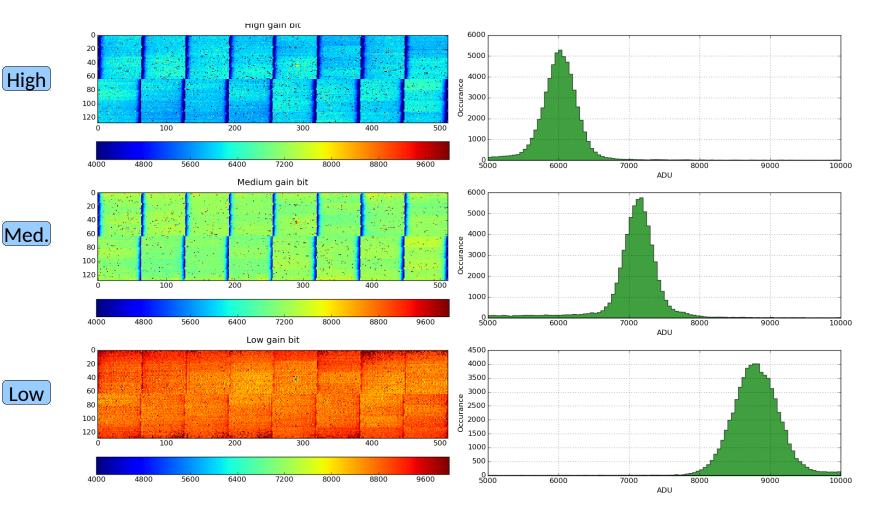
• Gain map (pixel map for cell-175)



Gain bit map



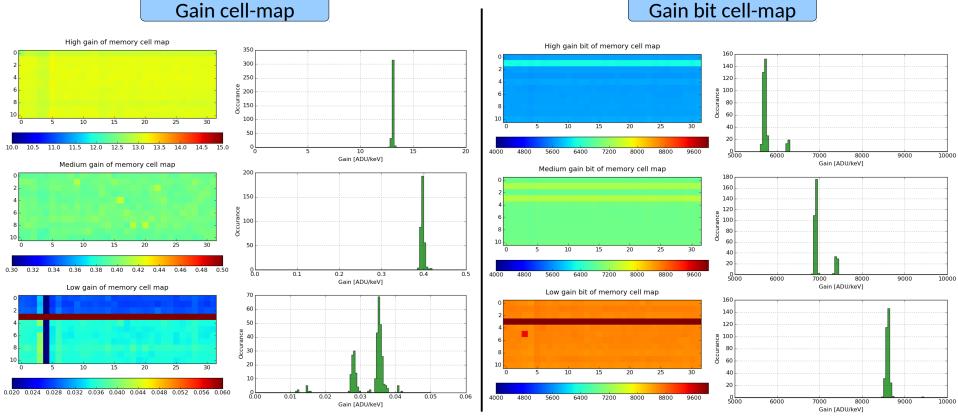
• Gain bit map (pixel map for cell-175)



Gain and gain bit map



• Gain and gain bit map (cell map for pixel-[20,200])

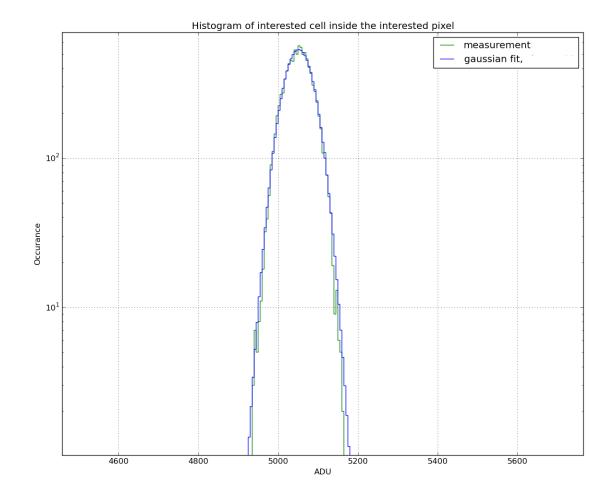


- Consistent gain for all memory cell unit (H & M)
- Cell dependent gain bit level \rightarrow calibratable on the cell basis

Noise



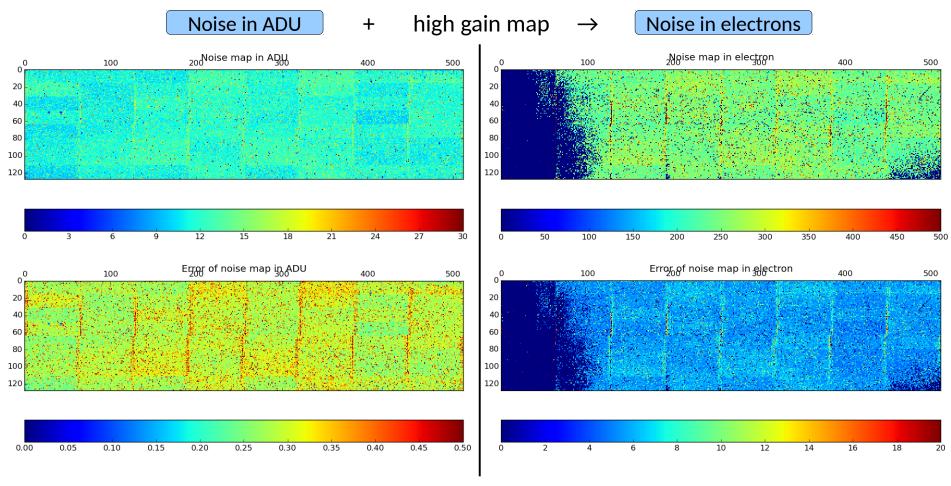
- Dark measurements in light shielded environment
 - 352 memory cells
 - 10 us integration time
 - Gaussian fitting
 - Sigma extracted



Noise map



• Noise pixel-map (cell-175)

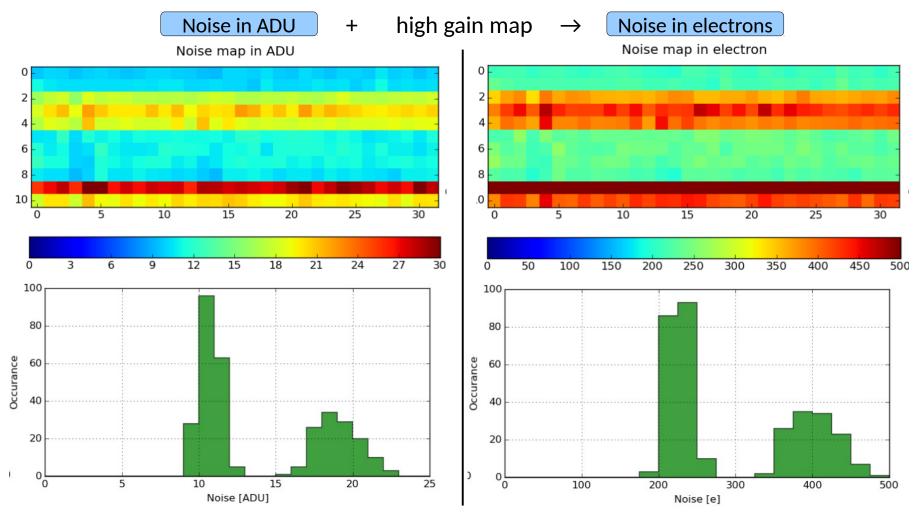


- 220 e⁻ for most of pixels (@ 15 degree C) → can be improved at low temperature

Noise map



• Noise cell-map (pixel-[20,200])

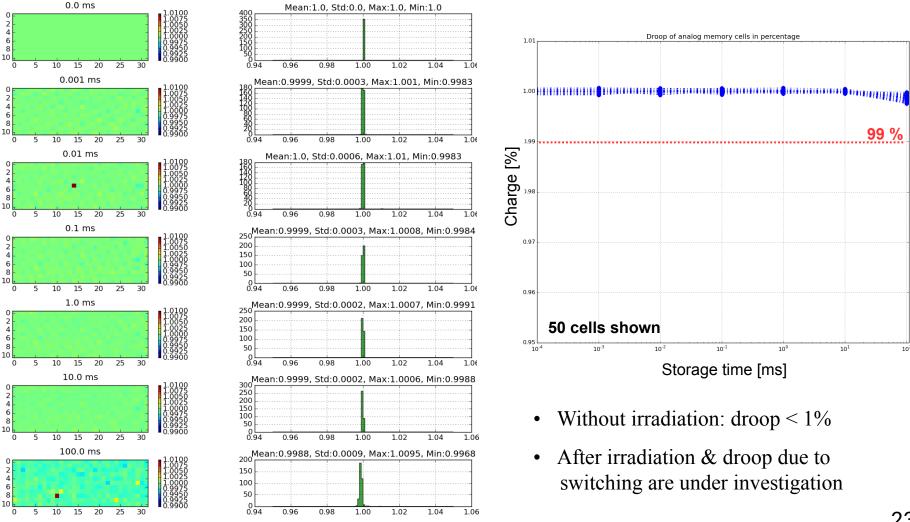


More investigations and compare to different methods \rightarrow has to be confirmed/understood!



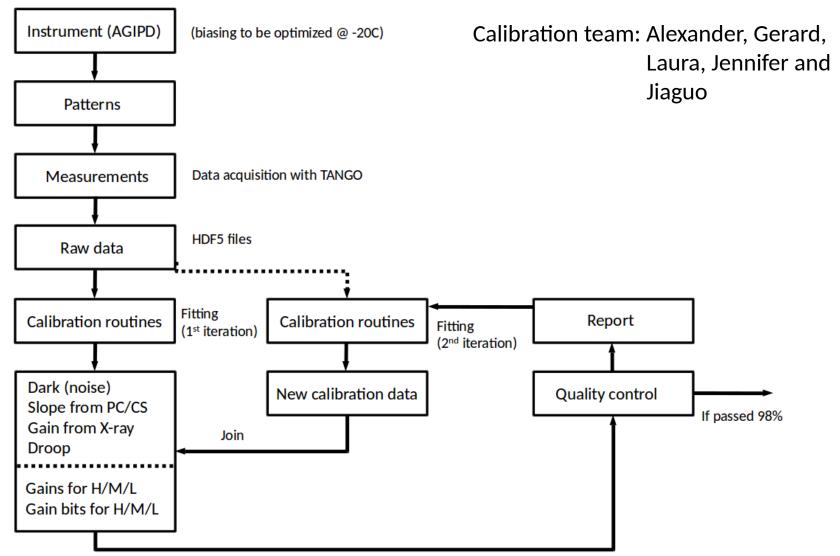


• Droop as function of storage time: 0 (direct write & read), 10, 100 us, 1, 10, 100 ms



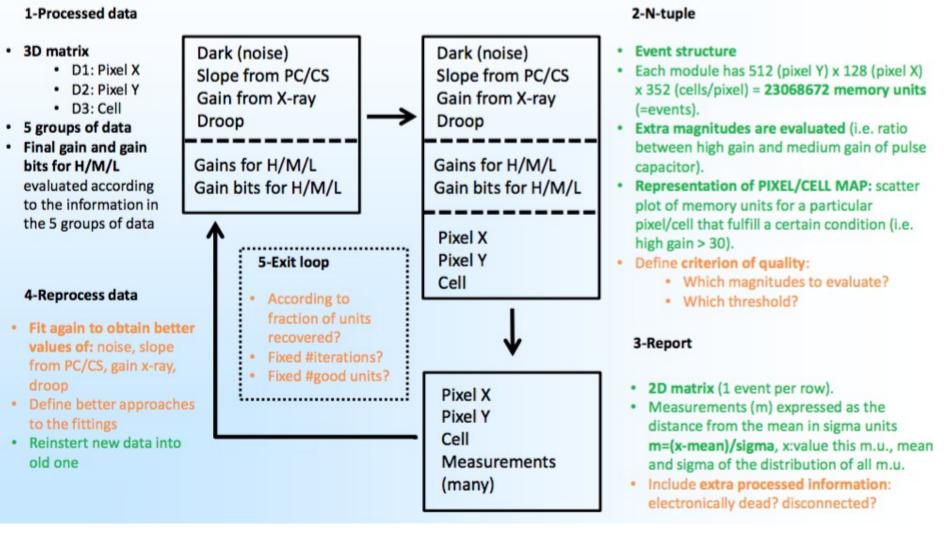
Calibration "framework"





Quality control





Summary



- Calibration procedure and "framework" established
- QC (\rightarrow Gerard) and re-fitting procedures (\rightarrow Jennifer) under development

First module calibrated

- Gains, offsets, gain bits, noise and droop
- Delivered to XFEL in Sept.
- Gain bit uniformity improvable with more settling time

• What is missing and to be understood:

- Fitting error and error propagation to "final" results
- Reliable droop measurement procedure (burst droop) @ different T and irradiations
- ASIC bias optimization at -20 C
- DAQ software for 10 G implemented multi-module system
- All routines adapted to HDF data format compatible



