AGIPD1.0 -> AGIPD1.1
Status / Plans

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AGIPD1.0: Characterization status (Nov 2014)

	Issue	Solution(s)	Criticality
1	**Readout speed:** Variation between offchip routes	Routing change to equalize the different RCs	Very high
2	**Readout speed:** Overall slow speed of analogue outputs	Improve power supply impedance (Offchip driver)	Very high
3	**"Ghosting"**: Crosstalk between outputs	Additional buffer to decouple reference voltage	High
4	**Digital Bit:** "High gain" level (matching to analog baseline)	Writing High Gain Bit with source follower from $V_{ref,CDS}$	Low
5	**Digital Bit:** "Low gain" voltage connected to vnwell_pix	Reconnect the "low gain" voltage to the vdd_pix	Low
6	**Digital Bit:** Optimizing gain bit separation	Different gain for analogue and gain readout (PXB)	Medium
7	**Digital Bit:** No gain encoding in fixed gain mode	Logic change to enable gain bit signals in fixed gain mode	High
8	**Pixel/Memcell maps:** Premature switching of mem row 3 (testI)	Crosstalk: Control Line/TestI increases injected current	High
9	**Pixel/Memcell maps:** "Stripe patterns" in memory map	Crosstalk / Routing change	High
10	**Pixel/Memcell maps:** Variation of baseline over chip	Crosstalk of control signal with $V_{ref,CDS}$	Very high
11	**Pixel/Memcell maps:** Variation of gain over chip	(Possibly) crosstalk in layout / Final reason not identified	Very high
12	**General optimization:** Power-on reset stability	Modify RC circuit	Medium
13	**General optimization:** Small overlap of CLK and token in MUX	Improve MUX_CLK driver	Low
14	**General optimization:** Additional capacitance of TSV pads		Very low
15	**Calibration:** Redesign test current source	Optimization of current mirror / enable switches	Very high
16	**Submission:** Periphery test structure		High
17	**Submission:** Additional layouts	(AGIPD 0.6, other?)	Low

	Status
	: Understood / Redesign needed
	: Understood / Realization to be discussed
	: Under investigation / Idea of reason
	: Under investigation/ Reason unclear

① Calibration circuits √

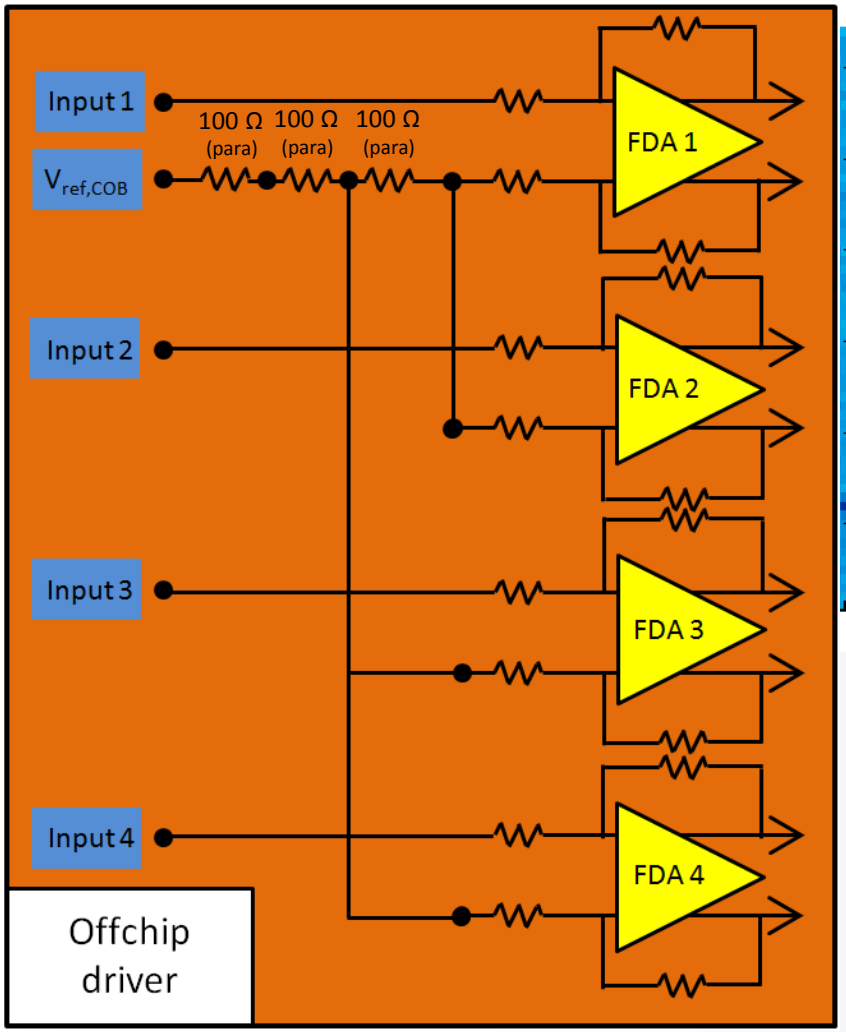
② 'Ghosting'

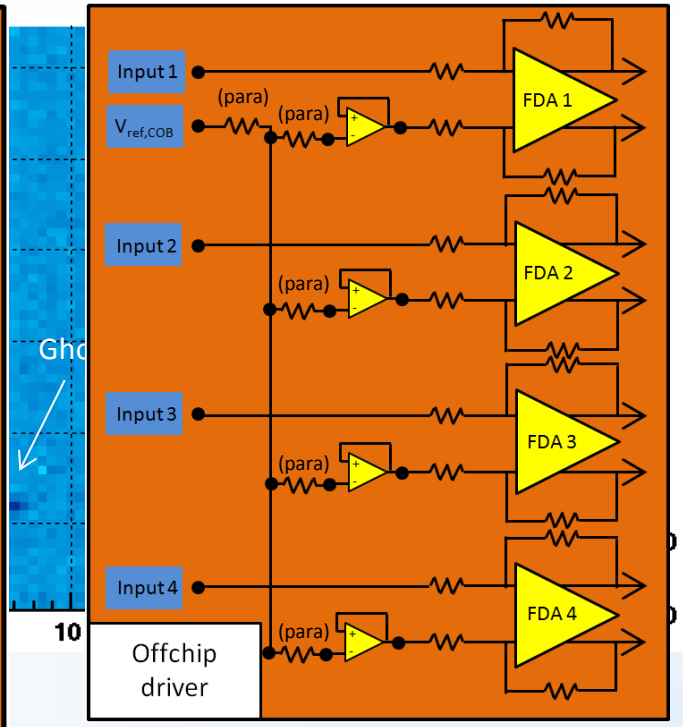
③ Digital bits

④ Readout speed

⑤ Pixel/Memory cell maps

AGIPD1.0: ‘Ghosting’

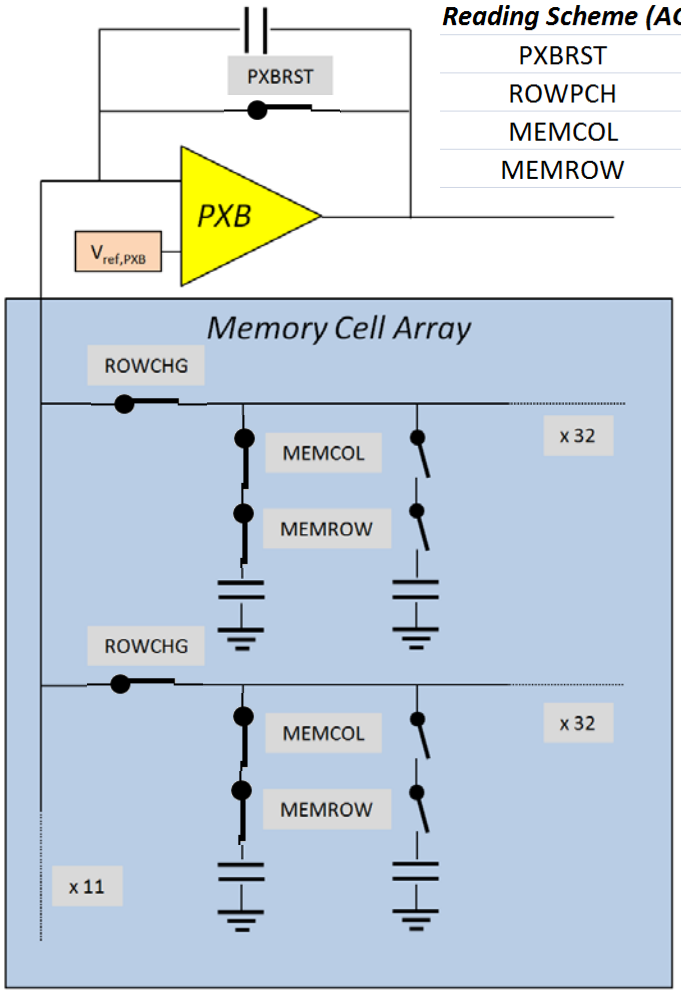


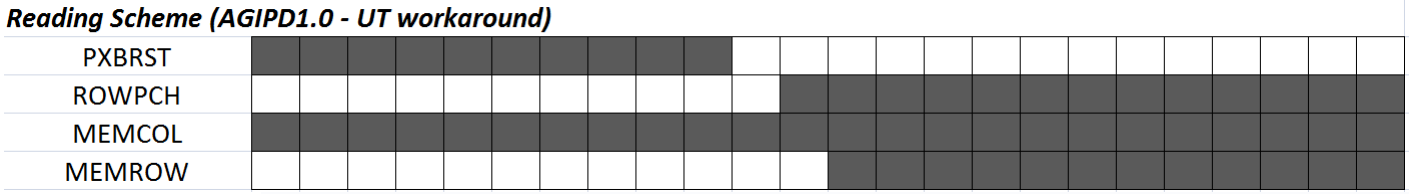


Reason: Resistive network
-> Solution: Buffering of $V_{ref,COB}$

1. Calibration circuits √
2. ‘Ghosting’ √
3. Digital bits
4. Readout speed
5. Pixel/Memory cell maps

AGIPD1.0: ‘Digital Bits’



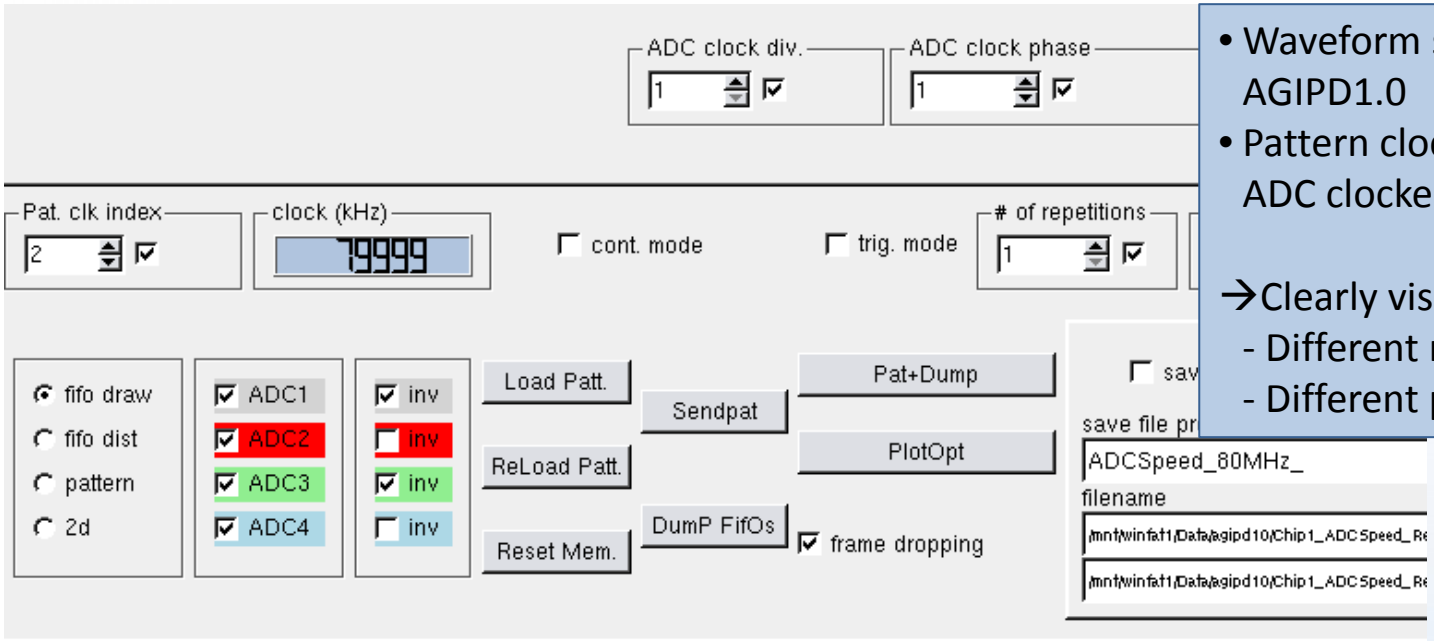


Reason:
- Switching scheme, when connecting the storage cells is different for the 1st row than for the other pixel rows
- Only one switch is open causing a discharge of the signal stored on capacitor
- Temperature sensitivity of storage cells

-> Solution:
- Different readout scheme
- Stable temperature (anyway there for ‘real’ system)

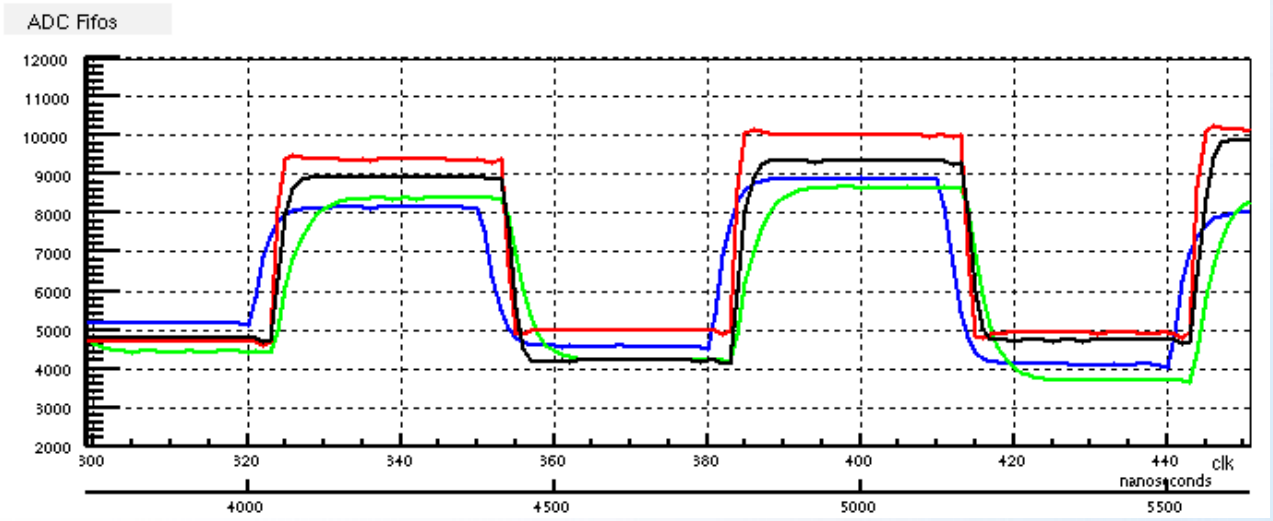
1. Calibration circuits √
2. ‘Ghosting’ √
3. Digital bits √
4. Readout speed
5. Pixel/Memory cell maps

AGIPD1.0: ‘Readout speed’



- Waveform samples of output of AGIPD1.0
- Pattern clocked @40 MHz
  ADC clocked @80 MHz

→Clearly visible are:
- Different risetimes of ADCs
- Different pulseheights



Wirebonds

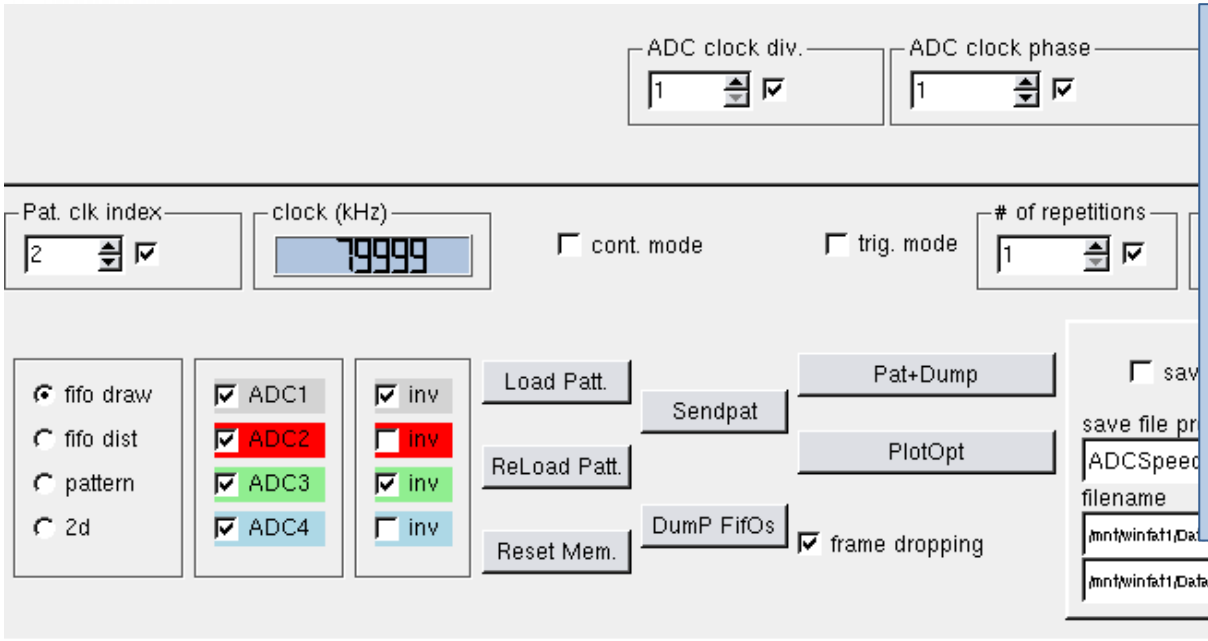
ADC2= Left

ADC1= Center/Left

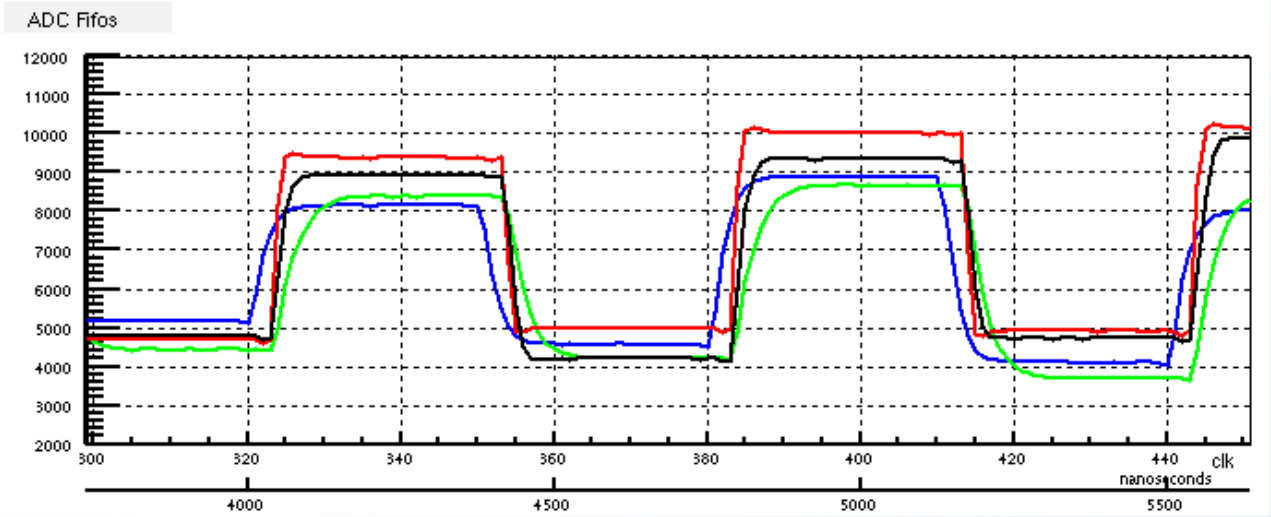
ADC4= Center/Right

ADC3= Right

AGIPD1.0: ‘Readout speed’



- Test of output speed:
  - Injection of high signal by current source into every 2nd column
  - Fitting of exponential for falling/rising waveform of each pixel
  → Extraction of tau (T) and pulse height
- 4 pixel rows tested (1..4)
- Storage cell: 30



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ADC2= Left

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AGIPD1.0: ‘Readout speed’

ADC2= Left

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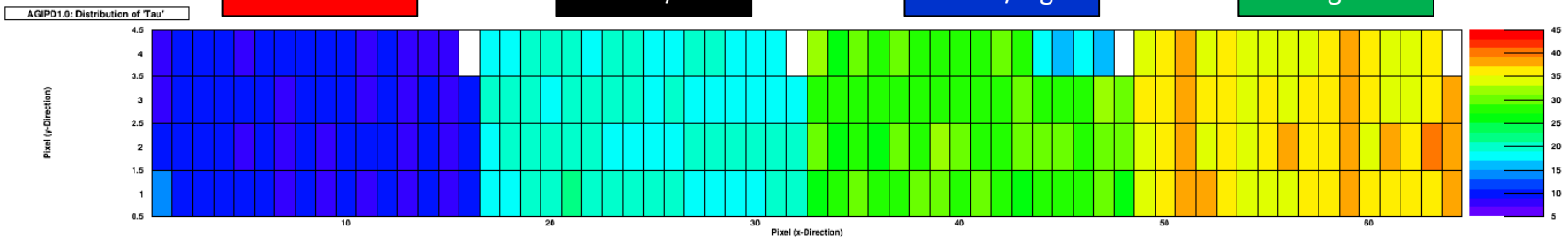
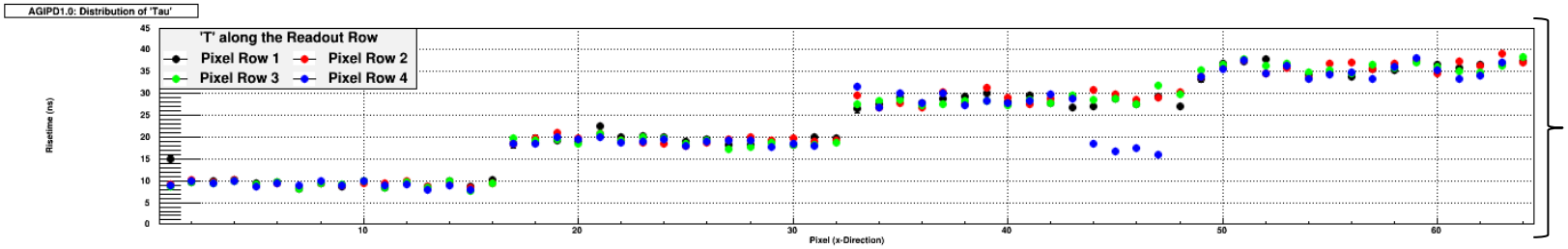
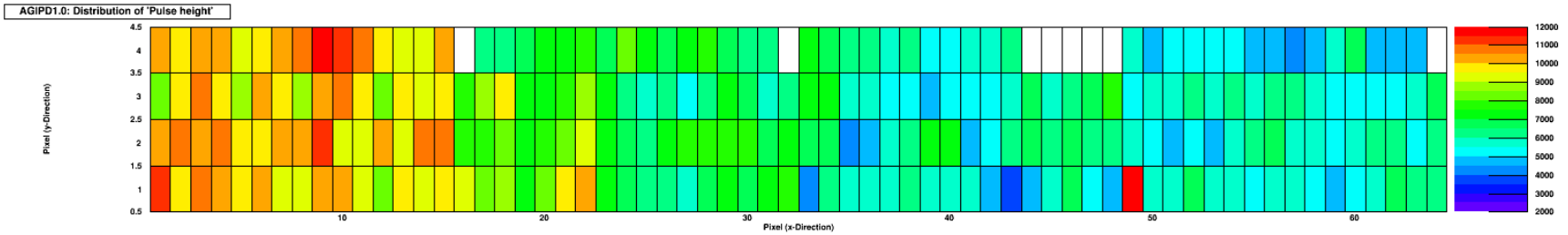
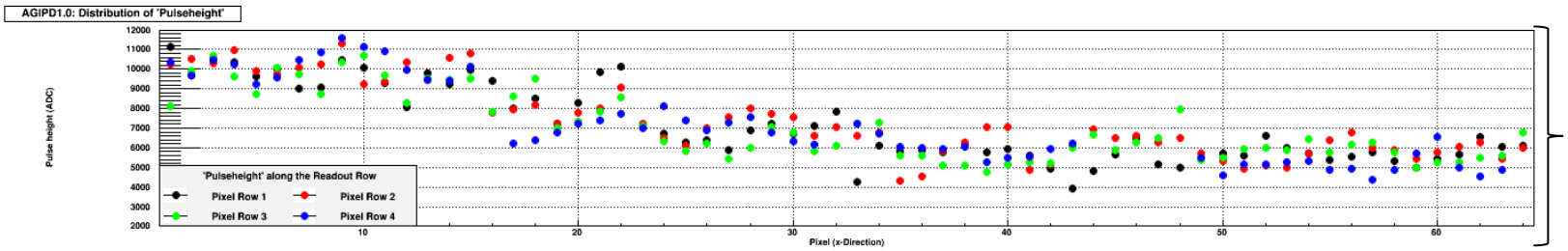




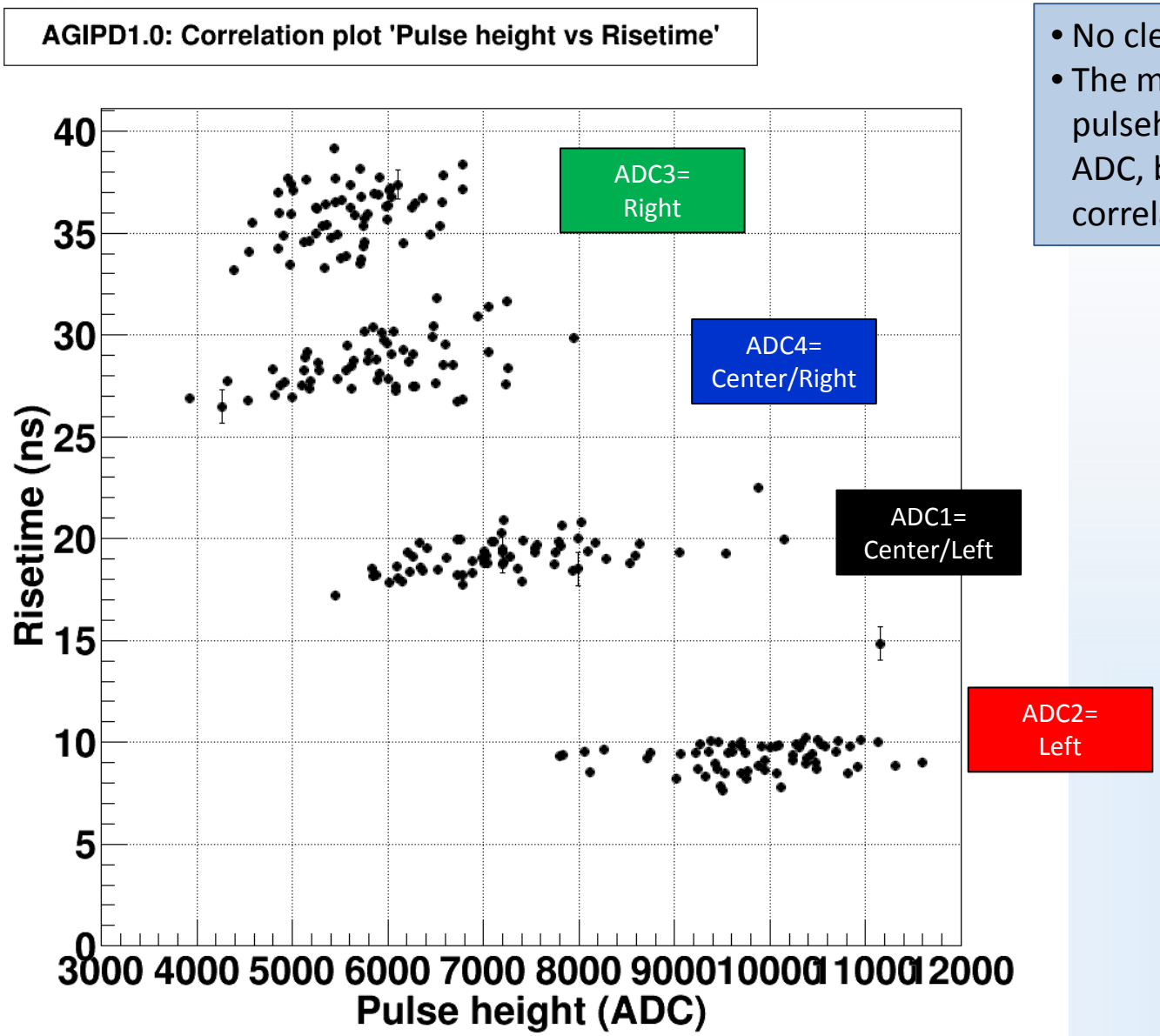
- Tau: 10 .. 40 ns
- Tau depends on ADC





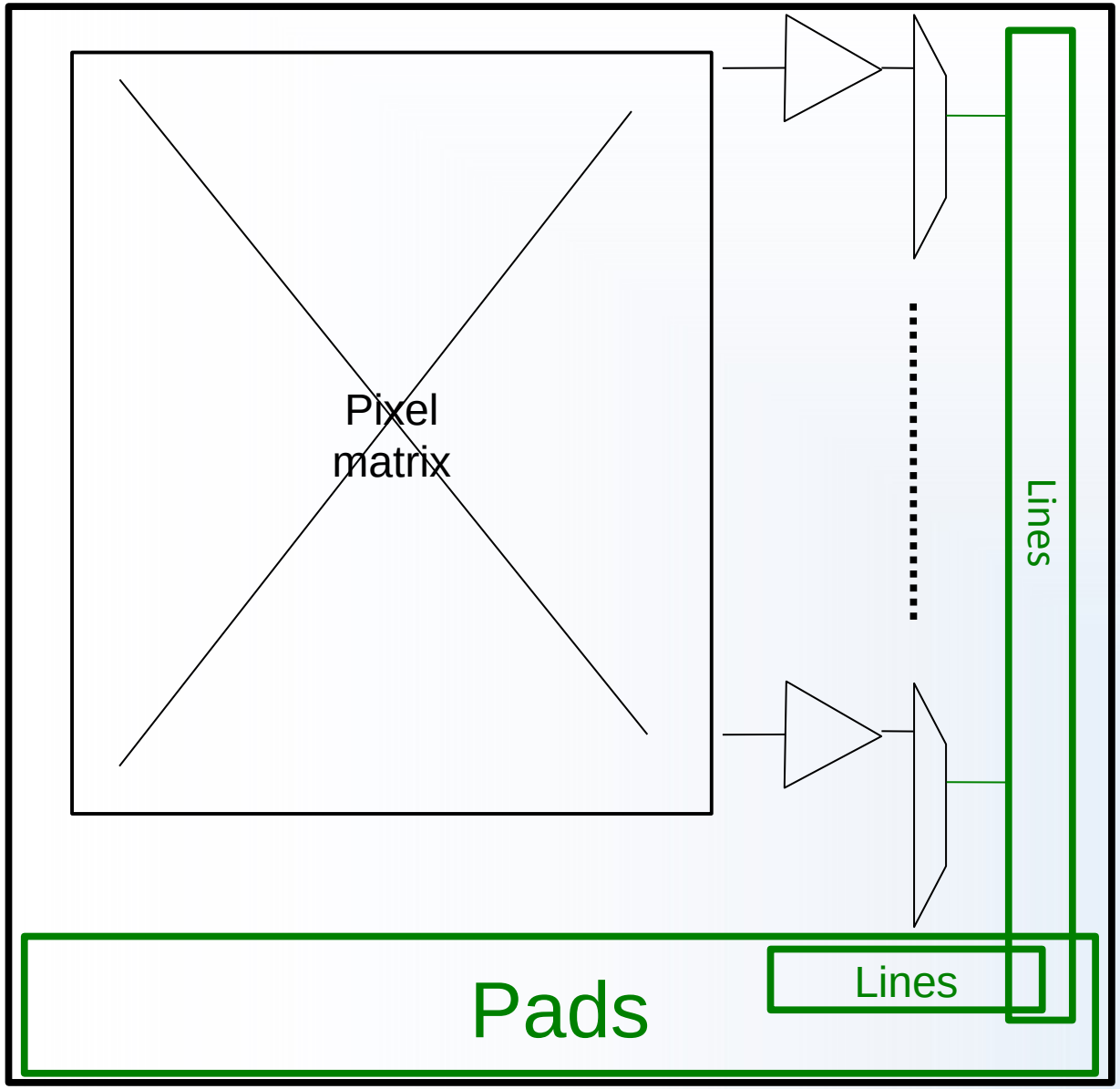
- Pulseheight seems to depend on ADC
- Pure qualitatively !

AGIPD1.0: ‘Readout speed’



- No clear correlation!
- The minimum/maximum pulseheight depends on the ADC, but it doesn’t seem to be correlated with Tau

AGIPD1.0: ‘Readout speed’



Simulations:

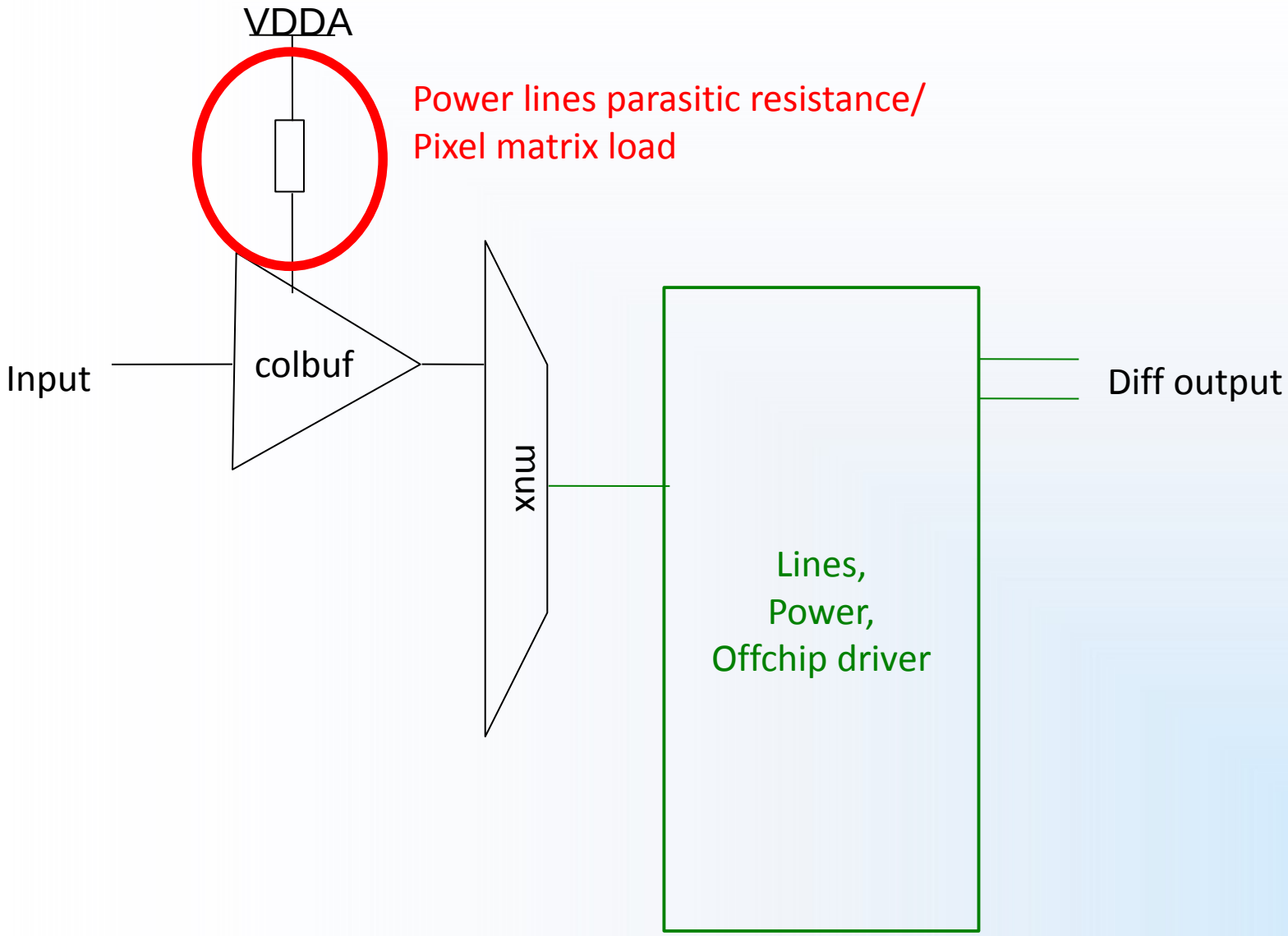
Extracted parasitics of:
- Signal lines
- Pads with offchip driver
- Power nets outside of pixel matrix

Schematic:
- Column buffer
- Output multiplexer with transmission gates

Outcome:

Verification of the **variations/ratio of the readout speed possible,** …but in overall simulations show **much faster behavior**

AGIPD1.0: ‘Readout speed’



AGIPD1.0: ‘Readout speed’

Reason:
- Different RCs for different routes offchip
- Bad connection of Column Buffer

-> Solution:
- Matching RCs
- Improving layout

① Calibration circuits √

② ‘Ghosting’ √

③ Digital bits √

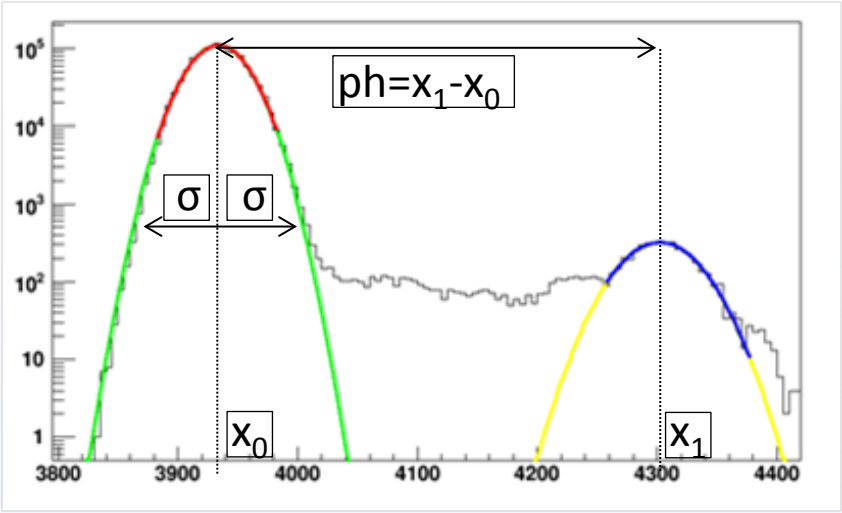
④ Readout speed √

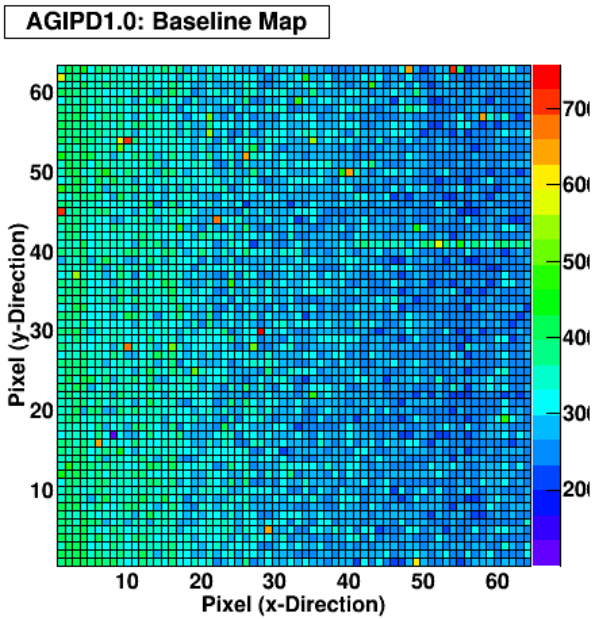
⑤ Pixel/Memory cell maps

AGIPD1.0: ‘Readout speed -> Maps’

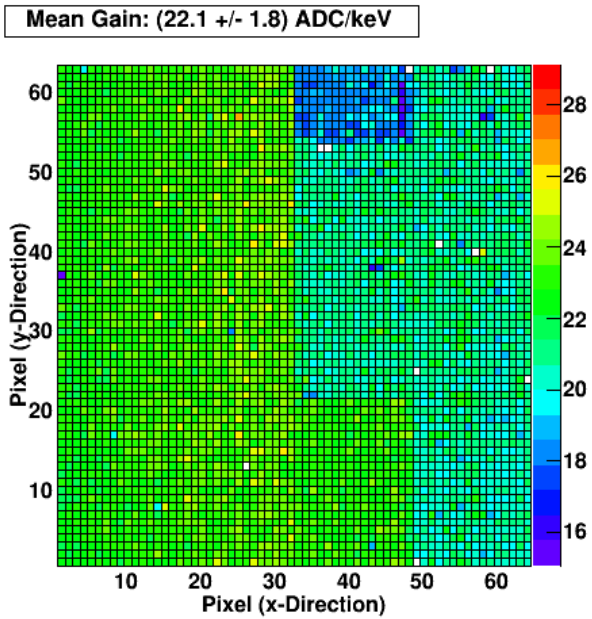
- Filling each memory cell **with fluorescence photons (Mo 17.5 keV)** with **10 µs integration time**
- Extracting:
  - Pulseheight**: ph = $x_1 - x_0$**
  - Baseline: **x_0**
  - Noise: **σ** (@ 200 ns integration time)
- Chip operated @ 80 MHz → 40 MHz on-chip (25 ns)
- Readout: Sampling after **150 ns (ADC @ 5 MHz)**

Readout at **10 MHz (Sampling after 75 ns)**

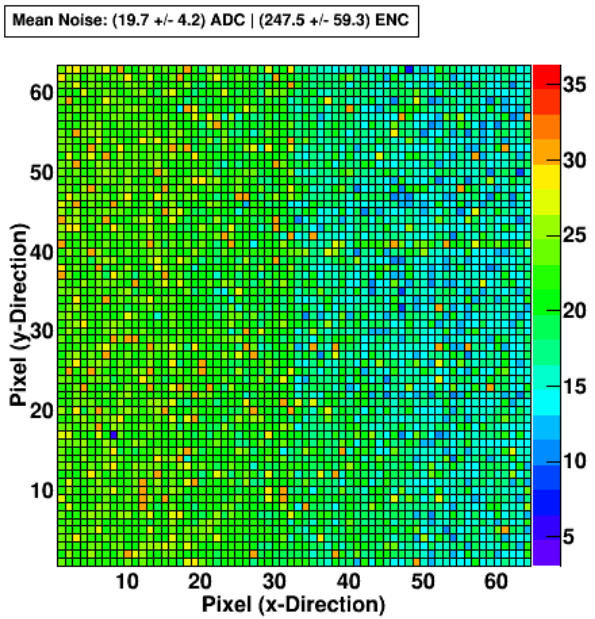




Baseline

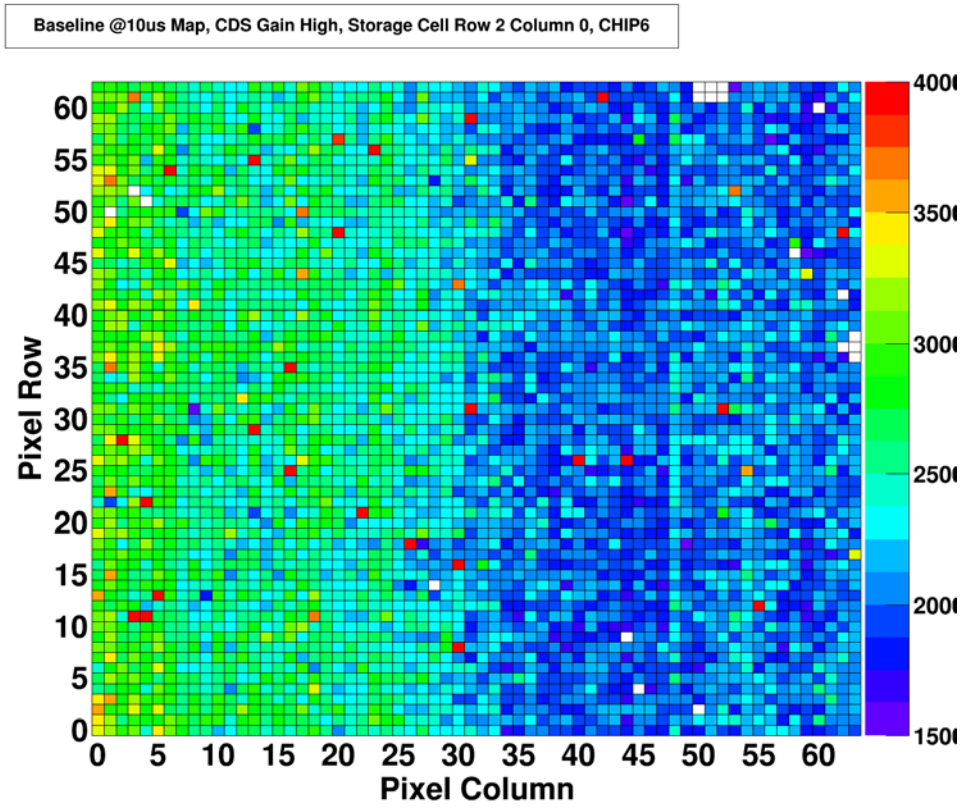


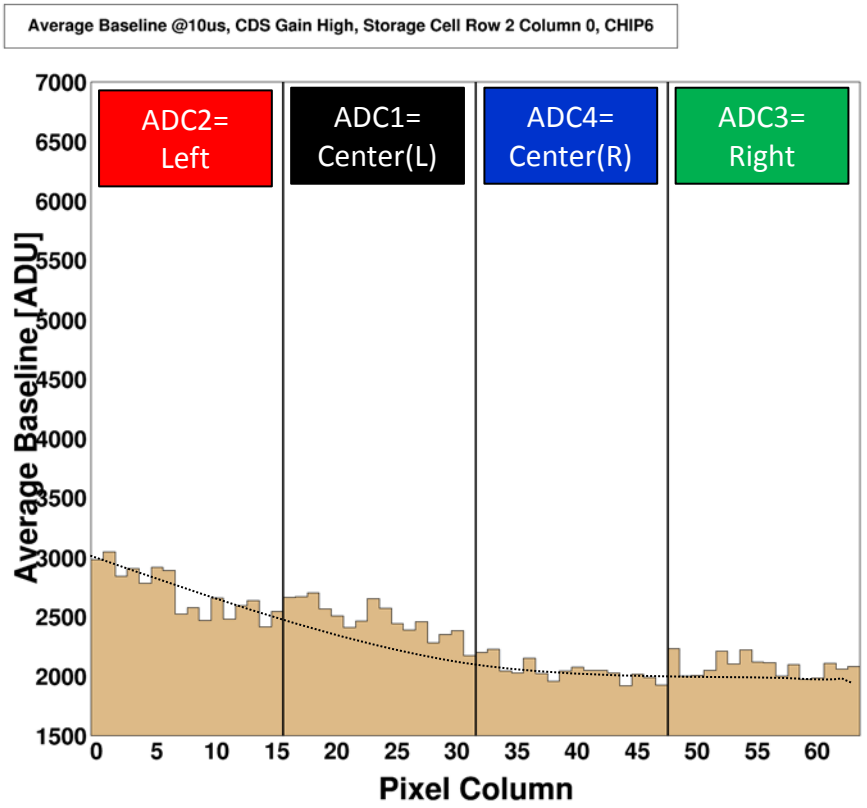
Gain



Noise

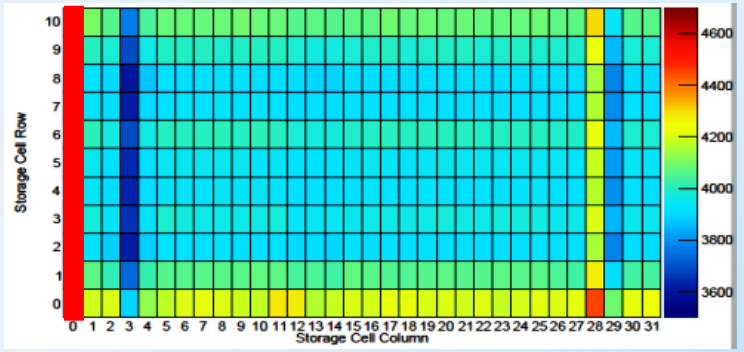
AGIPD1.0: ‘Pixel maps: Baseline’



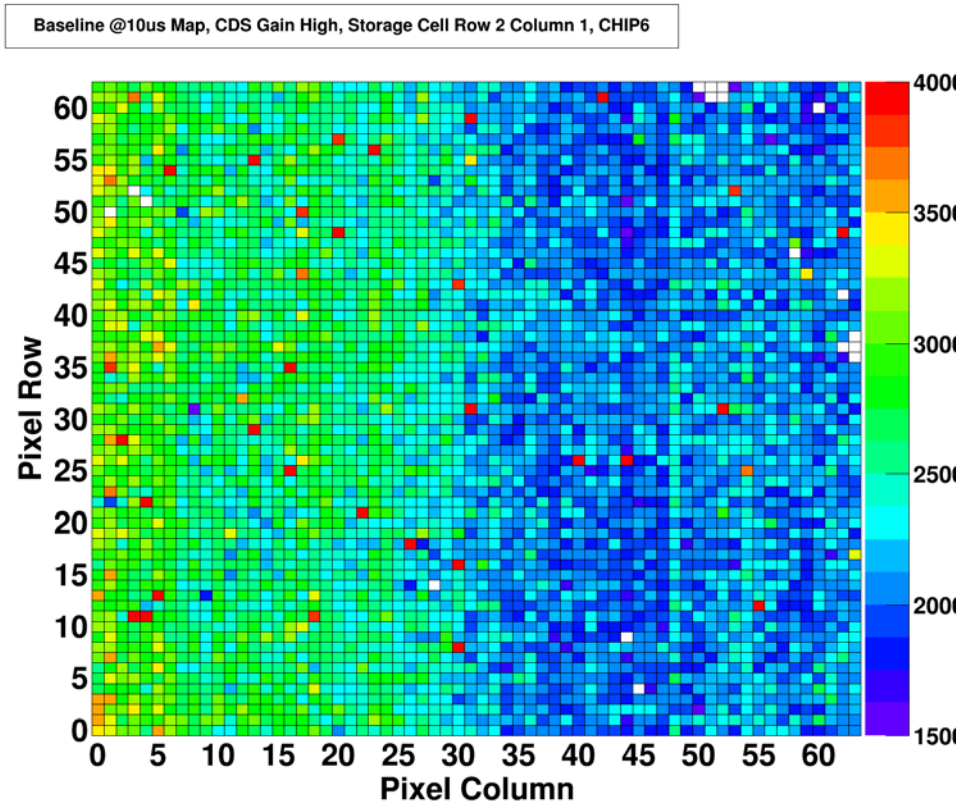


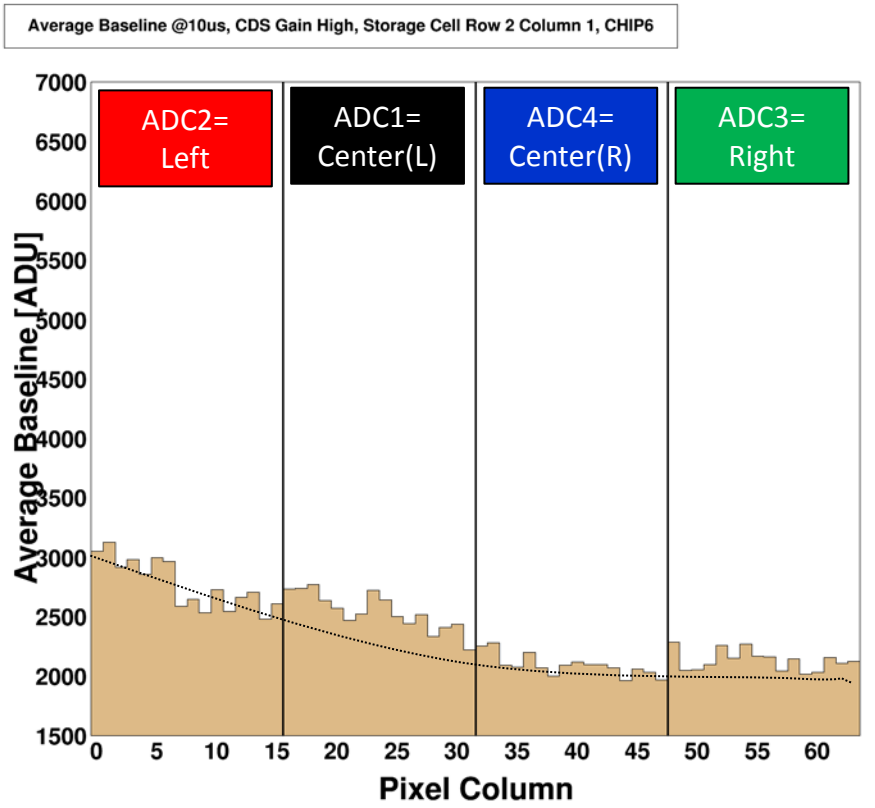
Readout at **5 MHz**
Integration time: **10 µs**

Memory cell: **64**
Row: 2 | Col: **0**



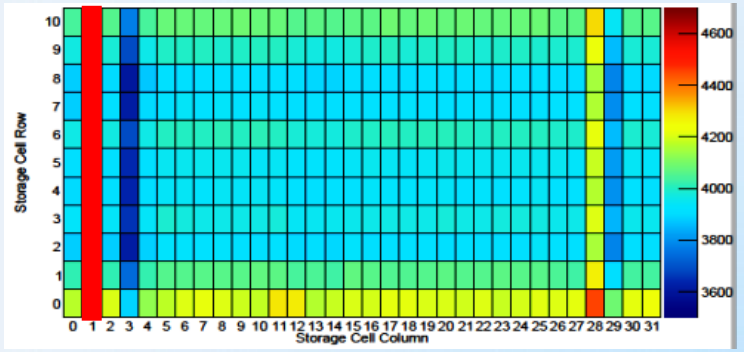
AGIPD1.0: ‘Pixel maps: Baseline’



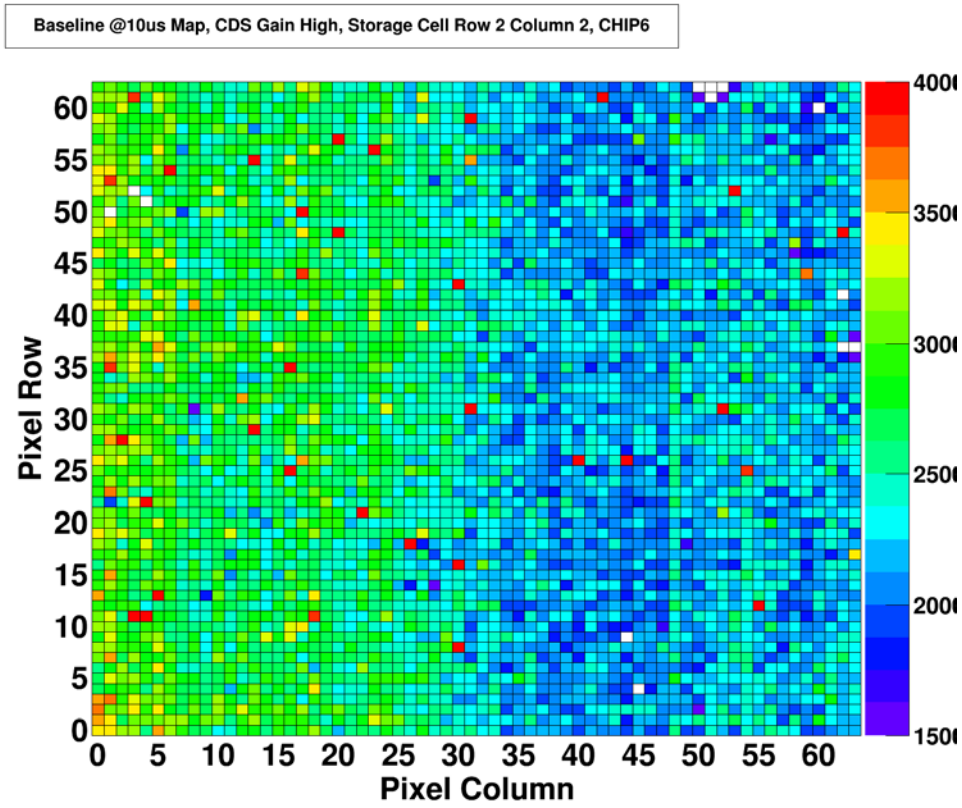


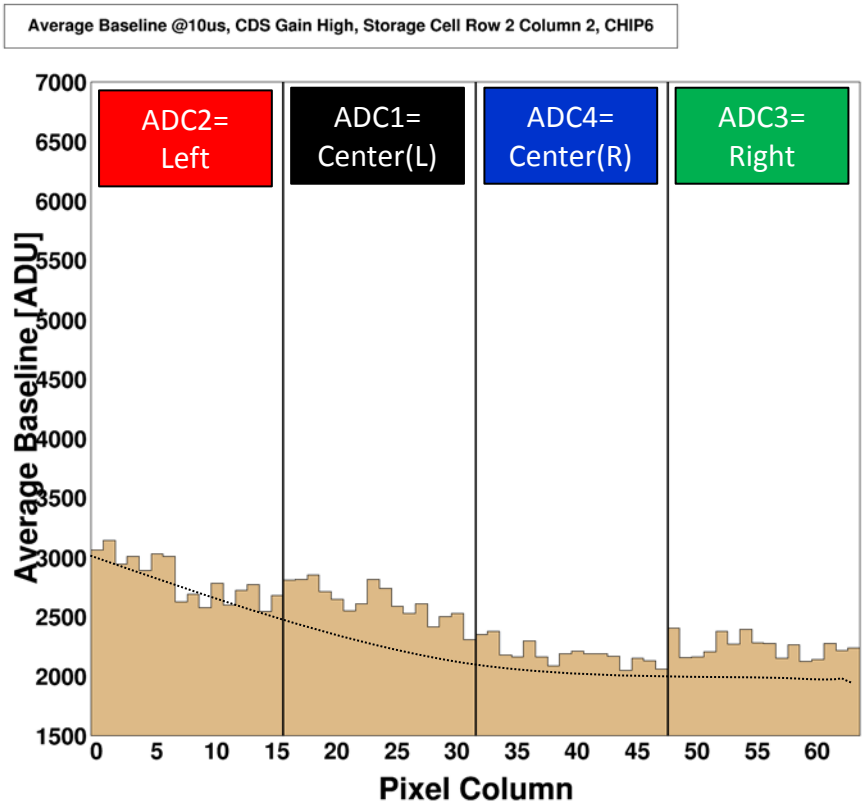
Readout at **5 MHz**
Integration time: **10 µs**

Memory cell: **65**
Row: 2 | Col: **1**



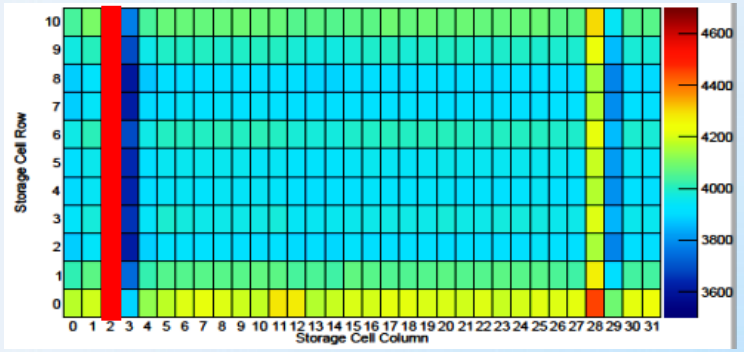
AGIPD1.0: ‘Pixel maps: Baseline’



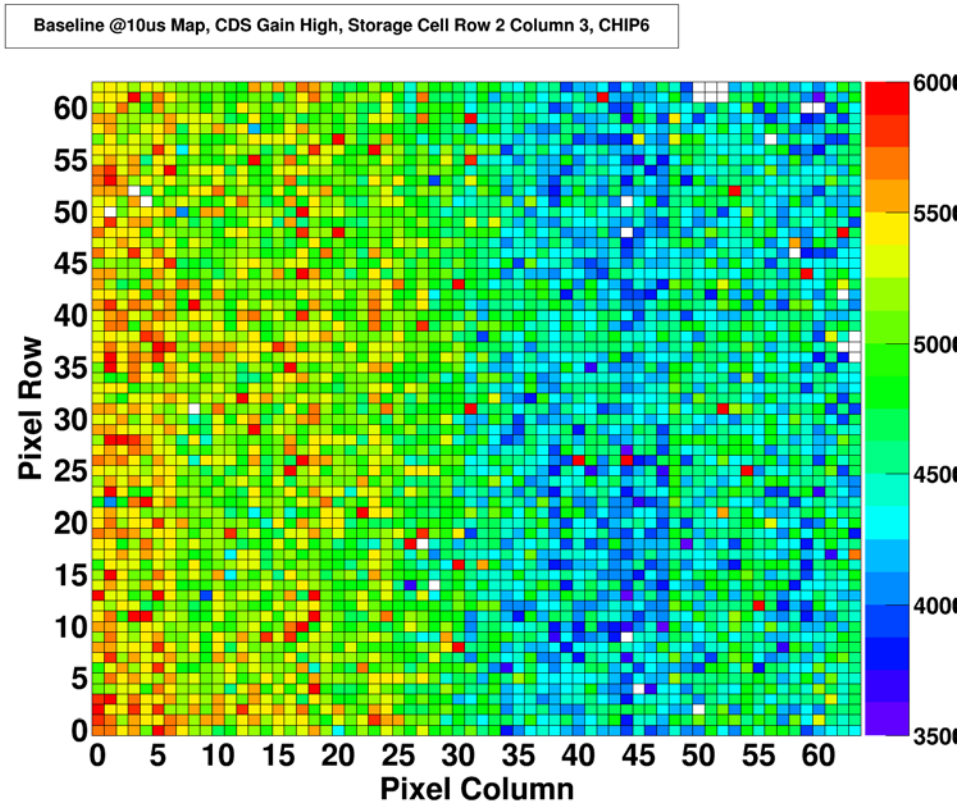


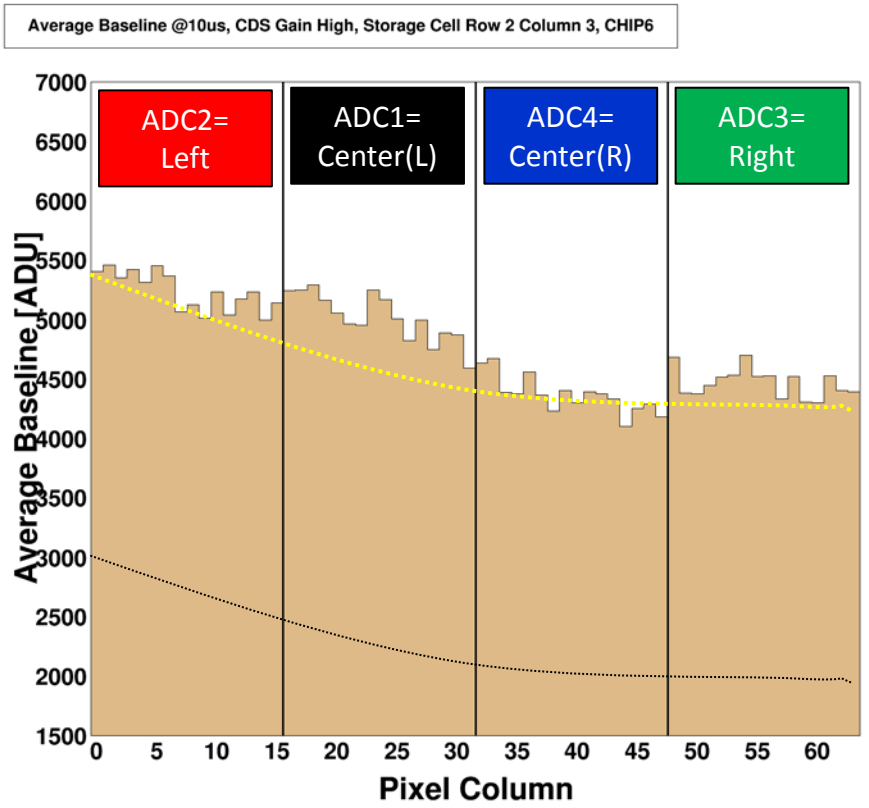
Readout at **5 MHz**
Integration time: **10 µs**

Memory cell: **66**
Row: 2 | Col: **2**



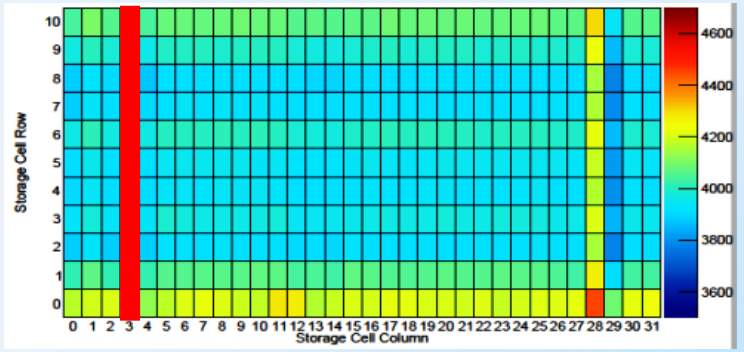
AGIPD1.0: ‘Pixel maps: Baseline’



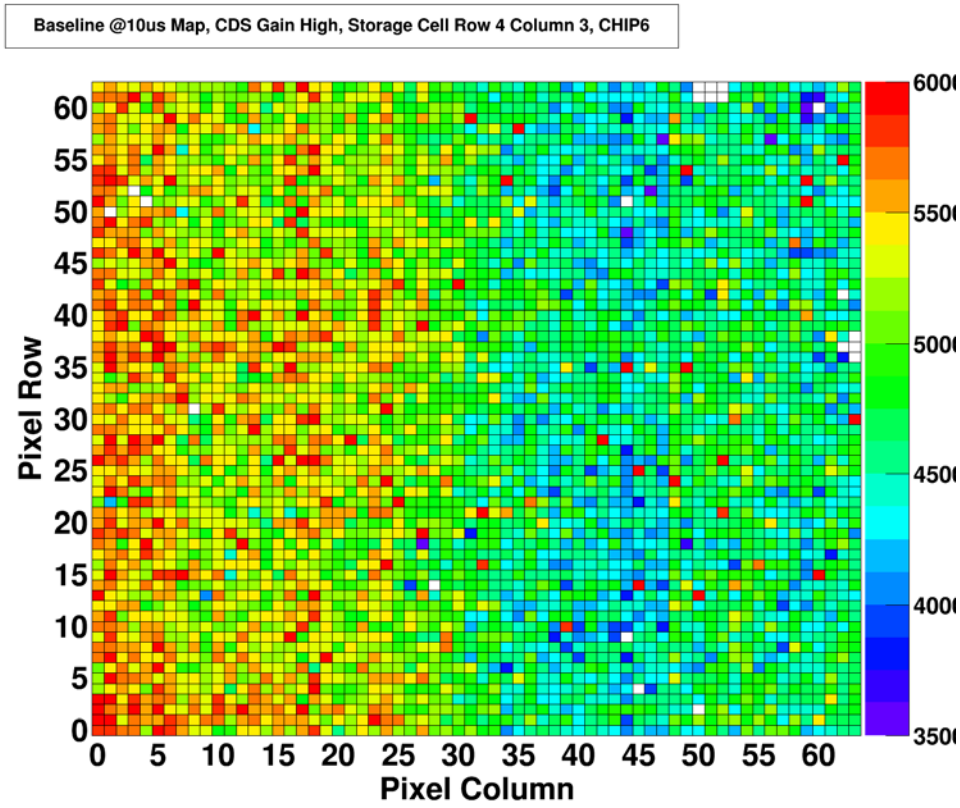


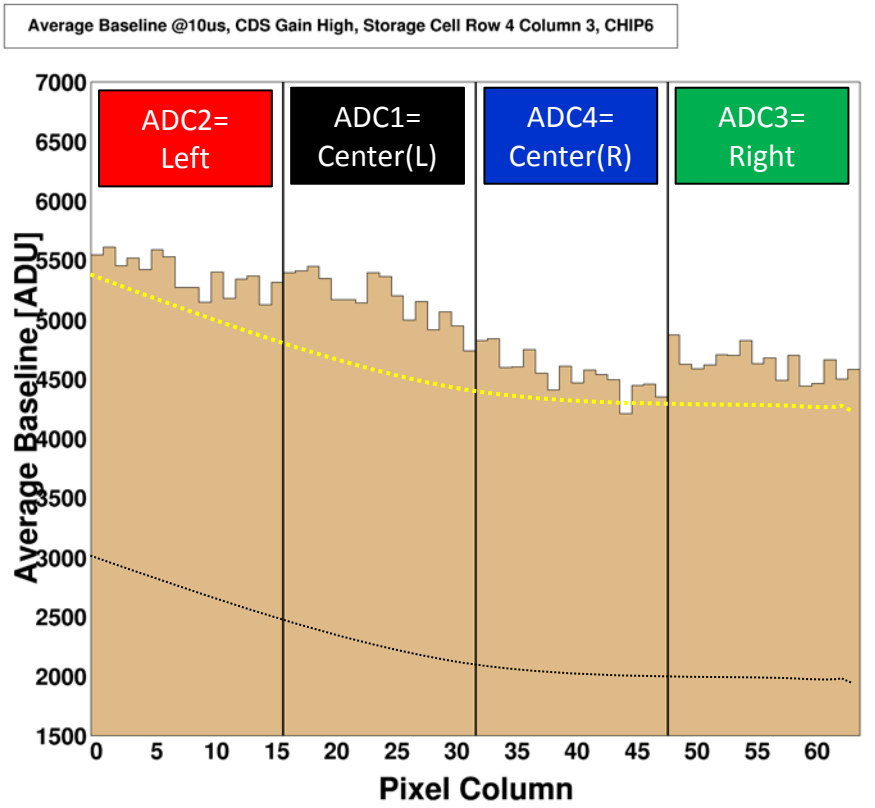
Readout at **5 MHz**
Integration time: **10 µs**

Memory cell: **67**
Row: 2 | Col: **3**



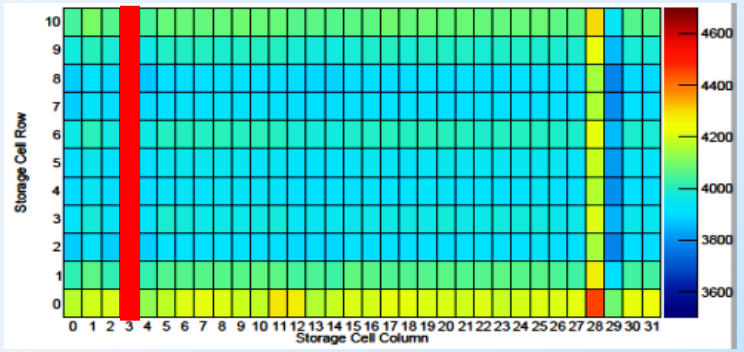
AGIPD1.0: ‘Pixel maps: Baseline’



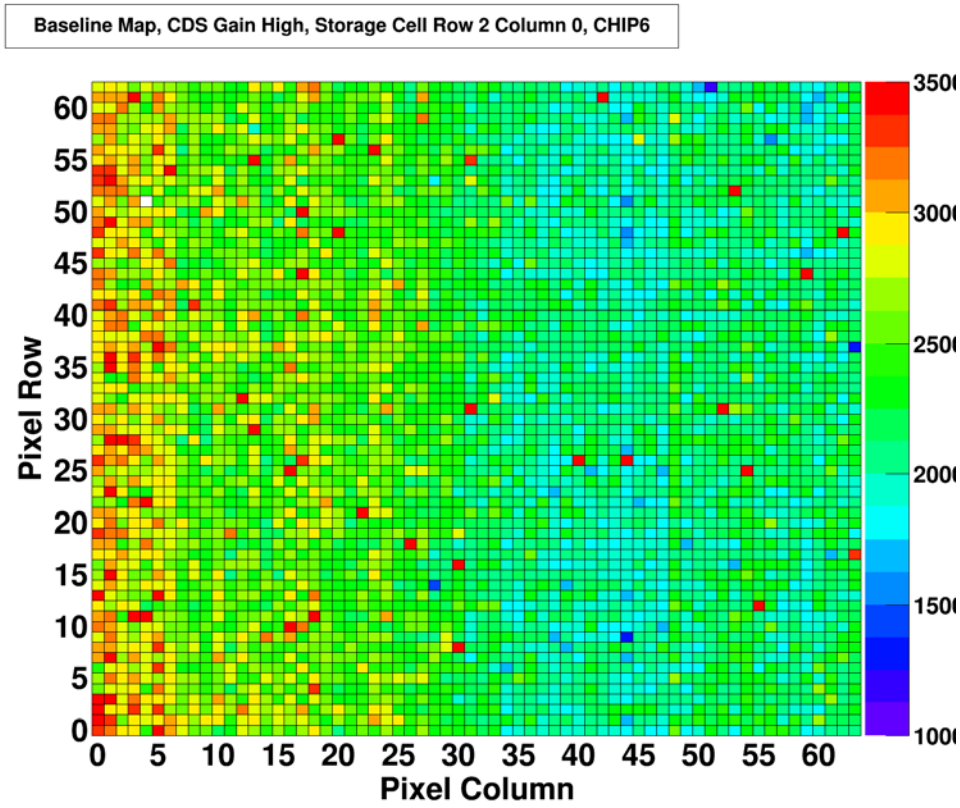


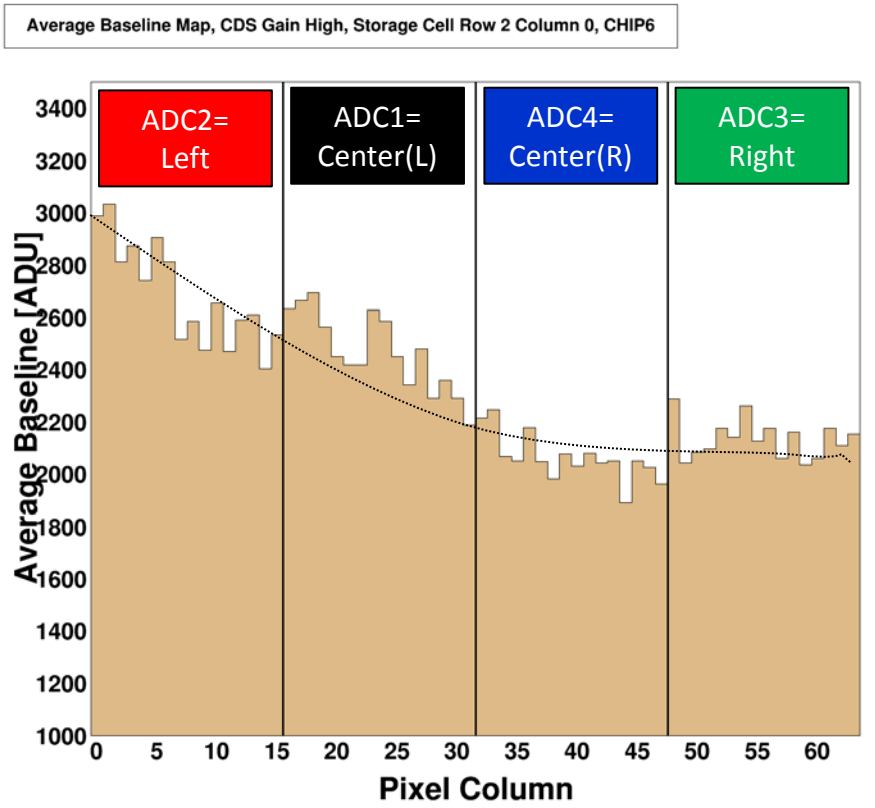
Readout at **5 MHz**
Integration time: **10 µs**

Memory cell: **131**
Row: 4 | Col: **3**



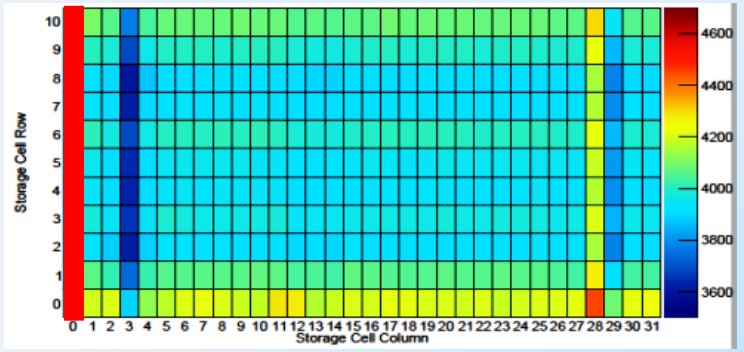
AGIPD1.0: ‘Pixel maps: Baseline’



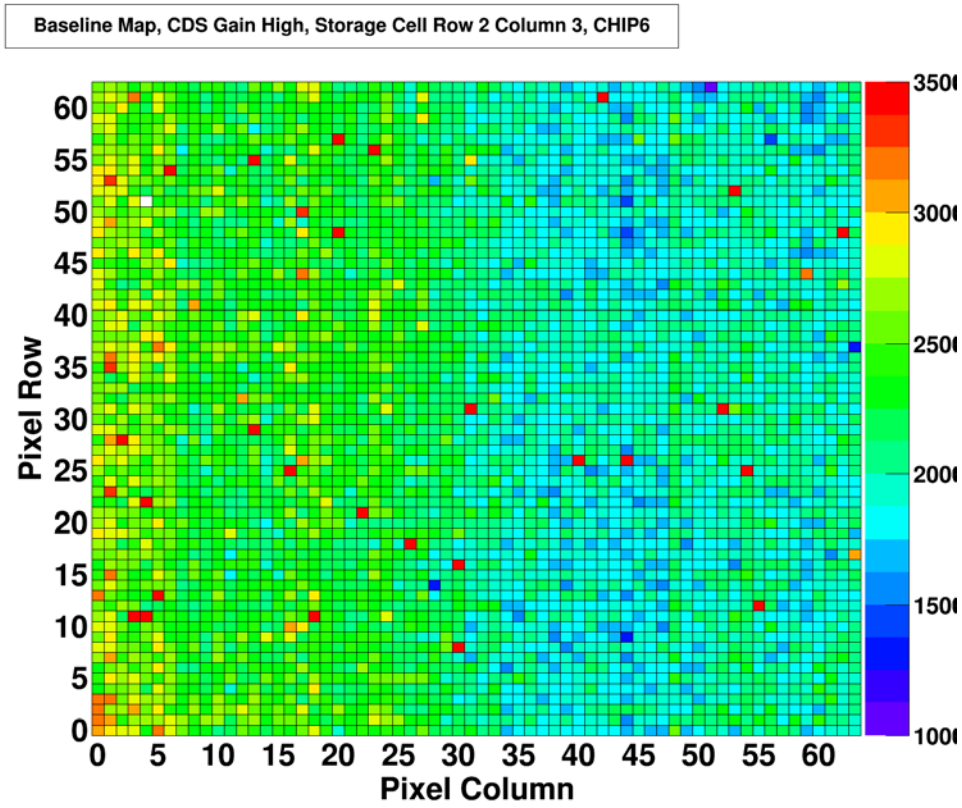


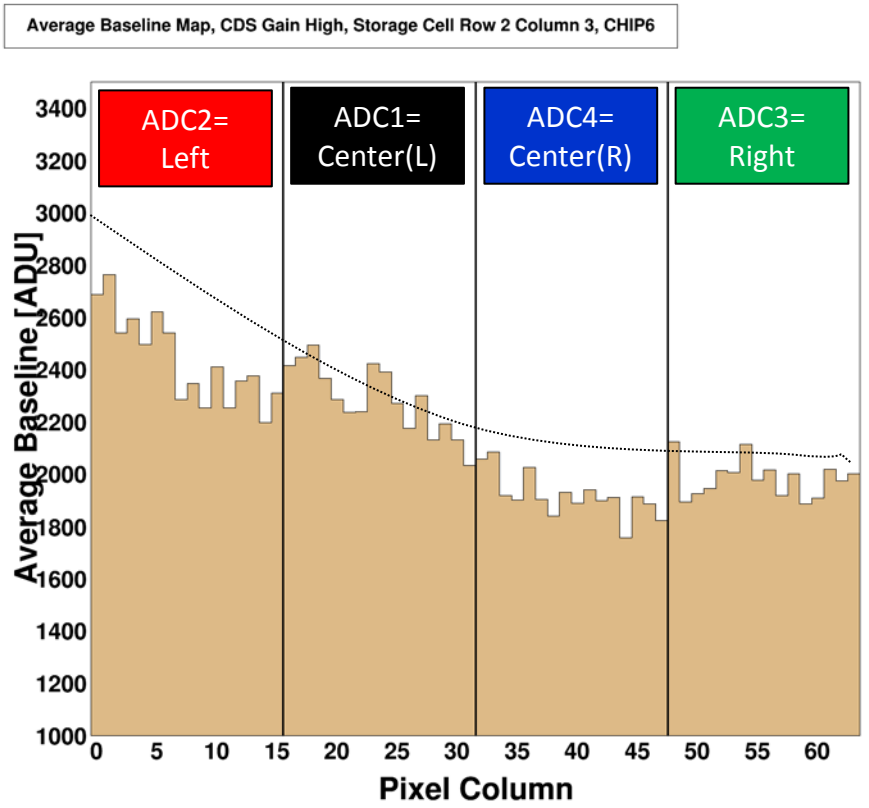
Readout at **5 MHz**
Integration time: **200 ns**

Memory cell: **64**
Row: 2 | Col: **0**



AGIPD1.0: ‘Pixel maps: Baseline’

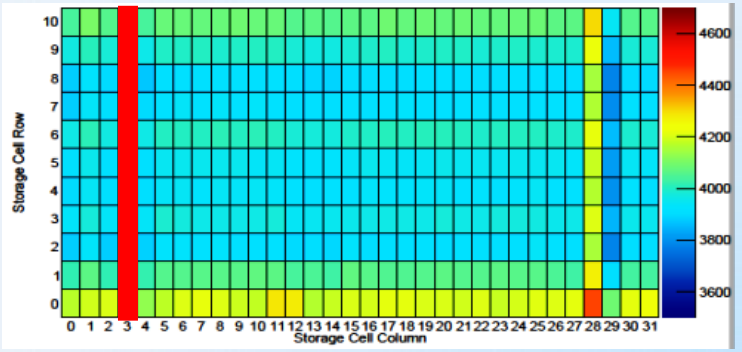




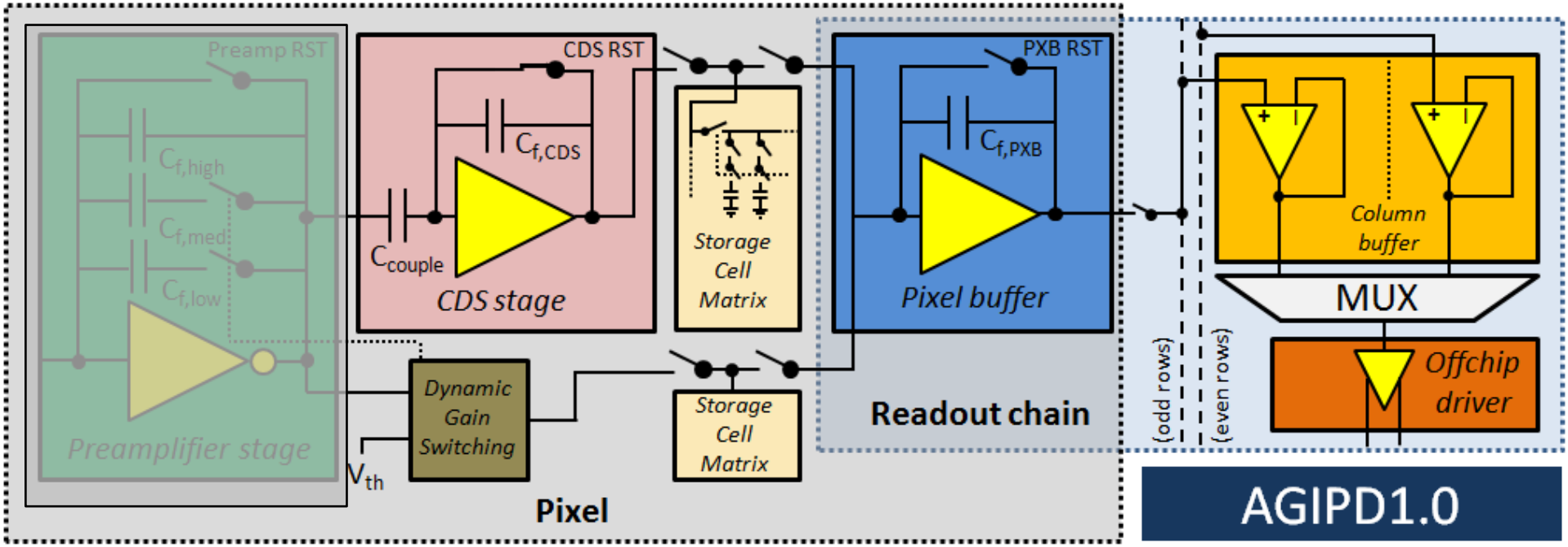
Readout at **5 MHz**
Integration time: **200 ns**

Memory cell: **67**
Row: 2 | Col: **3**

Problem: Strong change of baseline with integration time for memory cell column 3



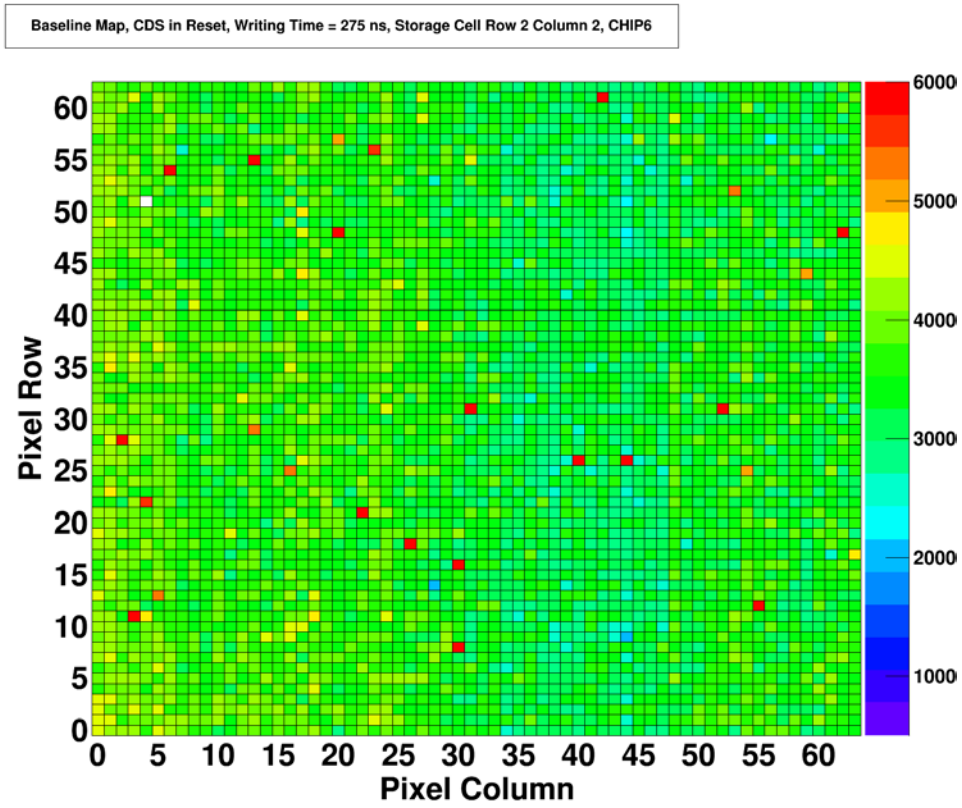
AGIPD1.0: ‘Pixel maps: Baseline’

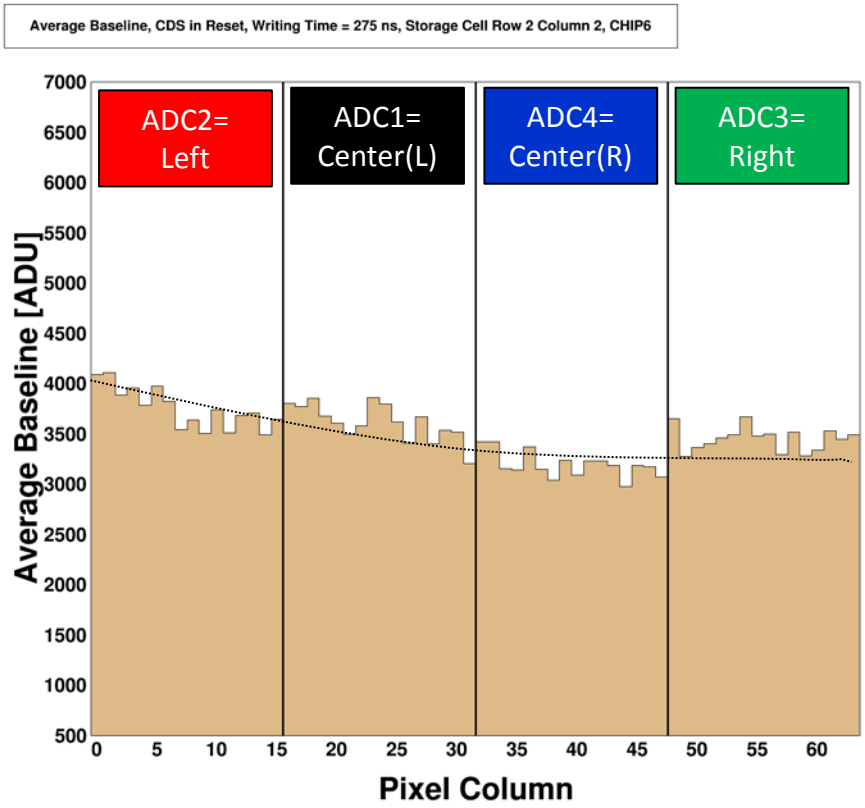


- Identify the origin of this change of baseline
- **CDS buffer in RESET**
- **Acquire baseline** for **$V_{ref,CDS}$= 700 mV**
- Use **different writing times**

-> Baseline should be stable

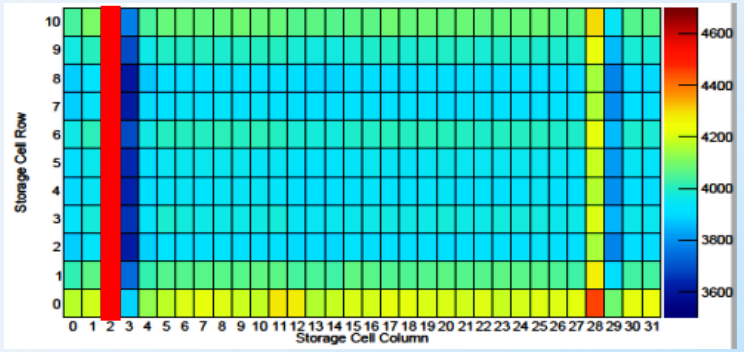
AGIPD1.0: ‘Pixel maps: Baseline’



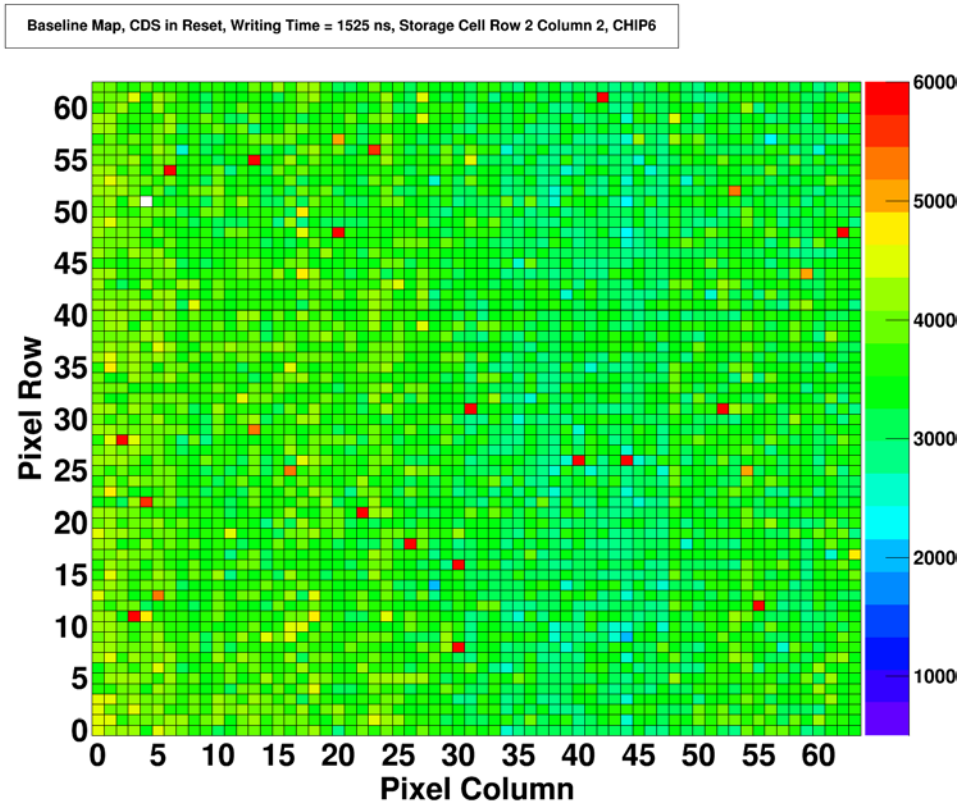


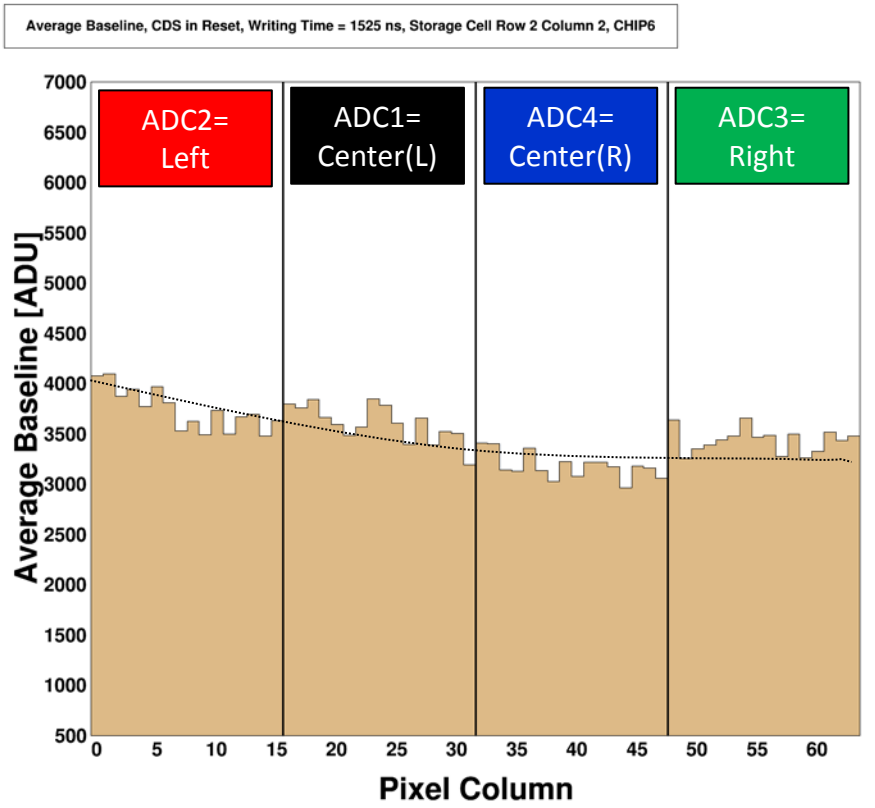
Readout at **5 MHz**
Integration time: **275 ns**

Memory cell: **66**
Row: 2 | Col: **2**



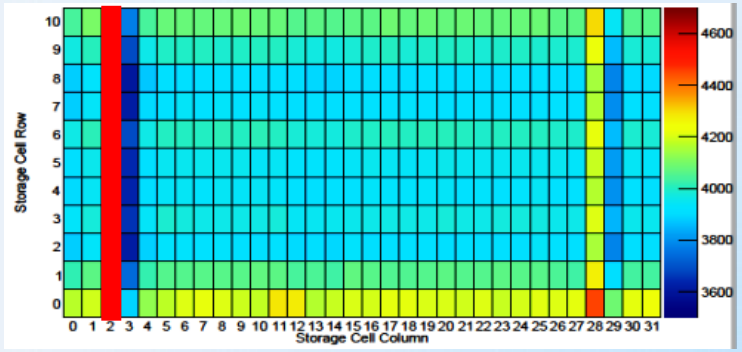
AGIPD1.0: ‘Pixel maps: Baseline’



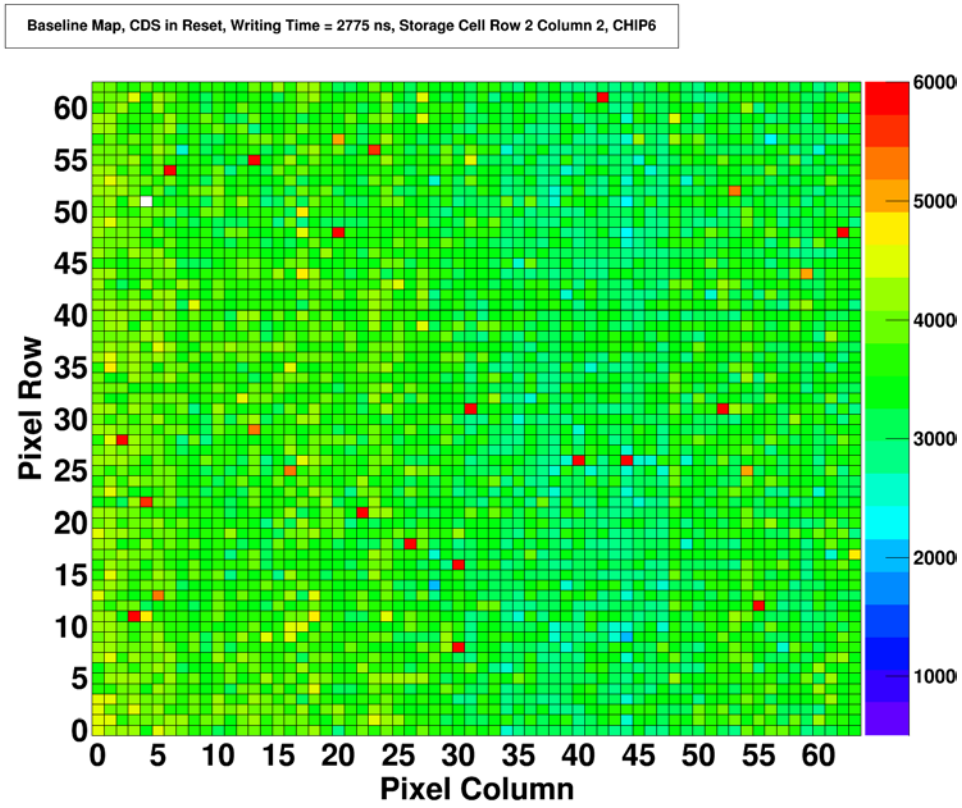


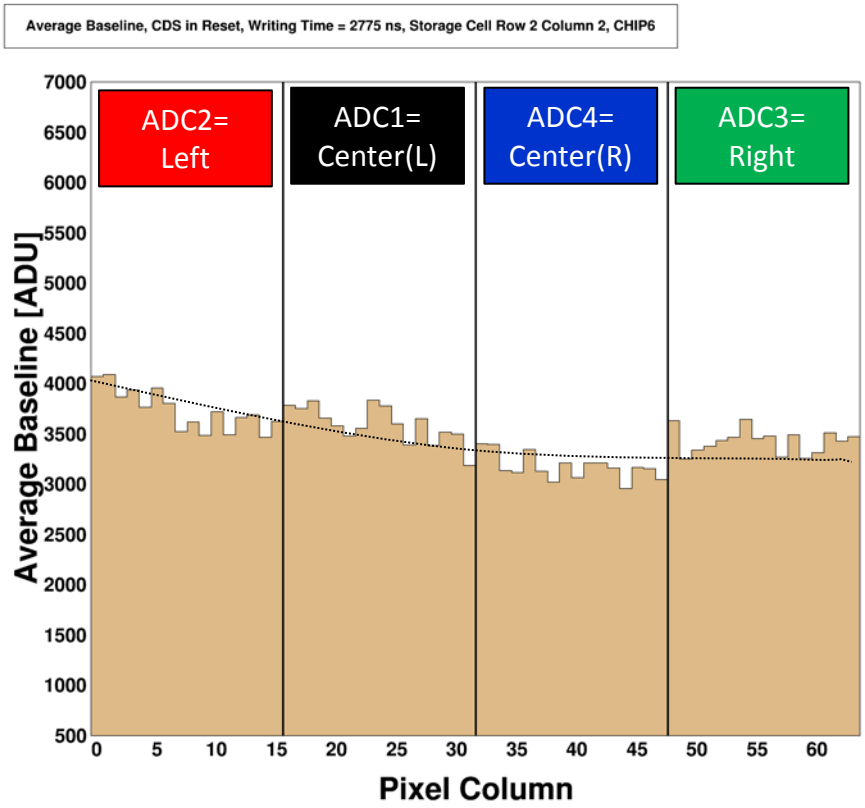
Readout at **5 MHz**
Integration time: **1.5 µs**

Memory cell: **66**
Row: 2 | Col: **2**



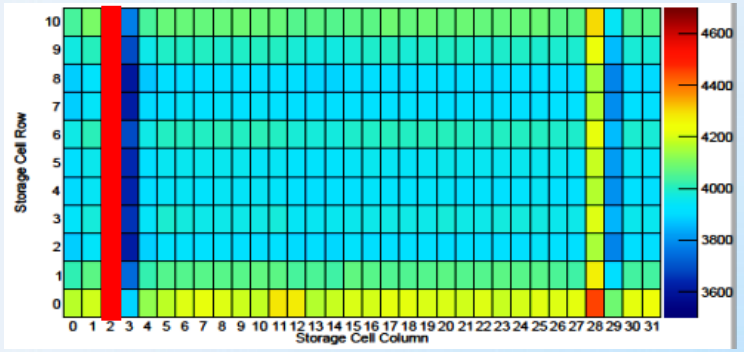
AGIPD1.0: ‘Pixel maps: Baseline’



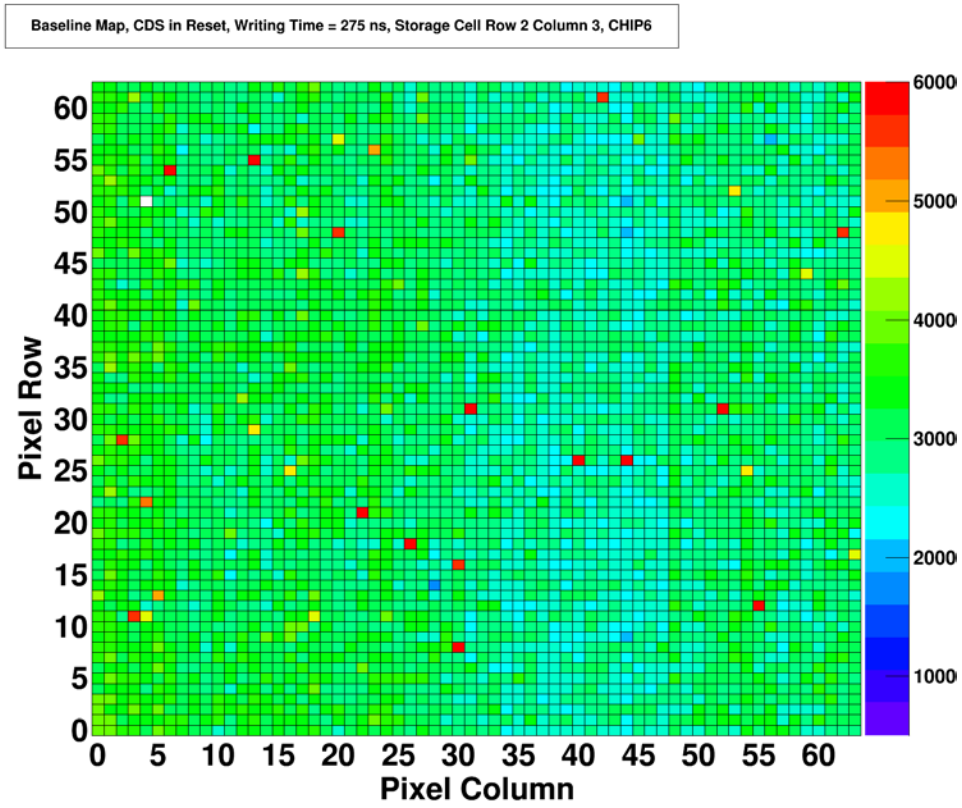


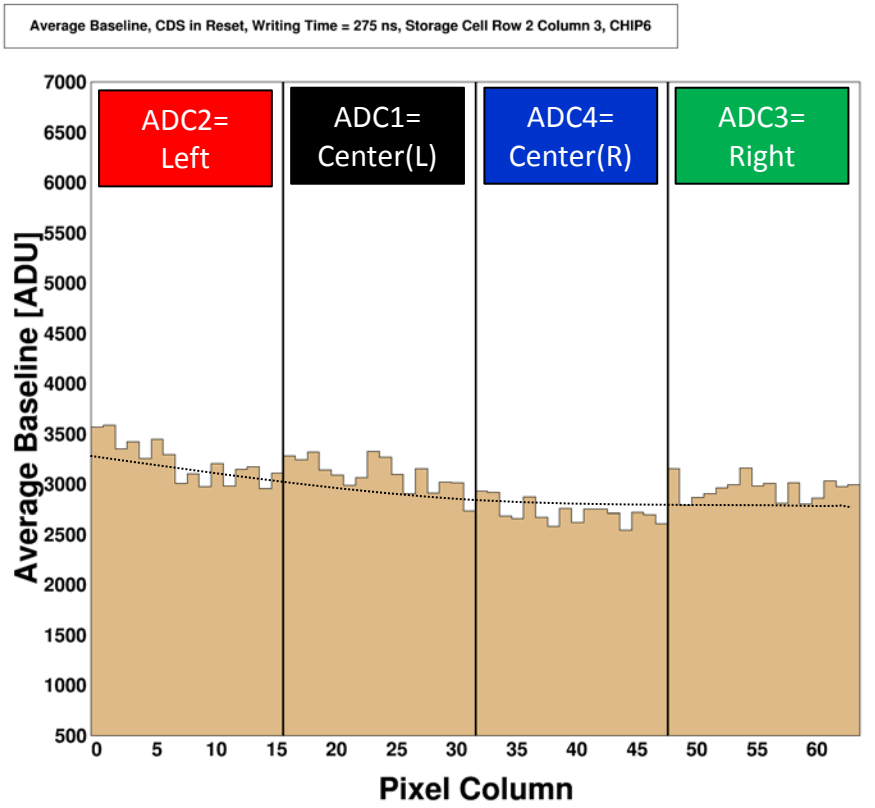
Readout at **5 MHz**
Integration time: **2.3 µs**

Memory cell: **66**
Row: 2 | Col: **2**



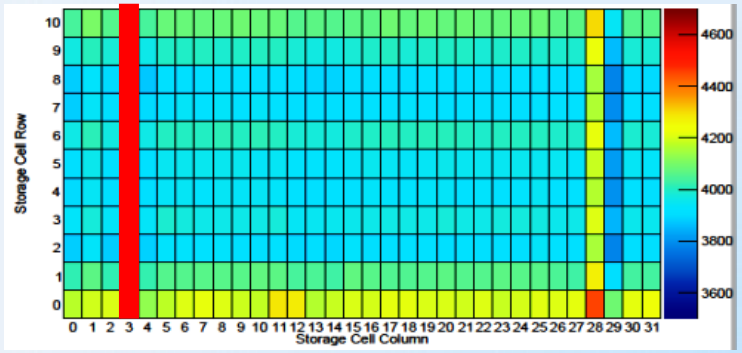
AGIPD1.0: ‘Pixel maps: Baseline’



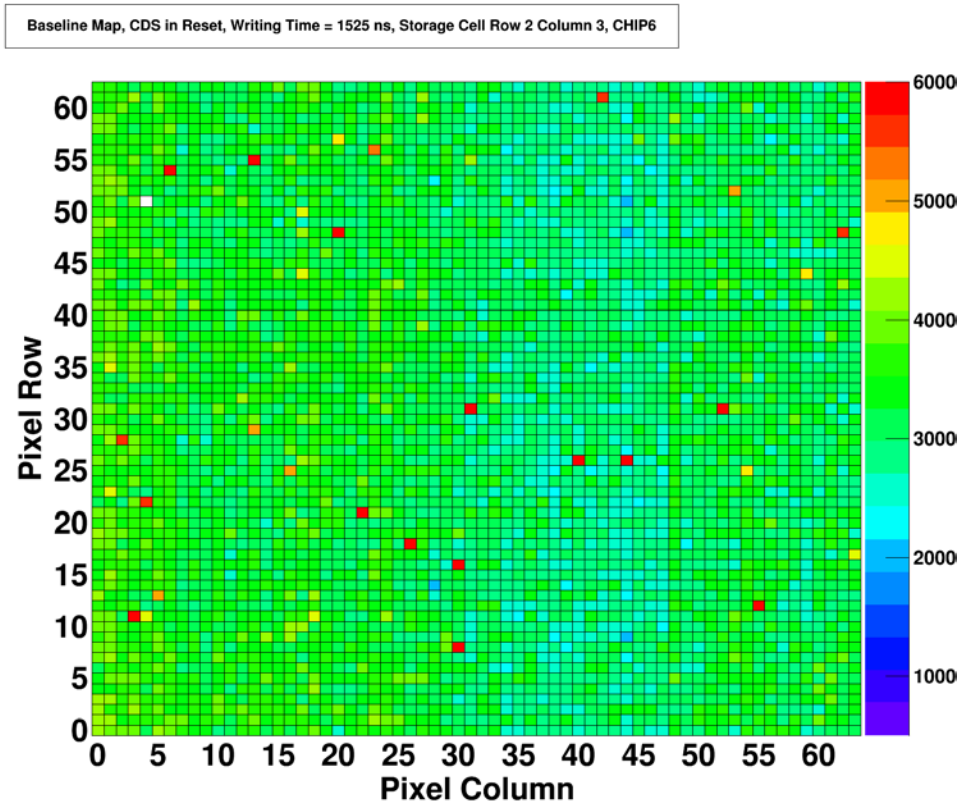


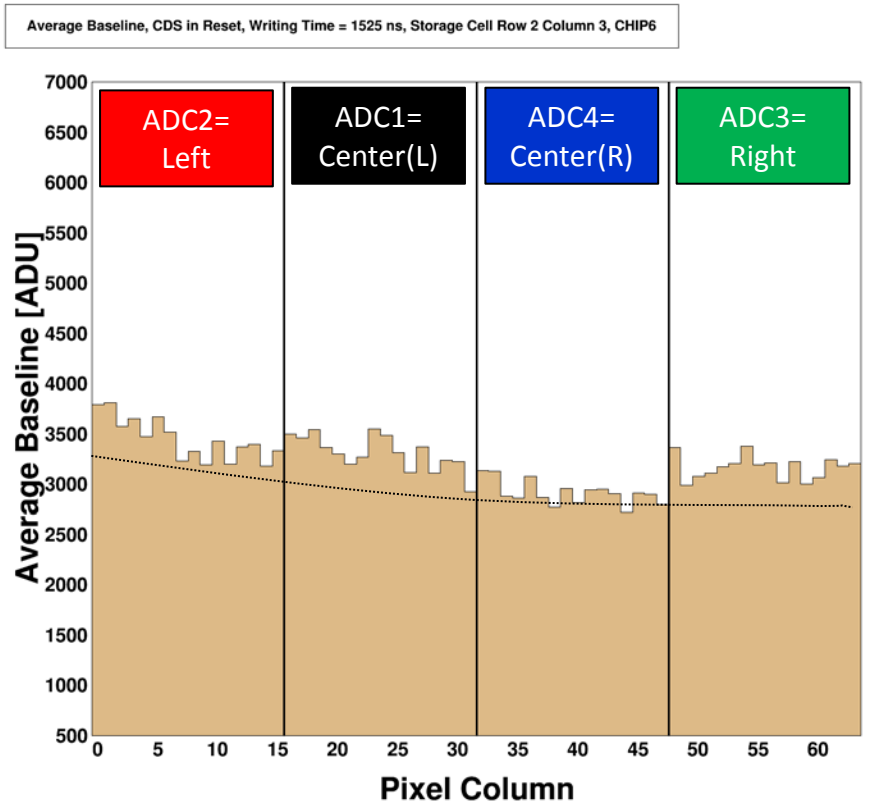
Readout at **5 MHz**
Integration time: **275 ns**

Memory cell: **67**
Row: 2 | Col: **3** ★



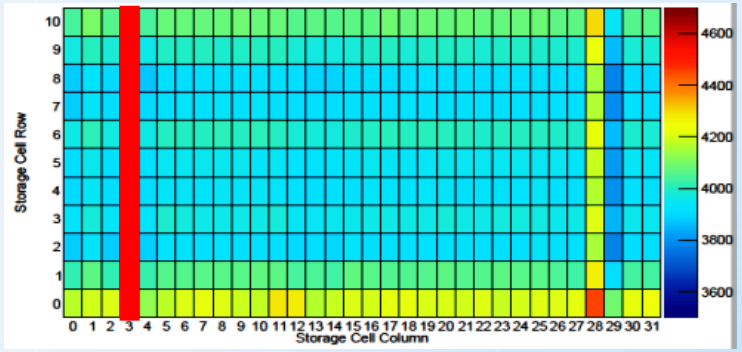
AGIPD1.0: ‘Pixel maps: Baseline’



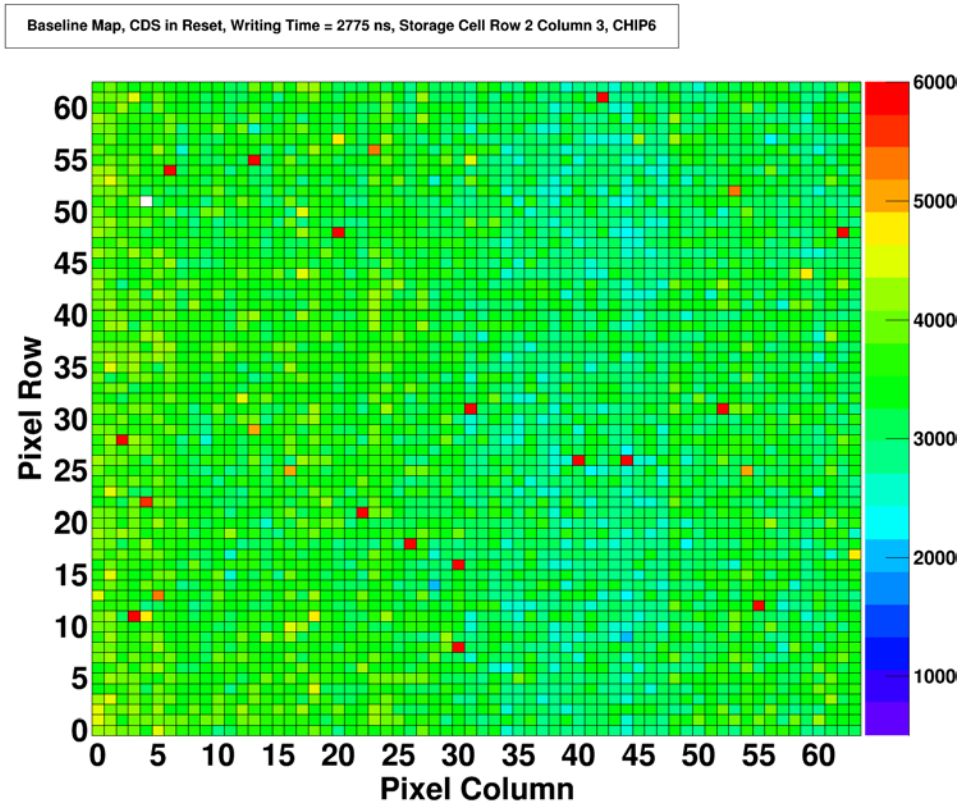


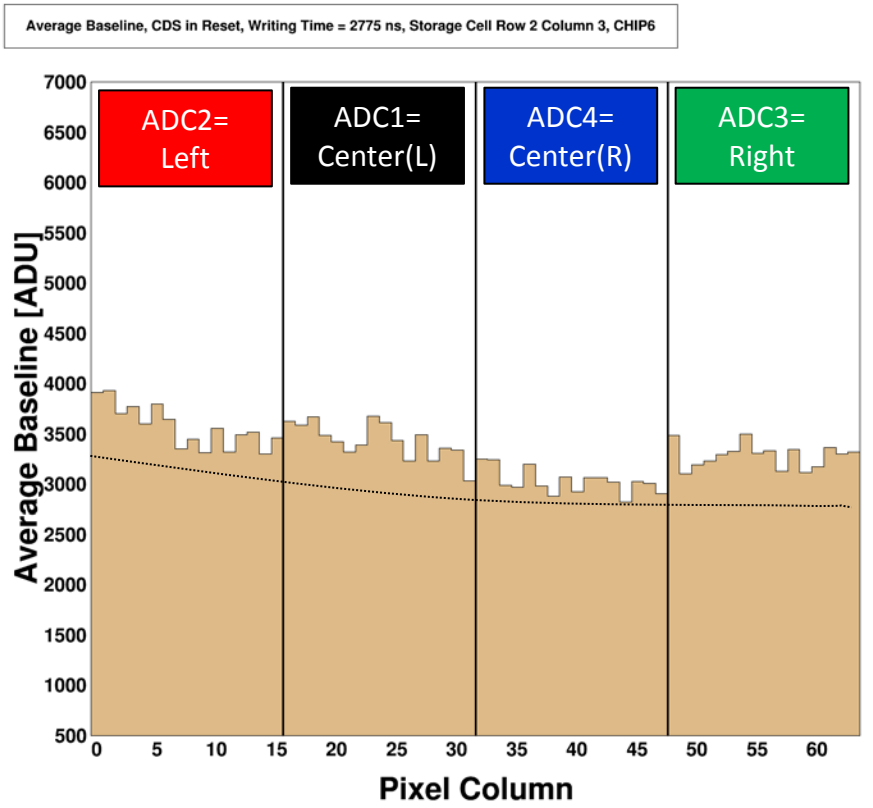
Readout at **5 MHz**
Integration time: **1.5 µs**

Memory cell: **67**
Row: 2 | Col: **3**



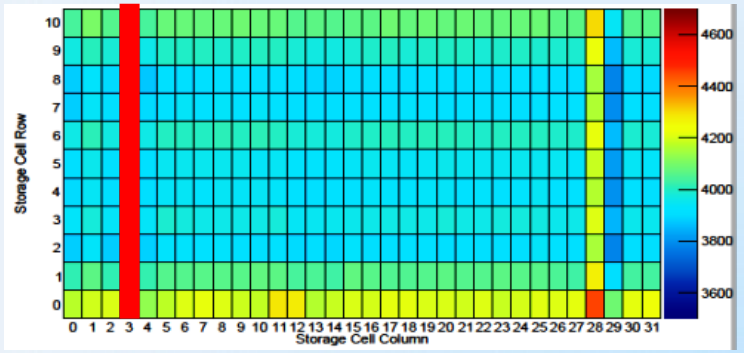
AGIPD1.0: ‘Pixel maps: Baseline’



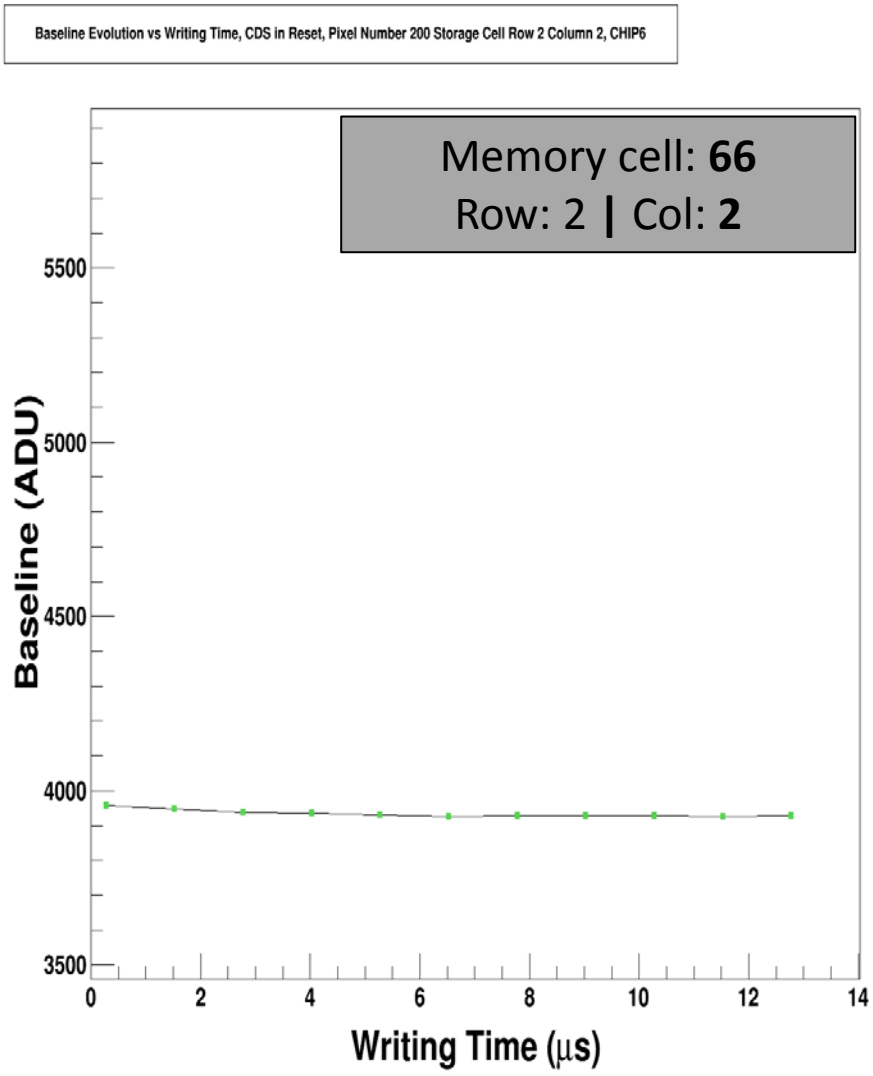


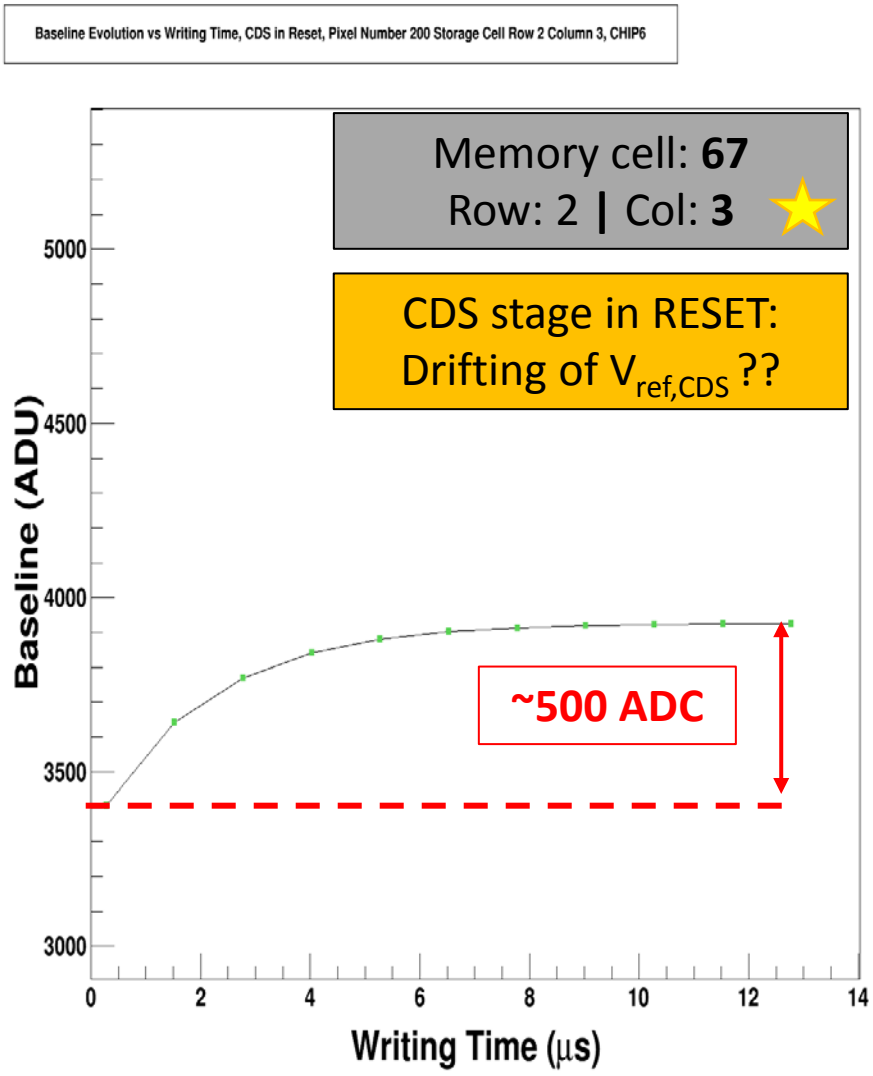
Readout at **5 MHz**
Integration time: **2.3 µs**

Memory cell: **67**
Row: 2 | Col: **3**

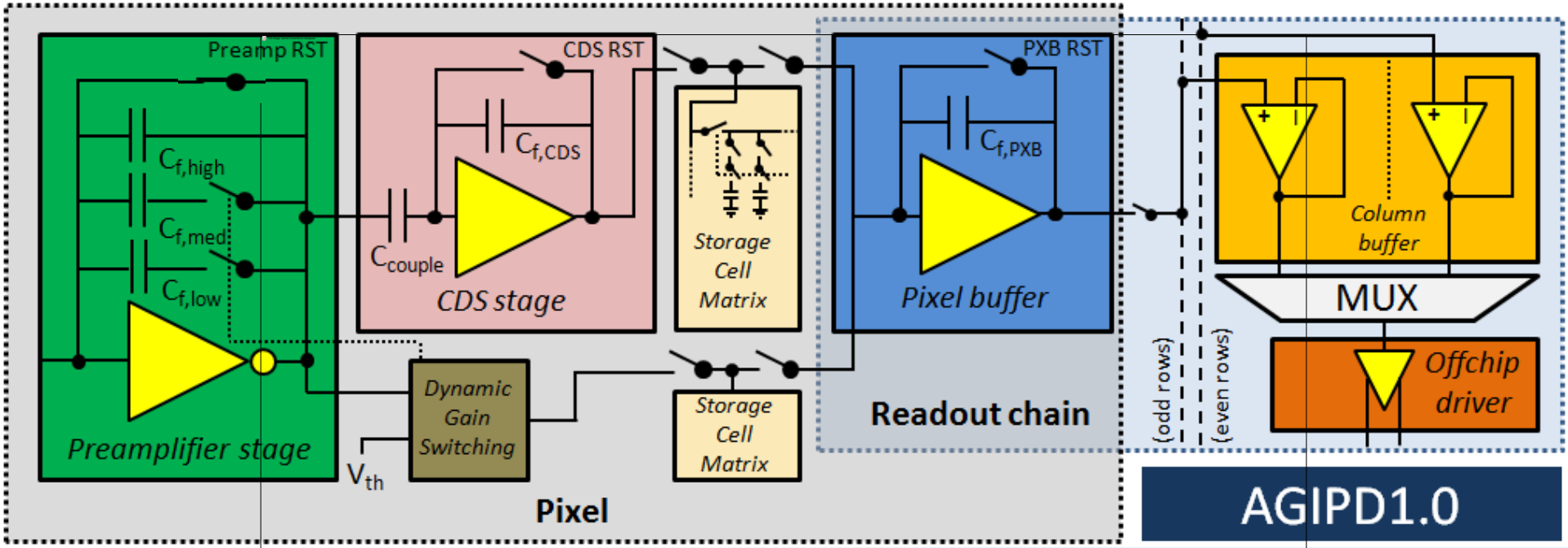


AGIPD1.0: ‘Pixel maps: Baseline’





AGIPD1.0: 'Pixel maps: Baseline'



- Identify the origin of this change of baseline
- **CDS buffer ACTIVE, PREAMP in RESET**
- **Acquire baseline** for **$V_{ref,CDS}$= 700 mV**
- Use **different writing times**

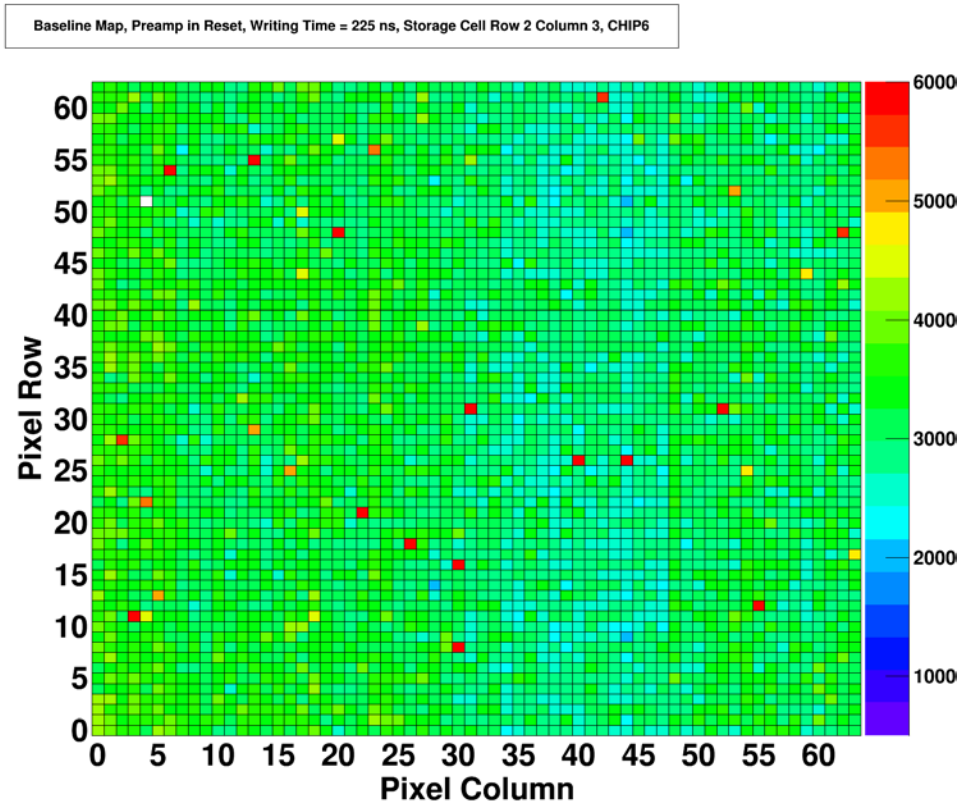
If the PREAMP is in RESET: $\Delta V_{in} = 0$

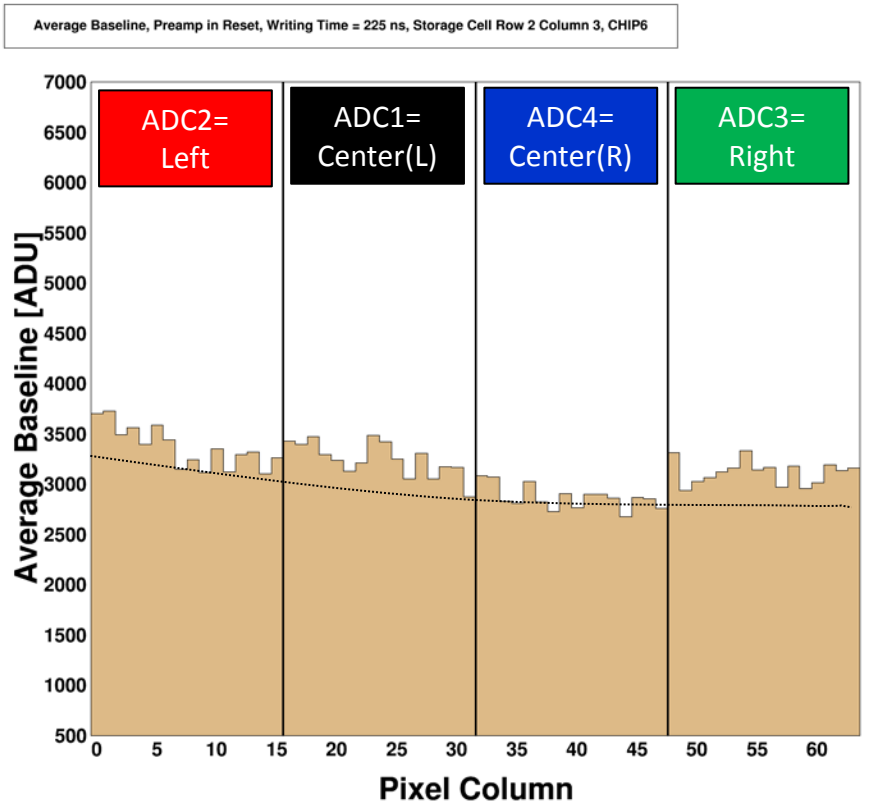
→ Drifting of $V_{ref,CDS}$ would result in:

$$\Delta V_{out} = (1 + \frac{C_c}{C_f}) \cdot \Delta V_{ref,CDS}$$

→ C_c/C_f=2.5: ΔV_{out}= 3.5 x 500 ADU = 1750 ADU

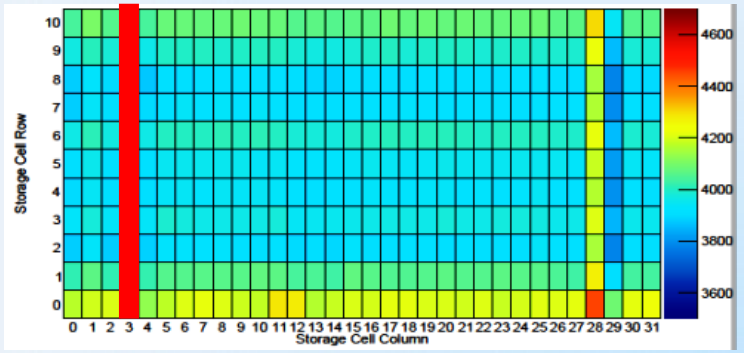
AGIPD1.0: ‘Pixel maps: Baseline’



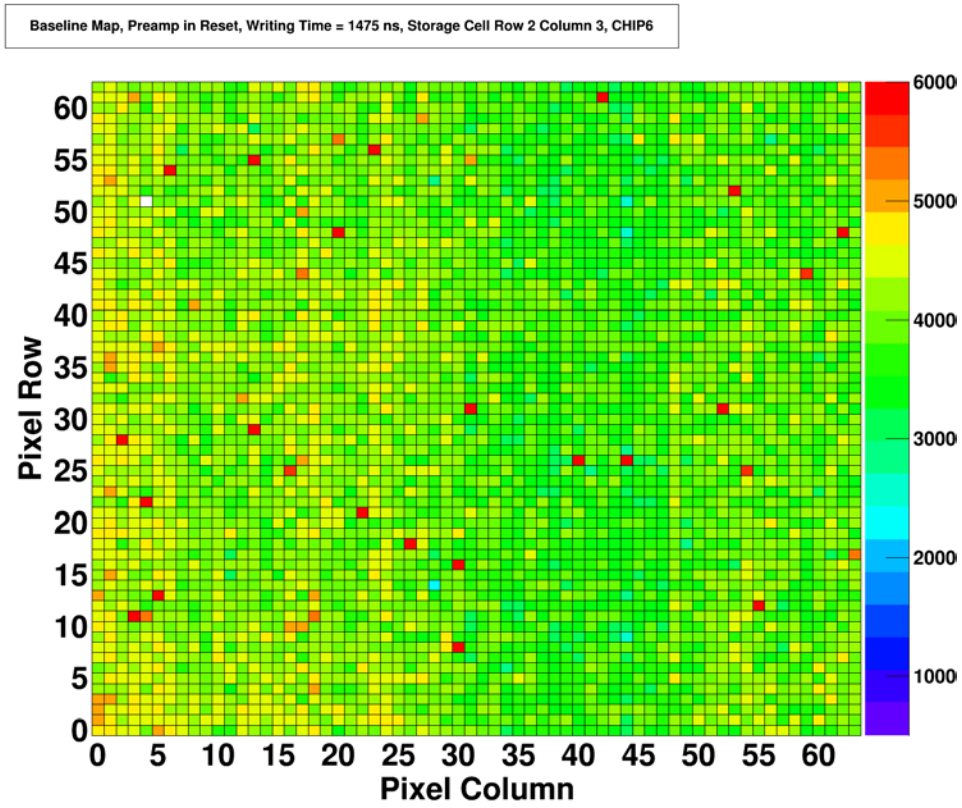


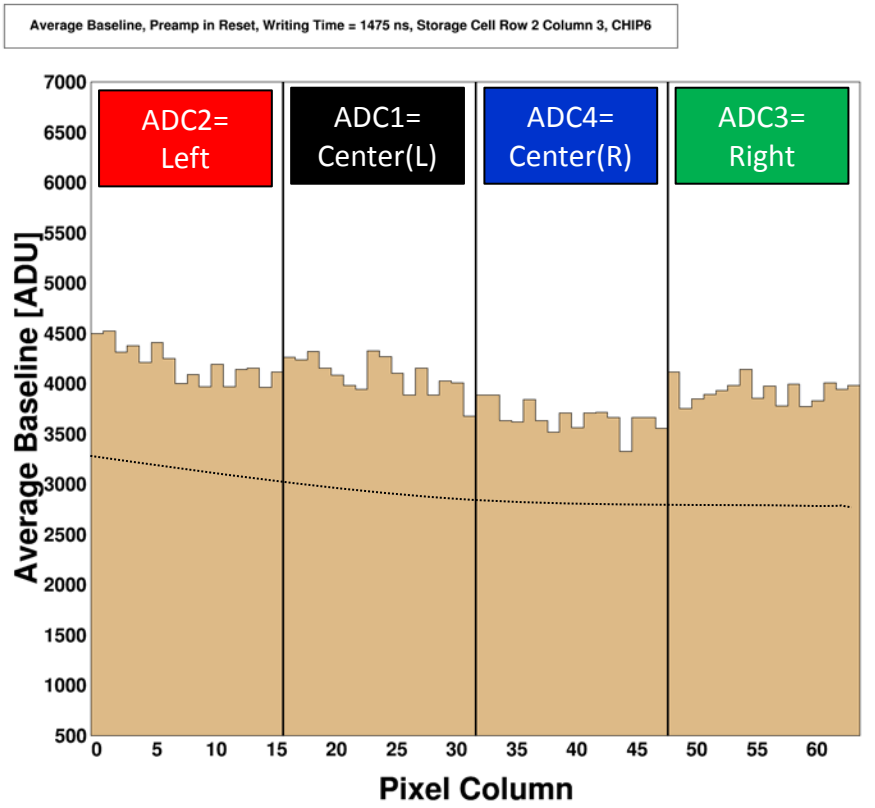
Readout at **5 MHz**
Integration time: **225 ns**

Memory cell: **67**
Row: 2 | Col: **3**



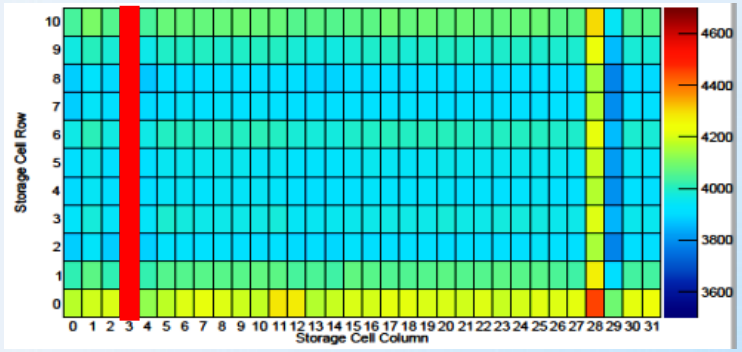
AGIPD1.0: ‘Pixel maps: Baseline’



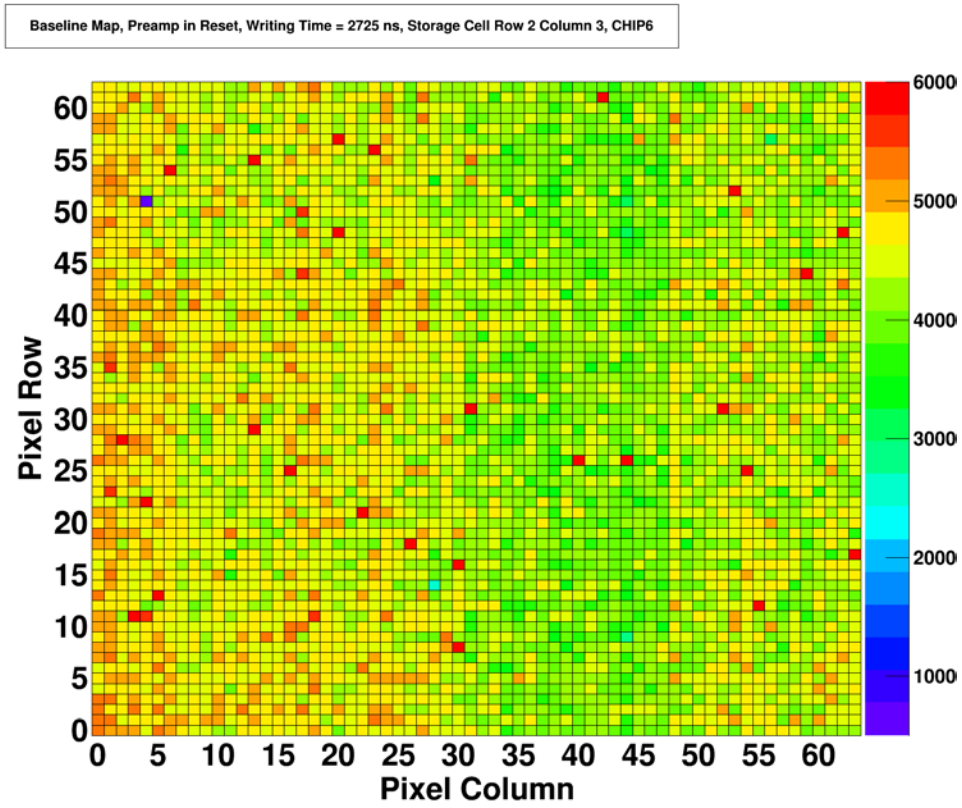


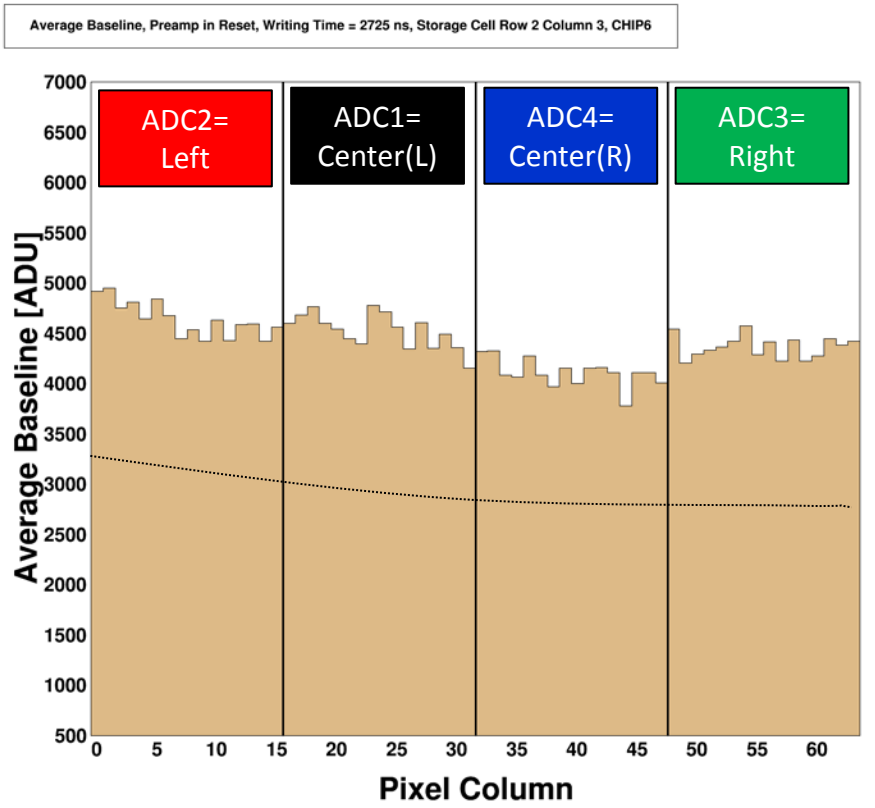
Readout at **5 MHz**
Integration time: **1.5 µs**

Memory cell: **67**
Row: 2 | Col: **3** ★



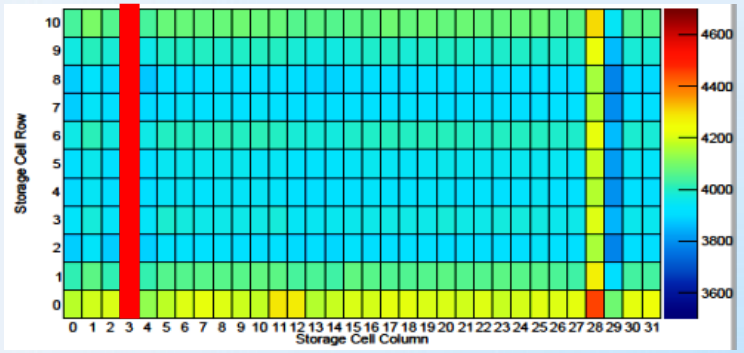
AGIPD1.0: ‘Pixel maps: Baseline’



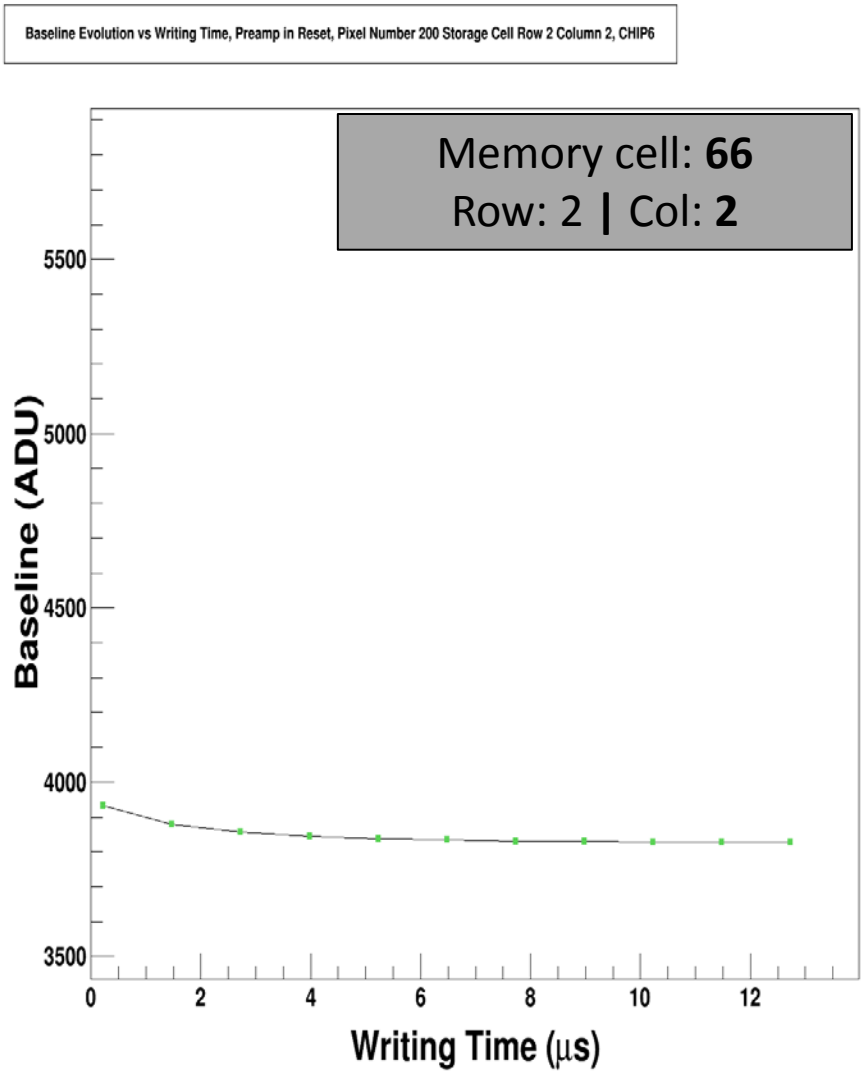


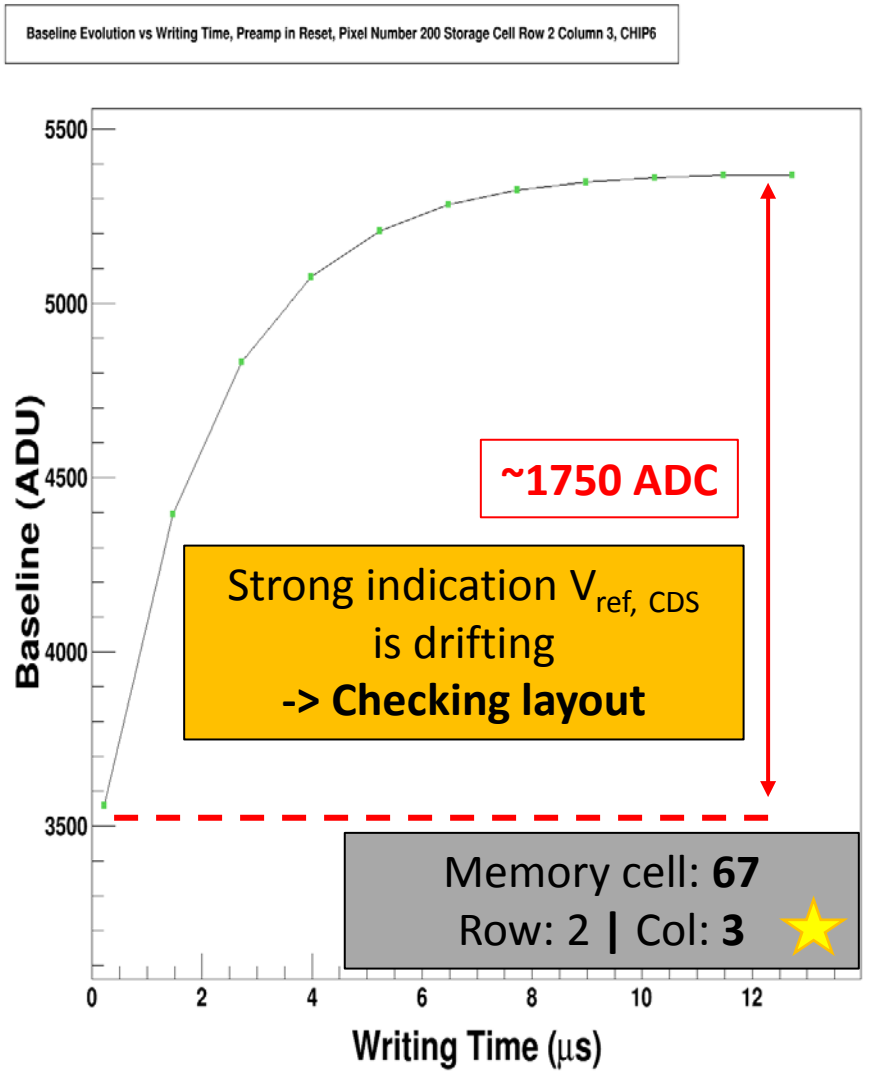
Readout at **5 MHz**
Integration time: **2.7 µs**

Memory cell: **67**
Row: 2 | Col: **3** ★

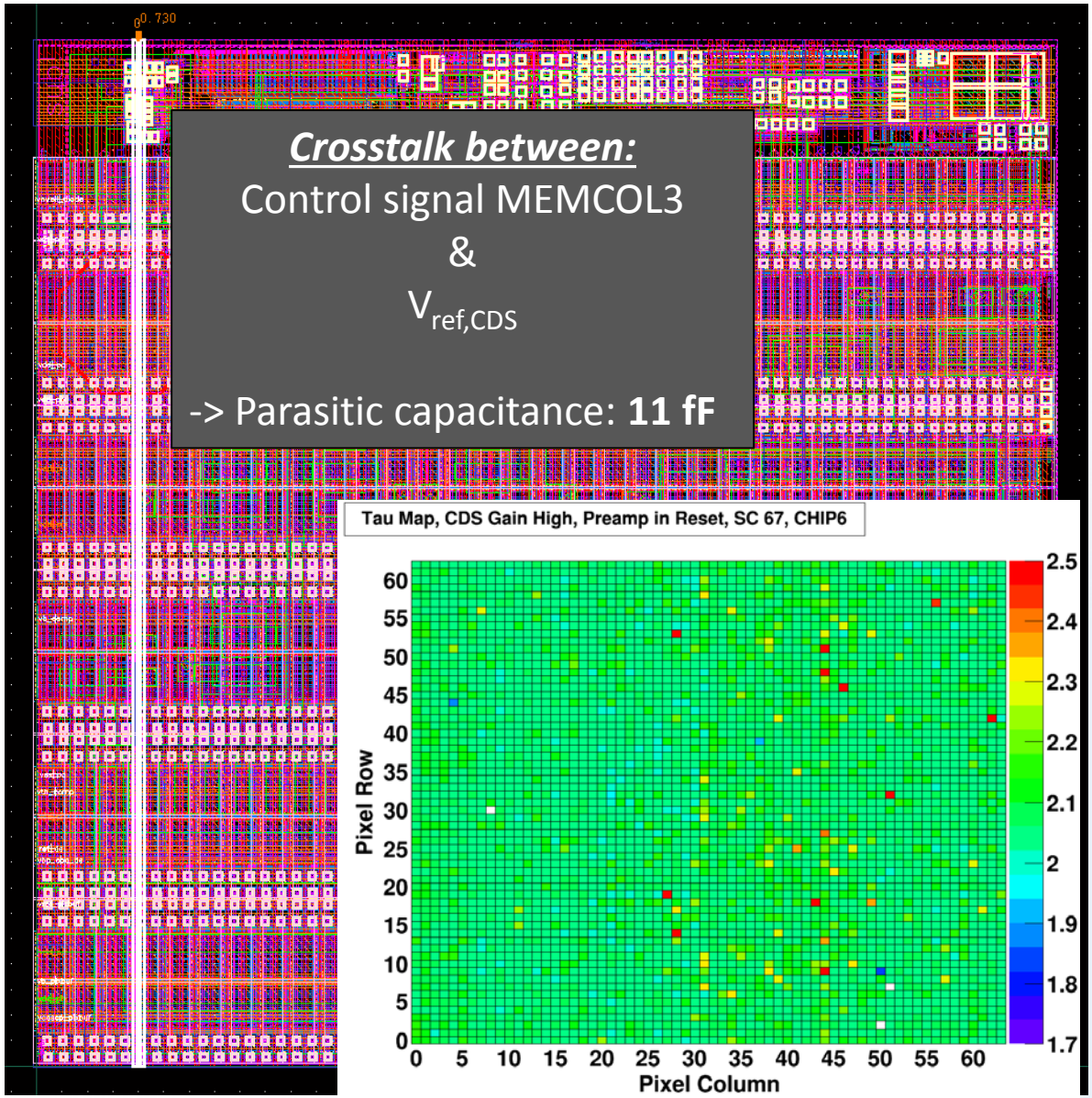


AGIPD1.0: ‘Pixel maps: Baseline’



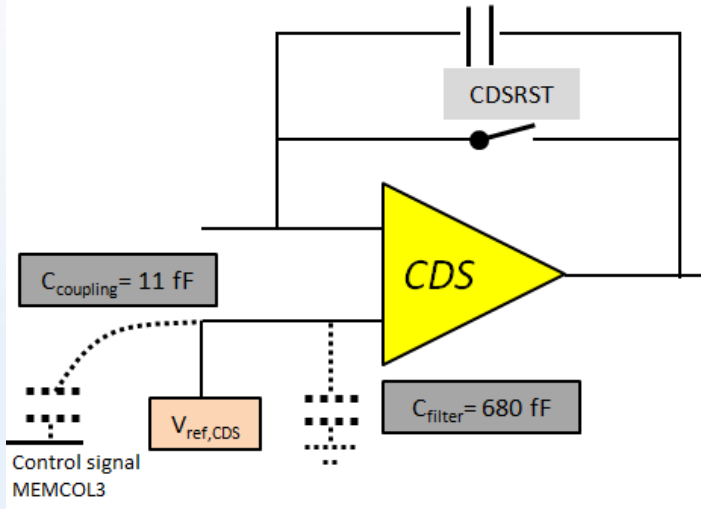


AGIPD1.0: ‘Pixel maps: Baseline’



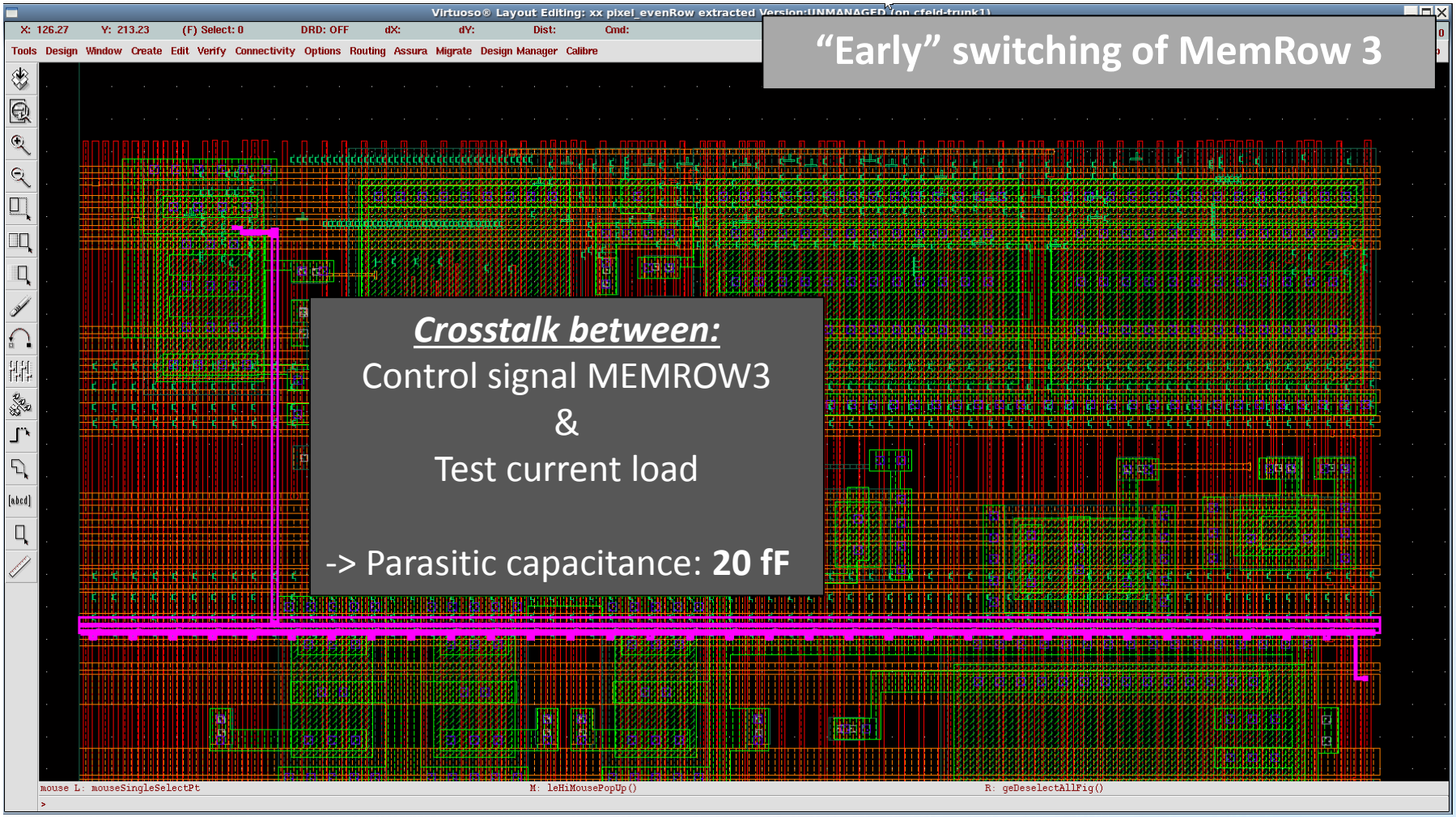
$C_{coupling}$ = 11 fF (MEMCOL 3/$V_{ref, CDS}$)
C_{filter} = 680 fF

-> Control signal at 1.5 V, if selected
-> **Increase of $V_{ref,CDS}$ of 23.8 mV or 585 ADU**



⑤ Pixel/Memory cell maps: Baseline drift ✓

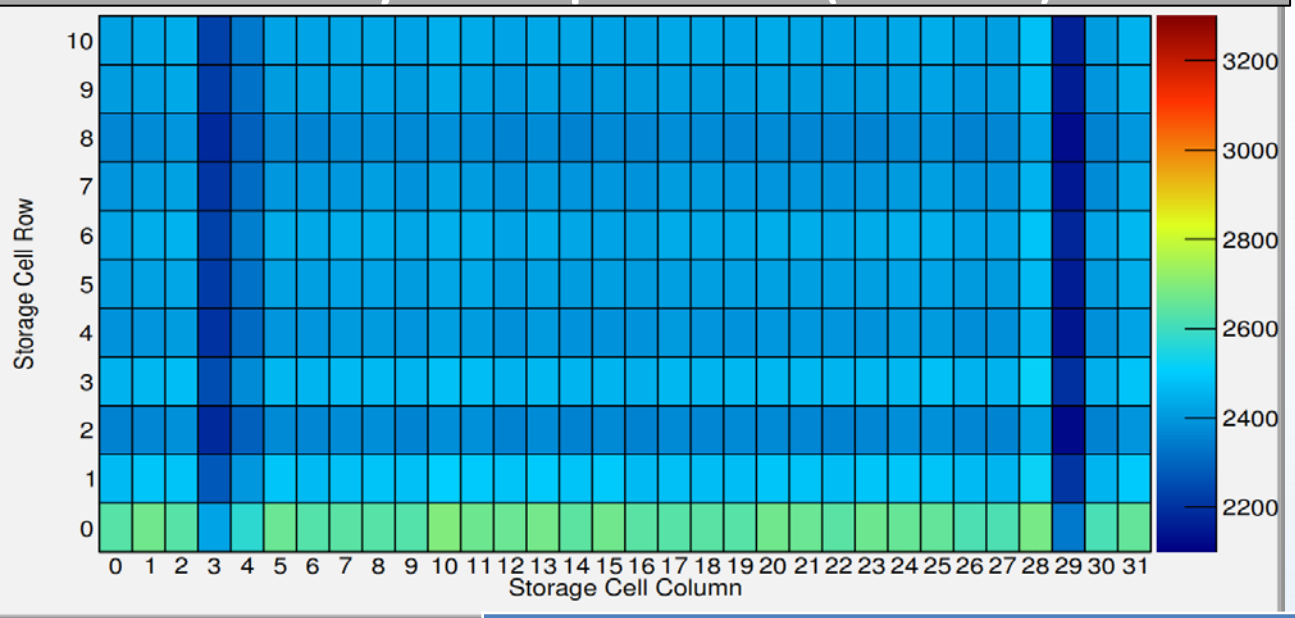
AGIPD1.0: ‘Memory Cell Maps’



Crosstalk **increases injected current**

AGIPD1.0: ‘Memory Cell Maps’

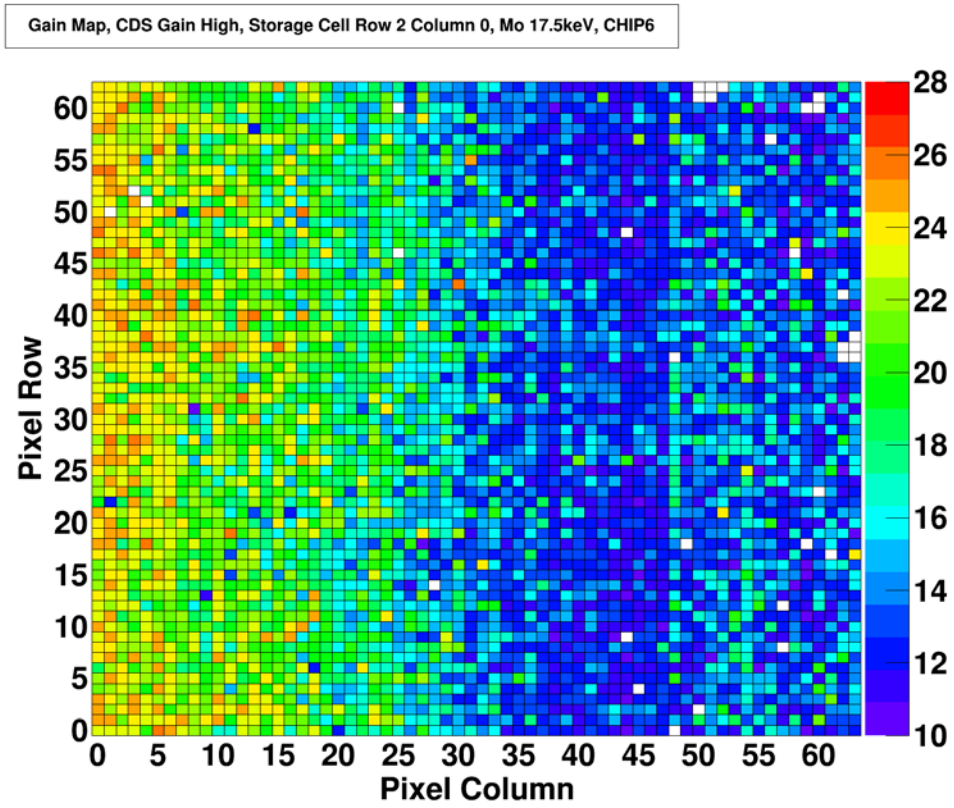
Memory cell map: Baseline (TestI OFF)

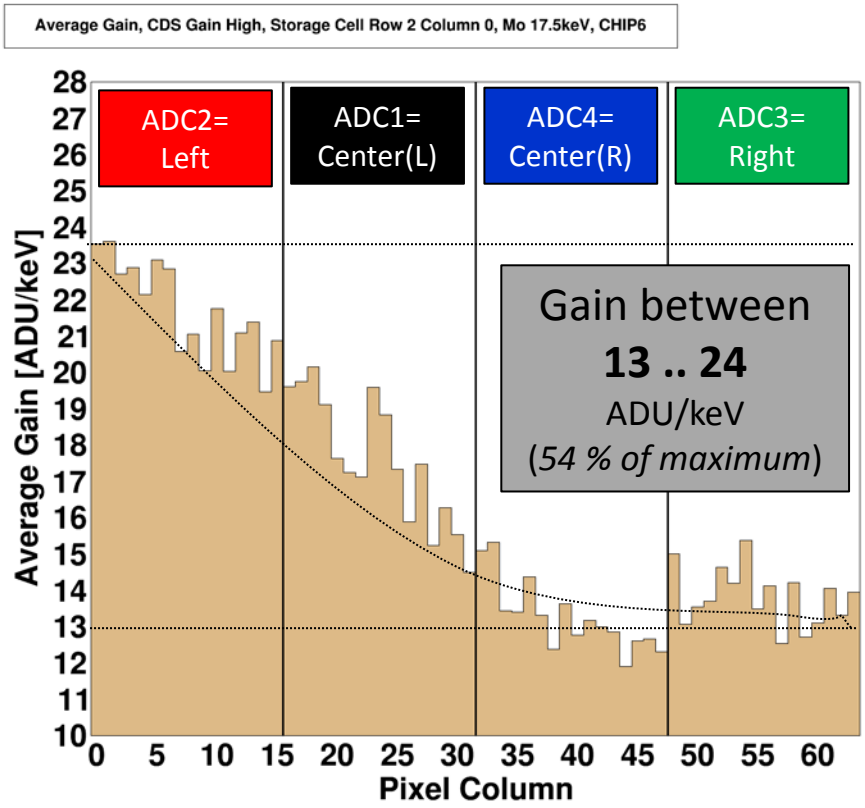


Several sources of crosstalk could be extracted and verified by simulations

Crosstalk between …		Parasitic capacitance
MEMCOL3	$V_{ref,CDS}$	11.1 fF
MEMROW3	Test current load	20.0 fF
MEMROW0	Pixel input	5.35 fF
MEMCOL29	Vref,PXB	12.5 fF
MEMCOL29	Pix Out	18.3 fF
…	…	…

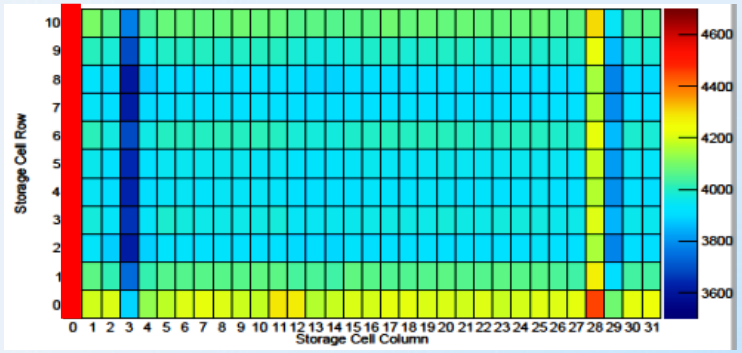
AGIPD1.0: ‘Pixel maps: Gain’



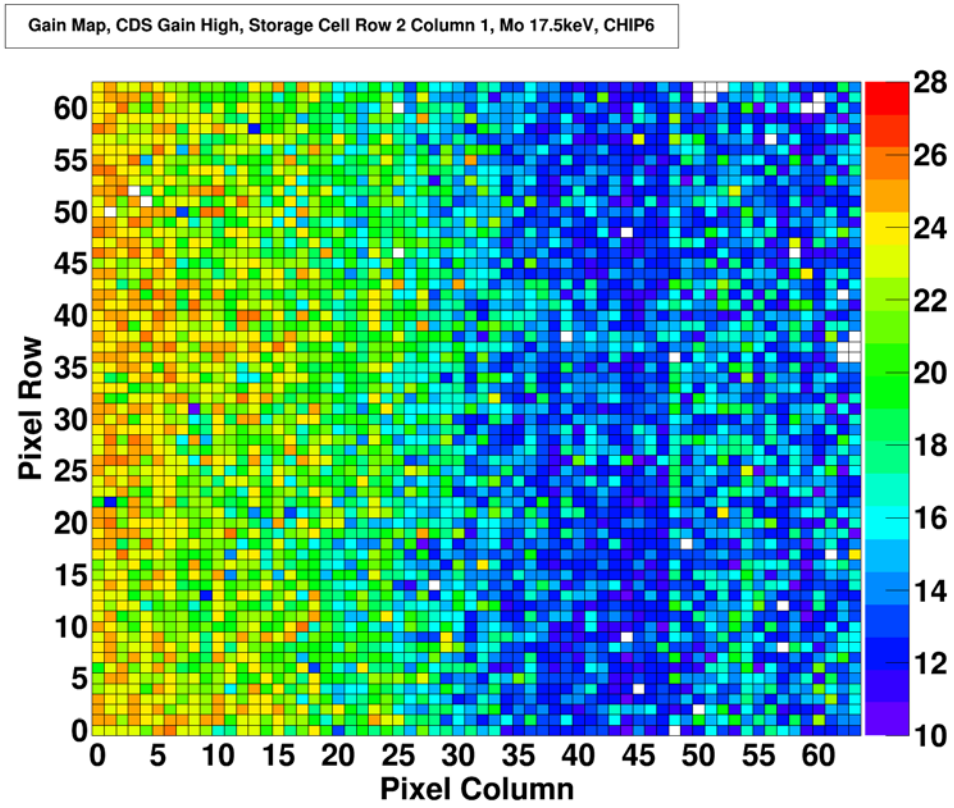


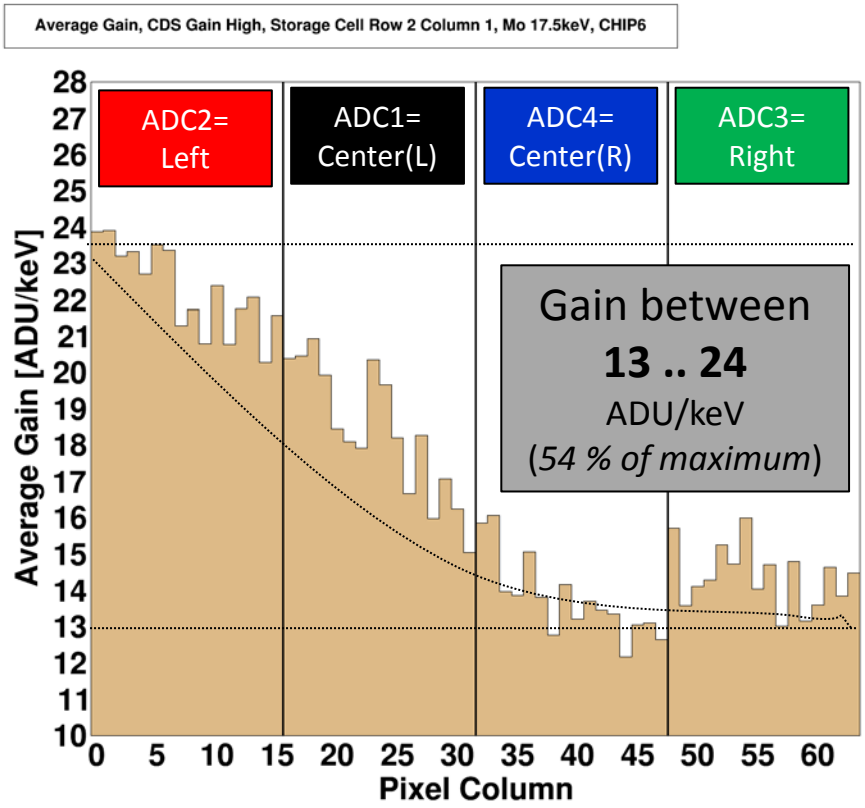
Readout at **5 MHz**
Integration time: **10 µs**

Memory cell: **64**
Row: 2 | Col: **0**



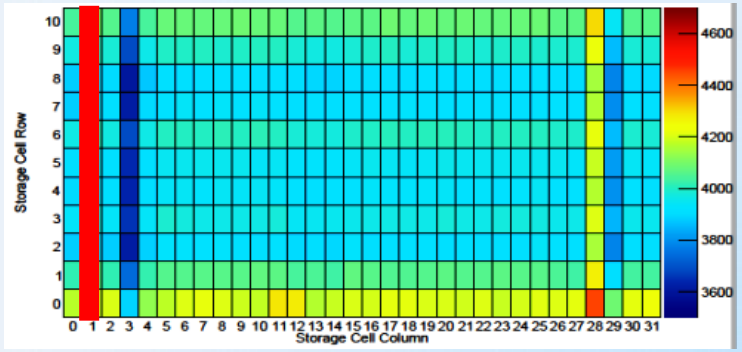
AGIPD1.0: ‘Pixel maps: Gain’



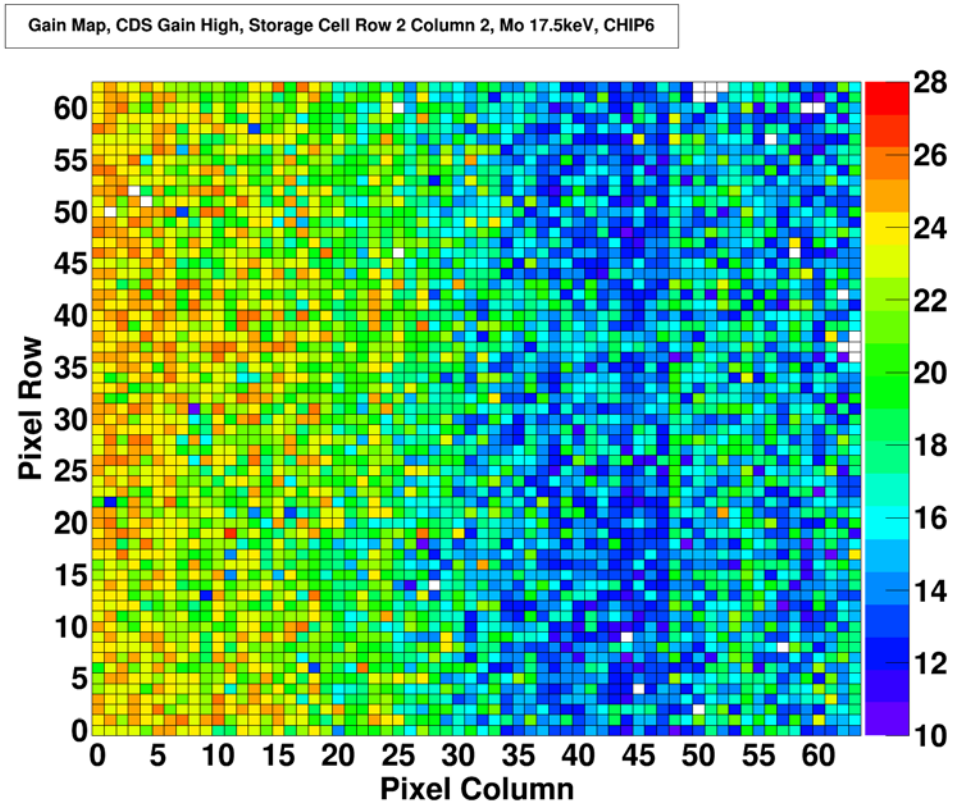


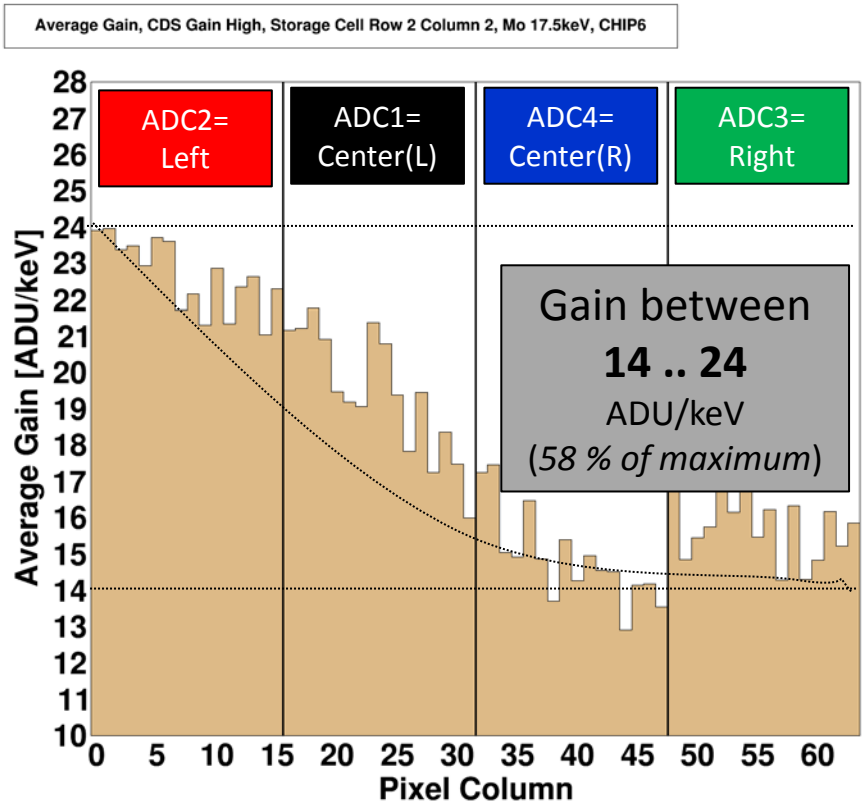
Readout at **5 MHz**
Integration time: **10 µs**

Memory cell: **65**
Row: 2 | Col: **1**



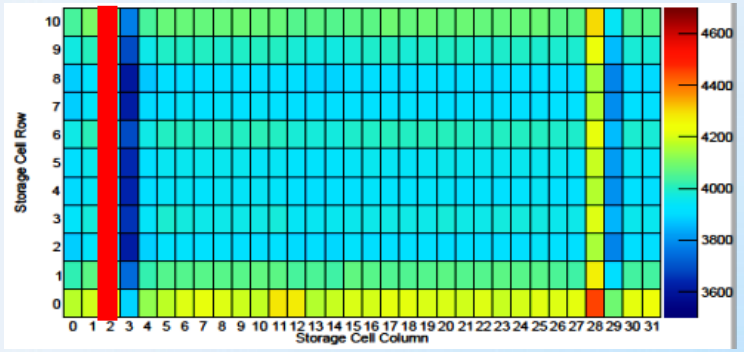
AGIPD1.0: ‘Pixel maps: Gain’



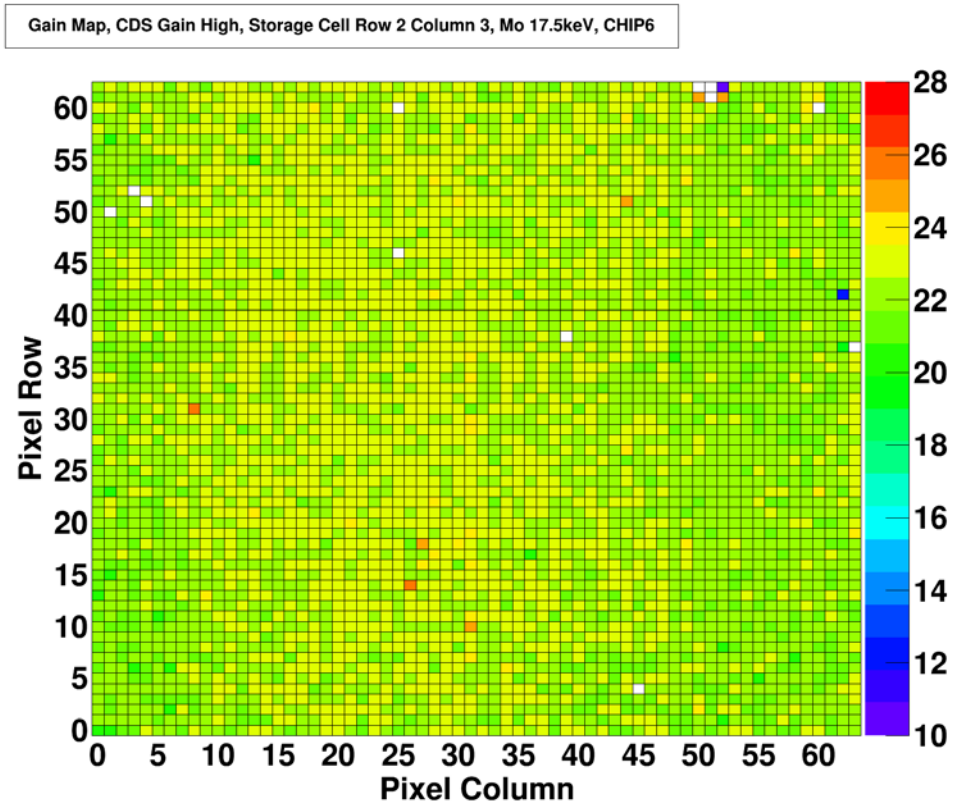


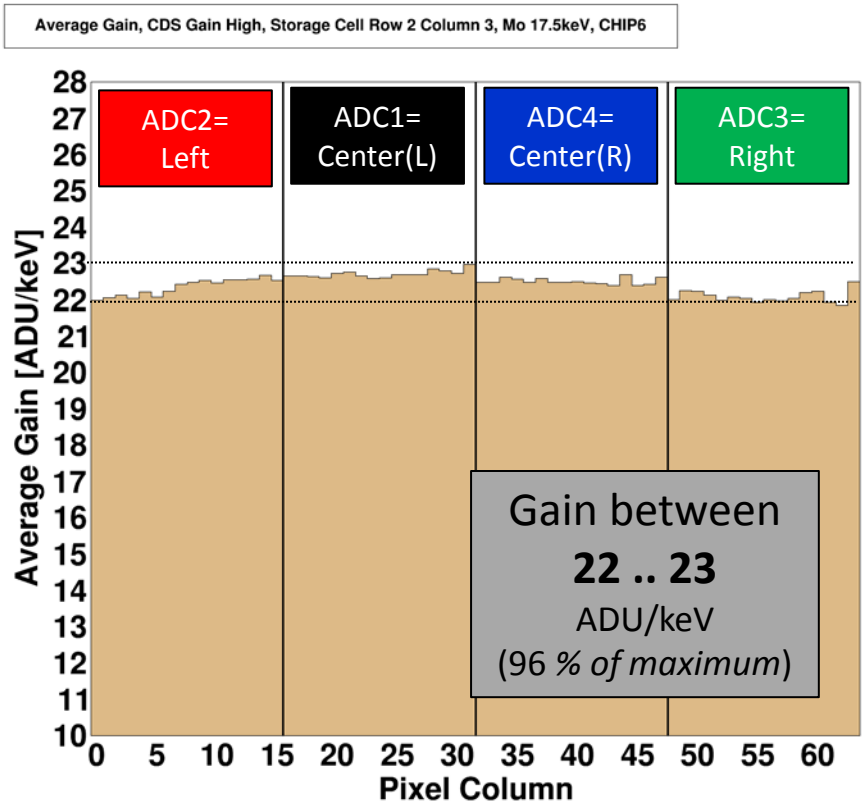
Readout at **5 MHz**
Integration time: **10 µs**

Memory cell: **66**
Row: 2 | Col: **2**



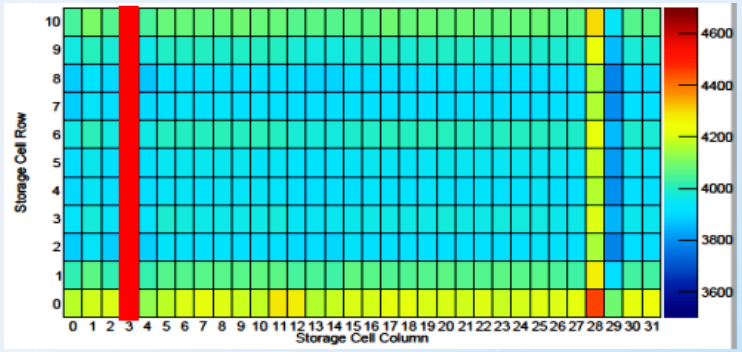
AGIPD1.0: ‘Pixel maps: Gain’



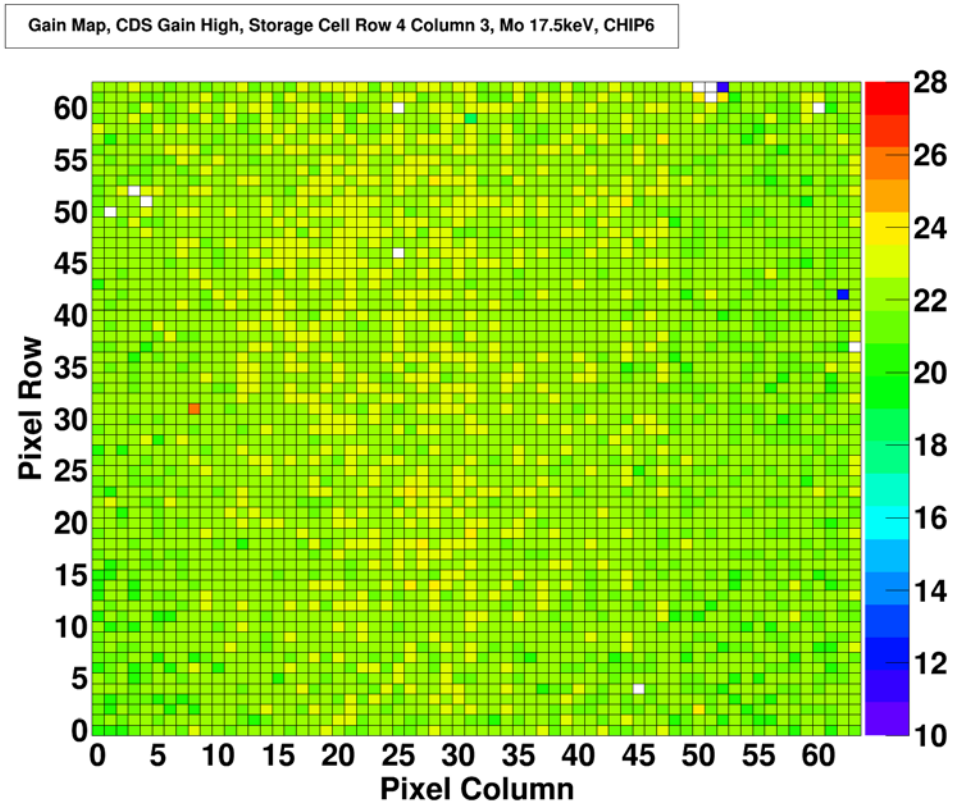


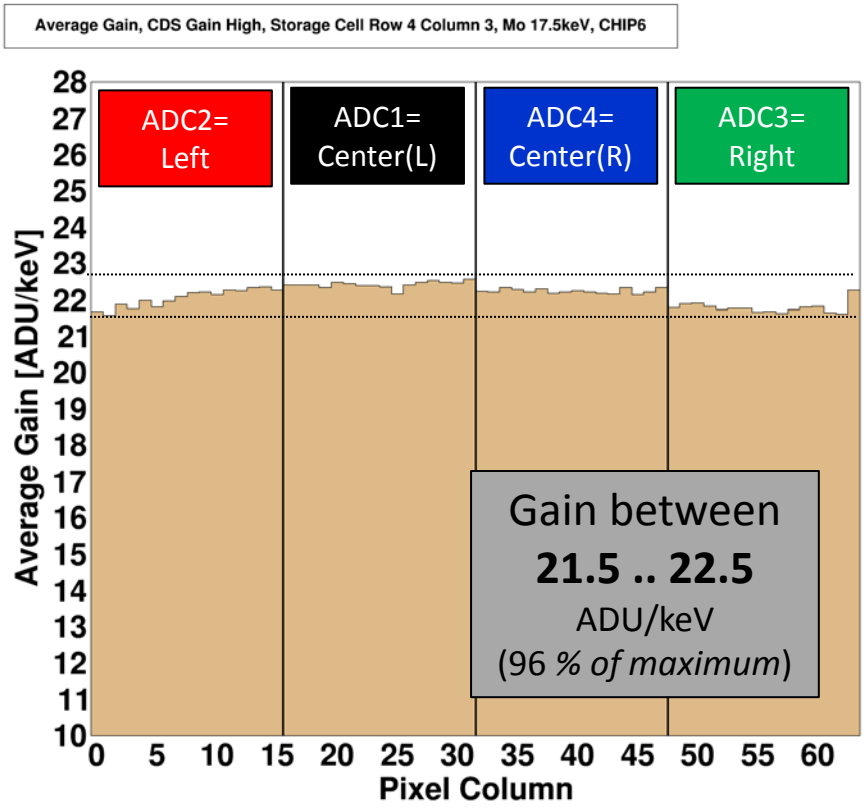
Readout at **5 MHz**
Integration time: **10 µs**

Memory cell: **67**
Row: 2 | Col: **3**



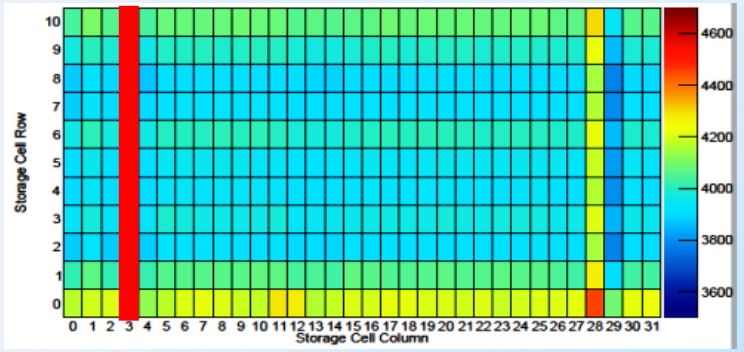
AGIPD1.0: ‘Pixel maps: Gain’



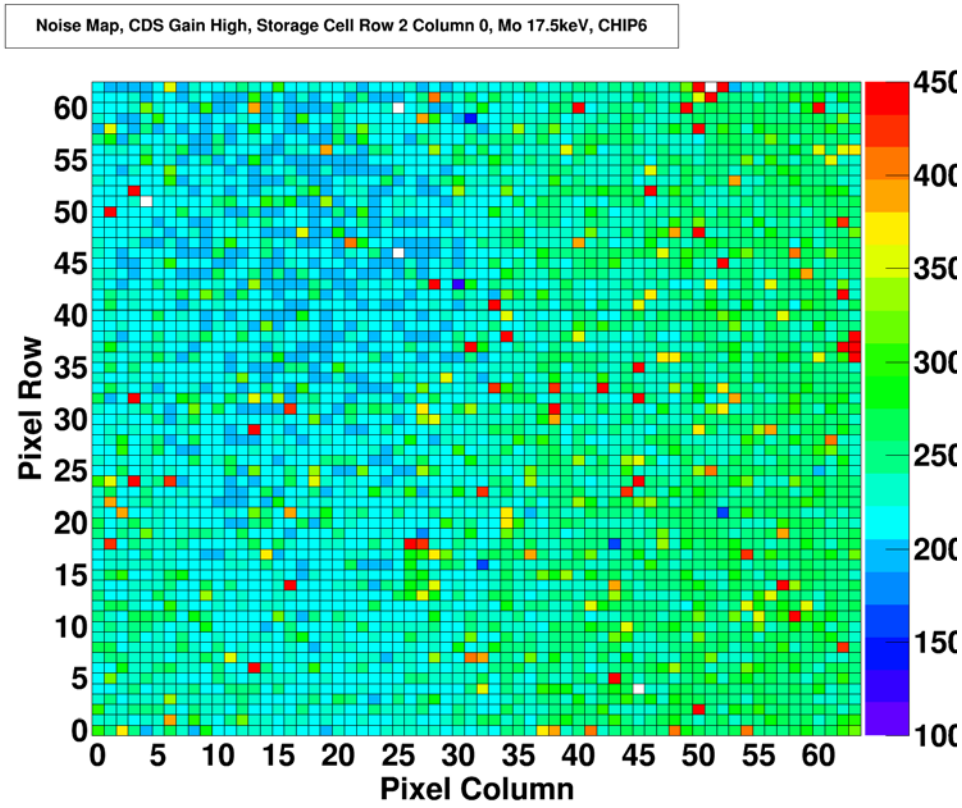


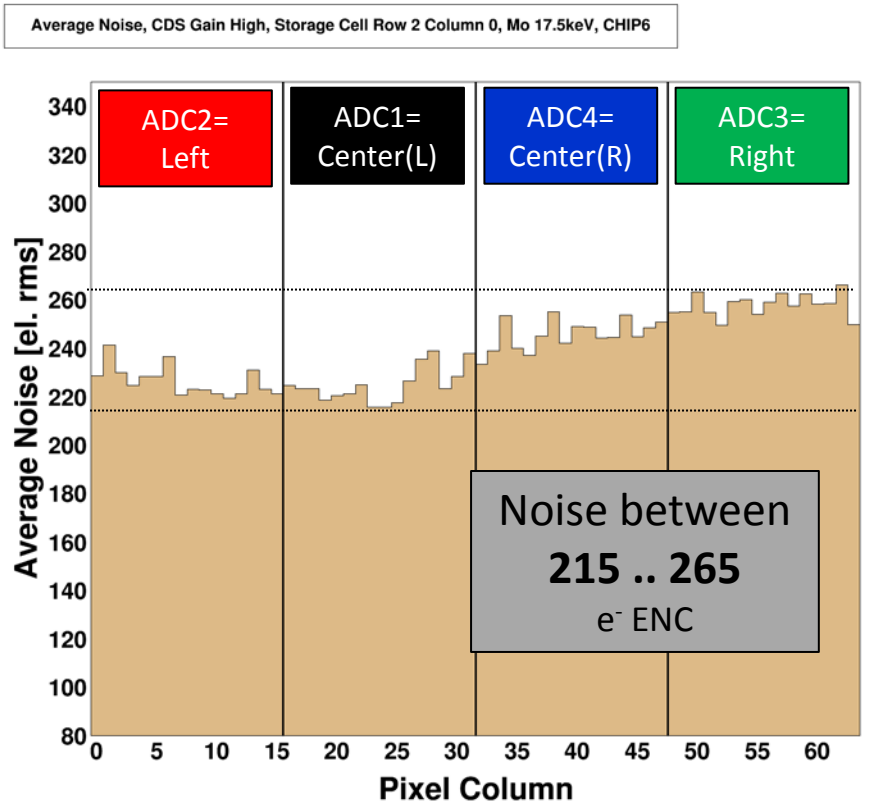
Readout at **5 MHz**
Integration time: **10 µs**

Memory cell: **131**
Row: 4 | Col: **3**



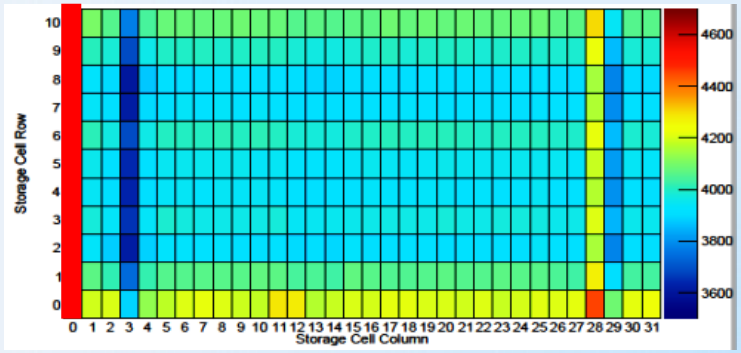
AGIPD1.0: ‘Pixel maps: Noise’



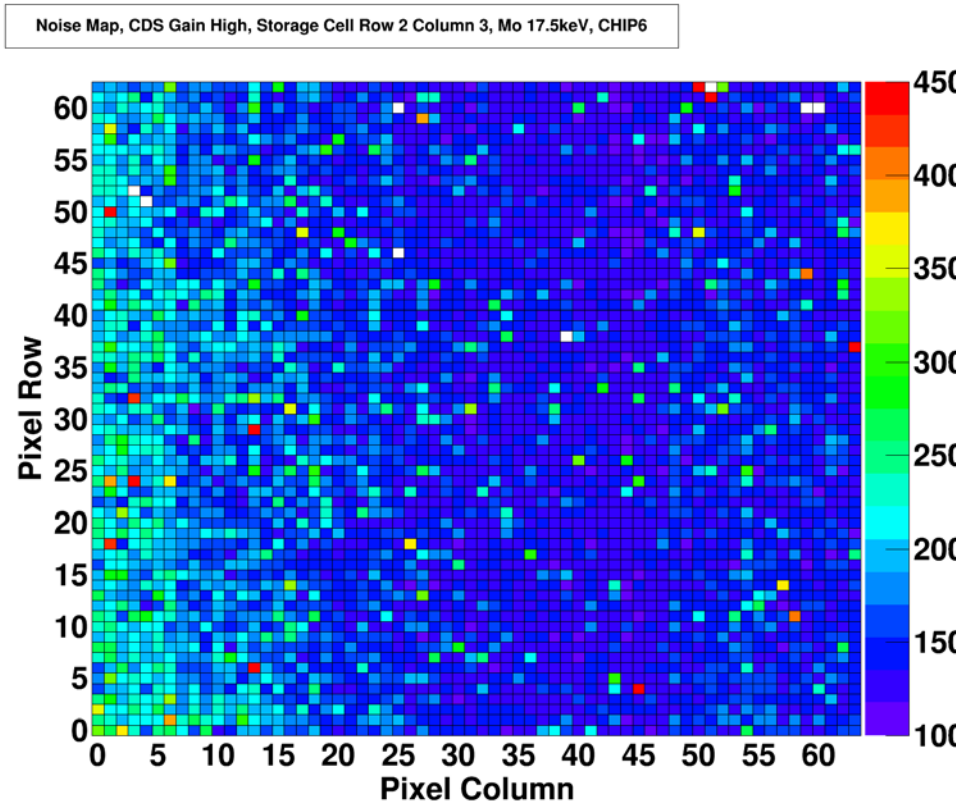


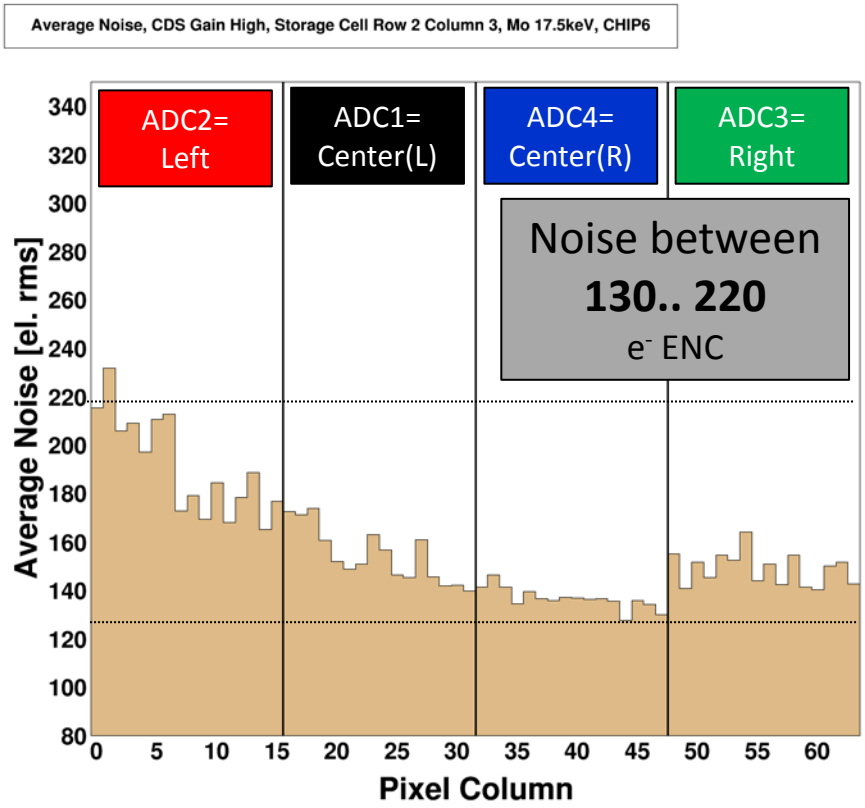
Readout at **5 MHz**
Integration time: **10 µs**

Memory cell: **64**
Row: 2 | Col: **0**



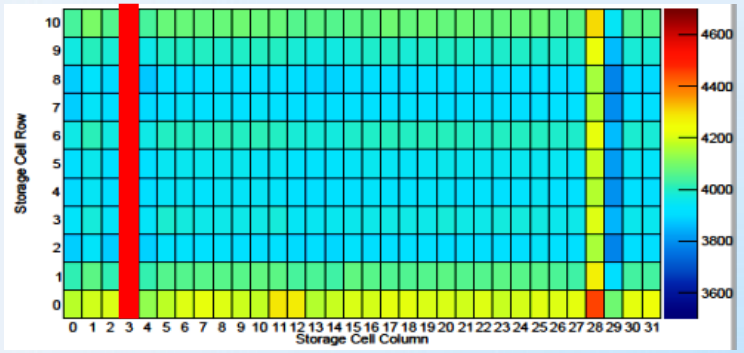
AGIPD1.0: ‘Pixel maps: Noise’



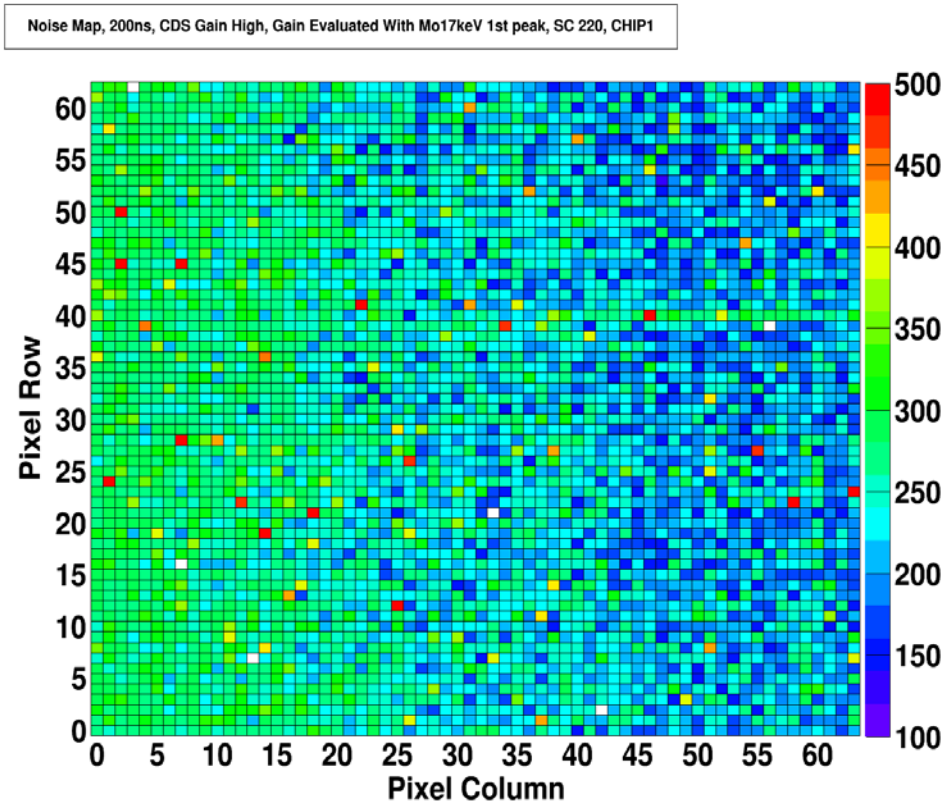


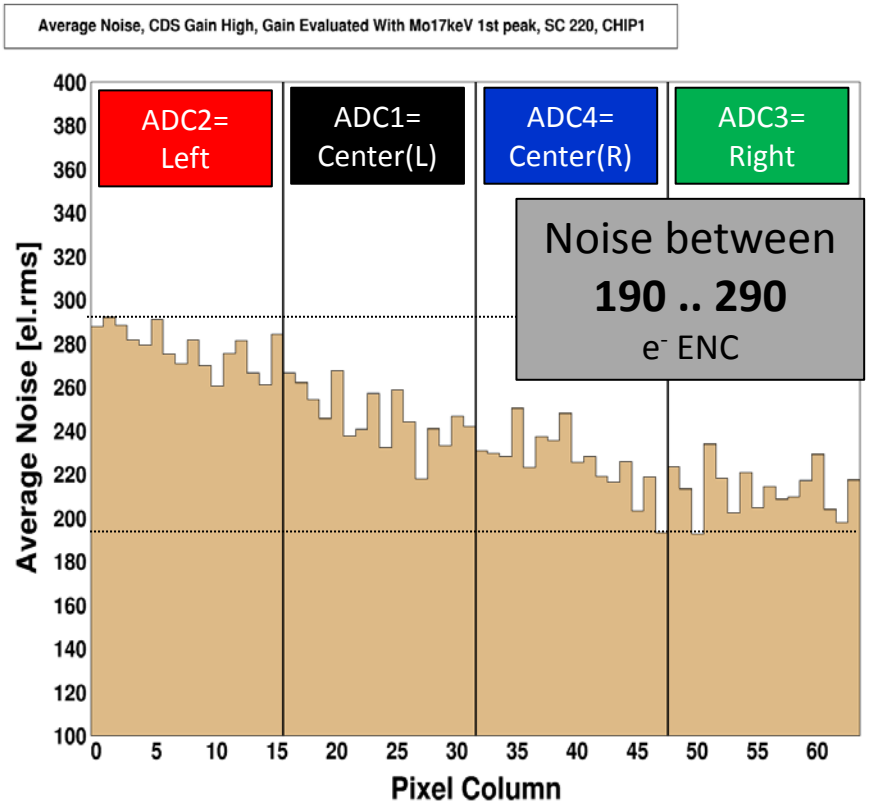
Readout at **5 MHz**
Integration time: **10 µs**

Memory cell: **67**
Row: 2 | Col: **3**



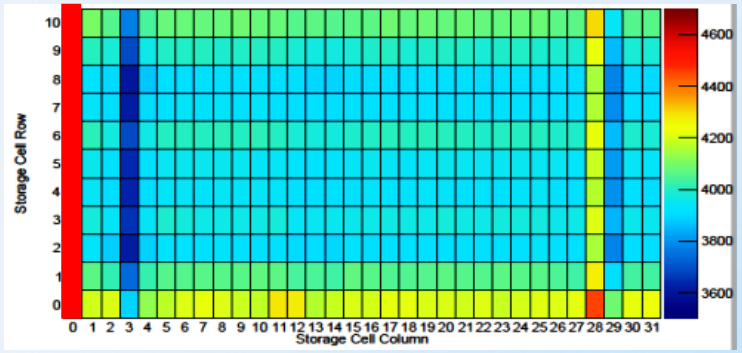
AGIPD1.0: ‘Pixel maps: Noise’





Readout at **5 MHz**
Integration time: **10 µs**

Memory cell: **220**
Row: 6 | Col: **28**
(Reference storage cell for initial noise measurement)



AGIPD1.0: Characterization status (May 2015)

	Issue	Solution(s)	Criticality	End Date
1	**Readout speed:** Variation between offchip routes	Routing change to equalize the different RCs	Very high	Done
2	**Readout speed:** Overall slow speed of analogue outputs	Improve power supply impedance (Offchip driver)	Very high	August
3	**"Ghosting"**: Crosstalk between outputs	Additional buffer to decouple reference voltage	High	June
4	**Digital Bit:** "High gain" level (matching to analog baseline)	Writing High Gain Bit with source follower from $V_{ref,CDS}$	Low	June
5	**Digital Bit:** "Low gain" voltage connected to vnwell_pix	Reconnect the "low gain" voltage to the vdd_pix	Low	June
6	**Digital Bit:** Optimizing gain bit separation	Different gain for analogue and gain readout (PXB)	Medium	June
7	**Digital Bit:** No gain encoding in fixed gain mode	Logic change to enable gain bit signals in fixed gain mode	High	June
8	**Pixel/Memcell maps:** Premature switching of mem row 3 (testI)	Crosstalk: Control Line/TestI increases injected current	High	July
9	**Pixel/Memcell maps:** "Stripe patterns" in memory map	Crosstalk / Routing change	High	July
10	**Pixel/Memcell maps:** Variation of baseline over chip	Crosstalk of control signal with $V_{ref,CDS}$	Very high	July
11	**Pixel/Memcell maps:** Variation of gain over chip	(Possibly) crosstalk in layout / Final reason not identified	Very high	Unknown
12	**General optimization:** Power-on reset stability	Modify RC circuit	Medium	July
13	**General optimization:** Small overlap of CLK and token in MUX	Improve MUX_CLK driver	Low	August
14	**General optimization:** Additional capacitance of TSV pads		Very low	
15	**Calibration:** Redesign test current source	Optimization of current mirror / enable switches	Very high	July
16	**Submission:** Periphery test structure		High	October
17	**Submission:** Additional layouts	(AGIPD 0.6, other?)	Low	October

Status

: Understood / Redesign needed

: Understood / Realization to be discussed

: Under investigation / Idea of reason

: Under investigation/ Reason unclear

Submission of AGIPD1.1: Fall 2015

① Calibration circuits √

② 'Ghosting' √

③ Digital bits √

④ Readout speed √

⑤ Pixel/Memory cell maps (√)