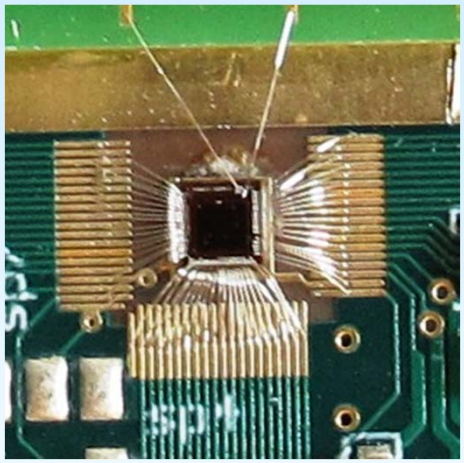
AGIPD - Prototypes

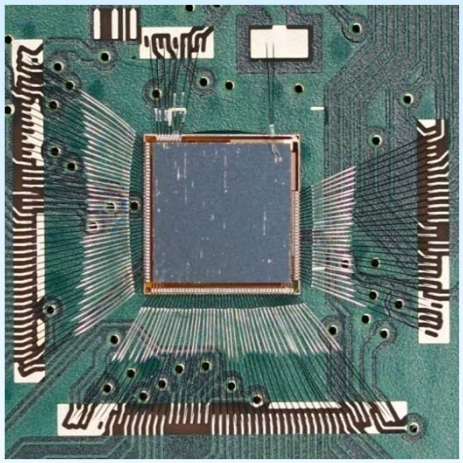
AGIPD 0.1



- No pixels yet
- 3 readout blocks consisting of:

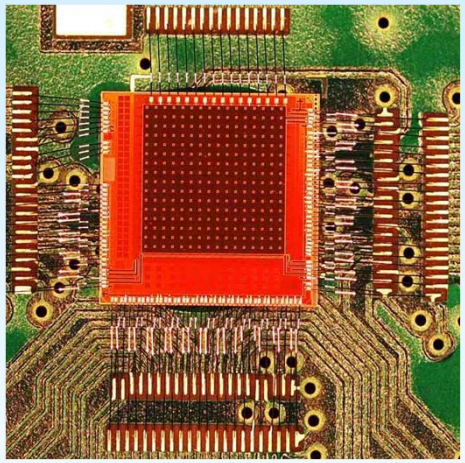
→ Readout chain (Preamp + CDS stage)
→3 different kinds of leakage current compensation

AGIPD 0.2



- 16 x 16 pixels
- 100 storage cells
- No leakage current compensation
- Different combinations of preamps and storage cell architechures

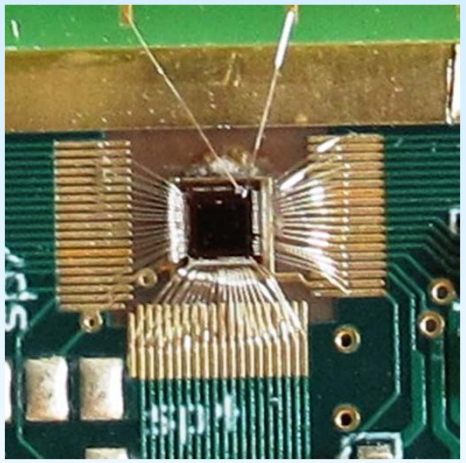
AGIPD 0.3



- 16 x 16 pixels
- 200 storage cells
- Radiation hard storage cell design
- High speed serial control logic

AGIPD - Characterization

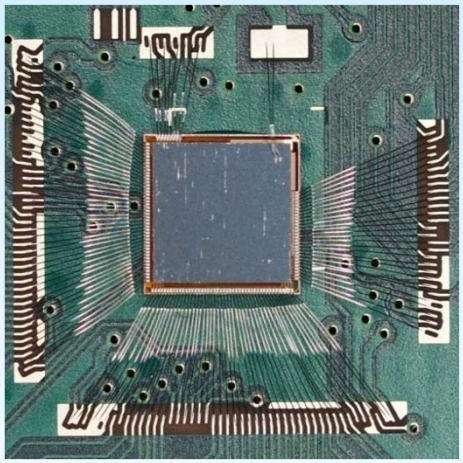
AGIPD 0.1



- Linearity of the gain
- Stress-test of the input gate at the preamp
- Temporal behavior of the preamp and CDS stage

Already Shown!

AGIPD 0.2

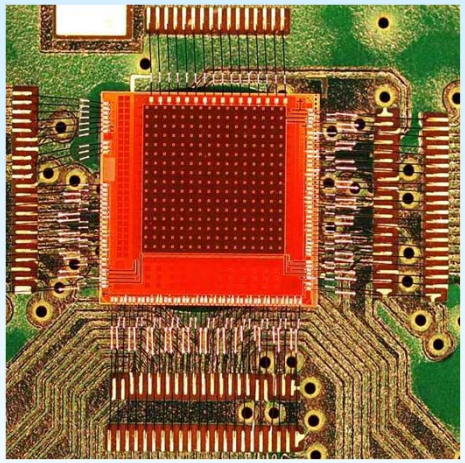


- Charge sharing & Crosstalk
- Storage cell variations
- Pixel-to-pixel variations

Okay!

- Gain vs. number of storage cells

AGIPD 0.3

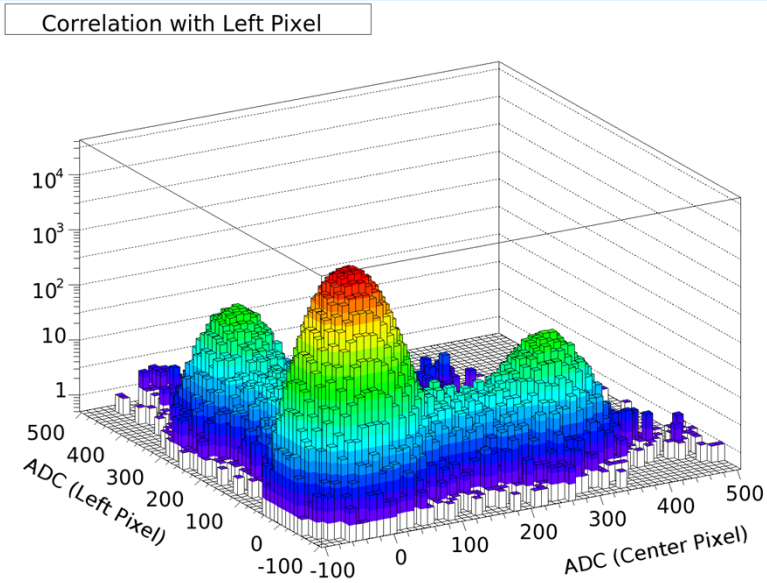


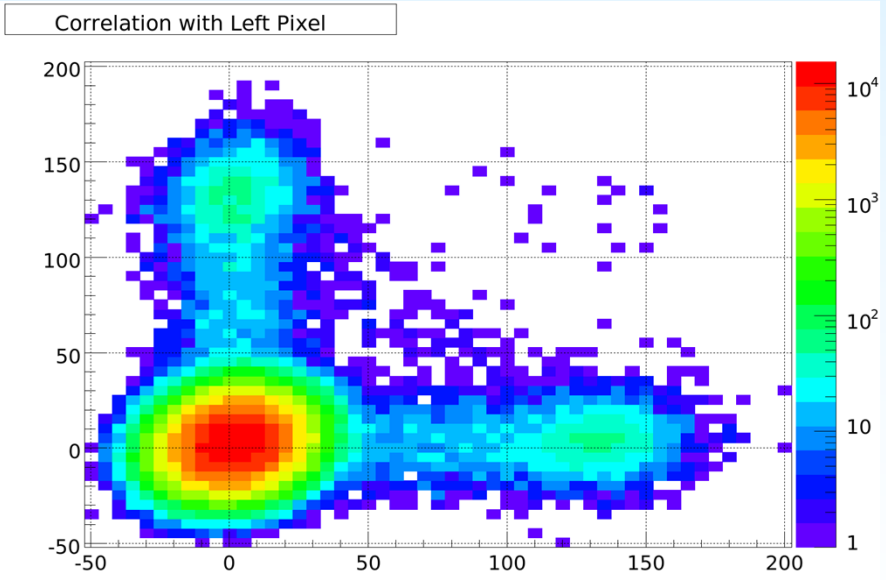
- Radiation hardness of storage cells
- Test of the high speed serial control logic

Ongoing

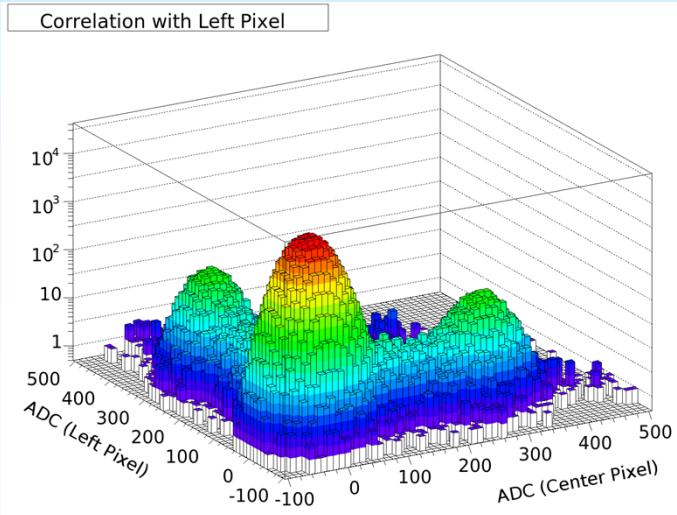
AGIPD02 - Charge Sharing

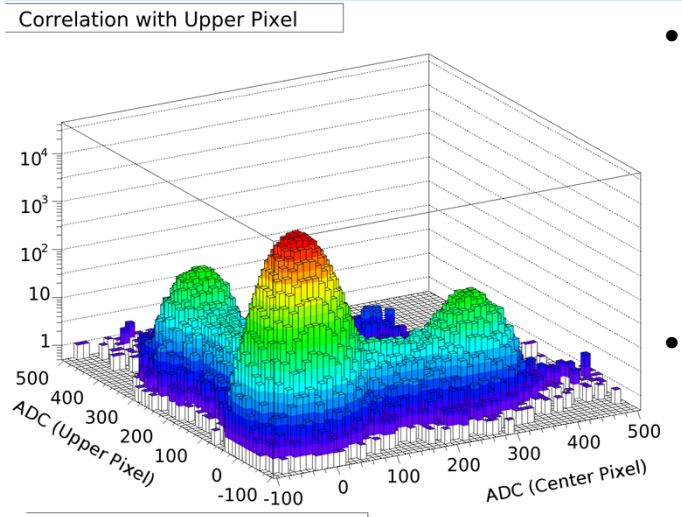
- X-ray fluorescence from Ge (10 keV) & Mo (17.5 keV) on pixel matrix
- Integration time: 1 μs
- Sensor voltage: 120 V
- 2d plot: Pulseheight in center pixel vs. Pulseheight in direct neighbor pixels



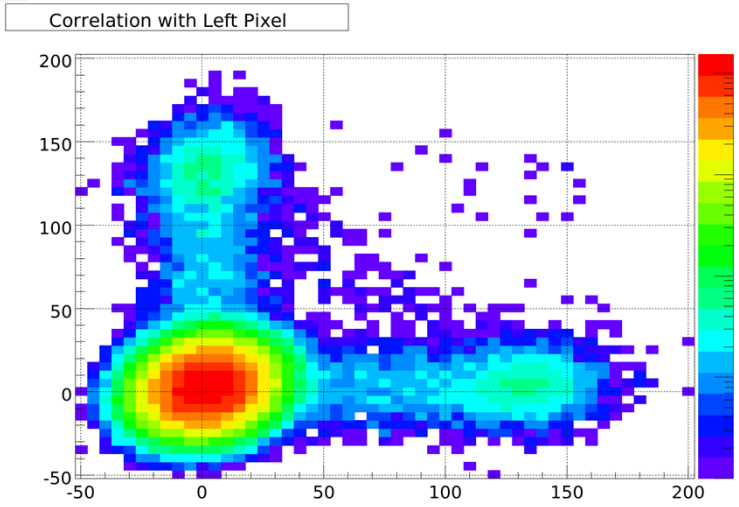


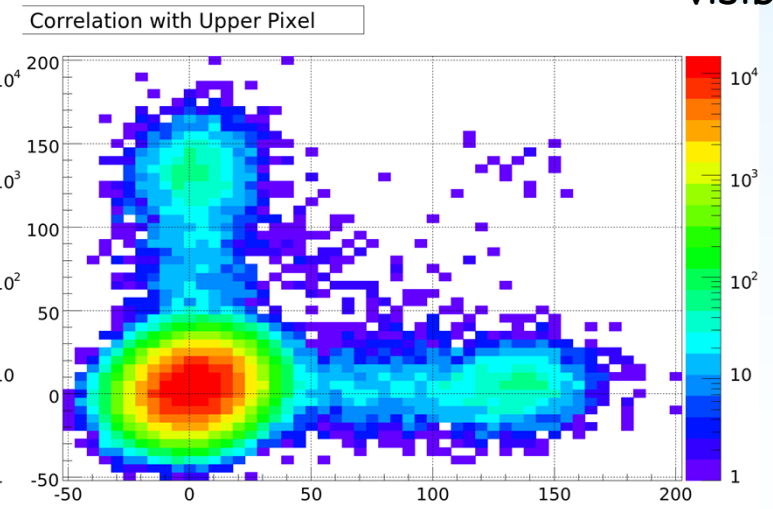
AGIPD02 - Charge Sharing





- Clear separation of photon peak (17.5 keV) from noise
- No significant charge sharing or crosstalk visible





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AGIPD02 – Storage Cell Variations

- Investigation of storage cell variations (LPPFET) using the internal current source
- Sensor voltage 120 V

- *Writing Single – Reading Single*:

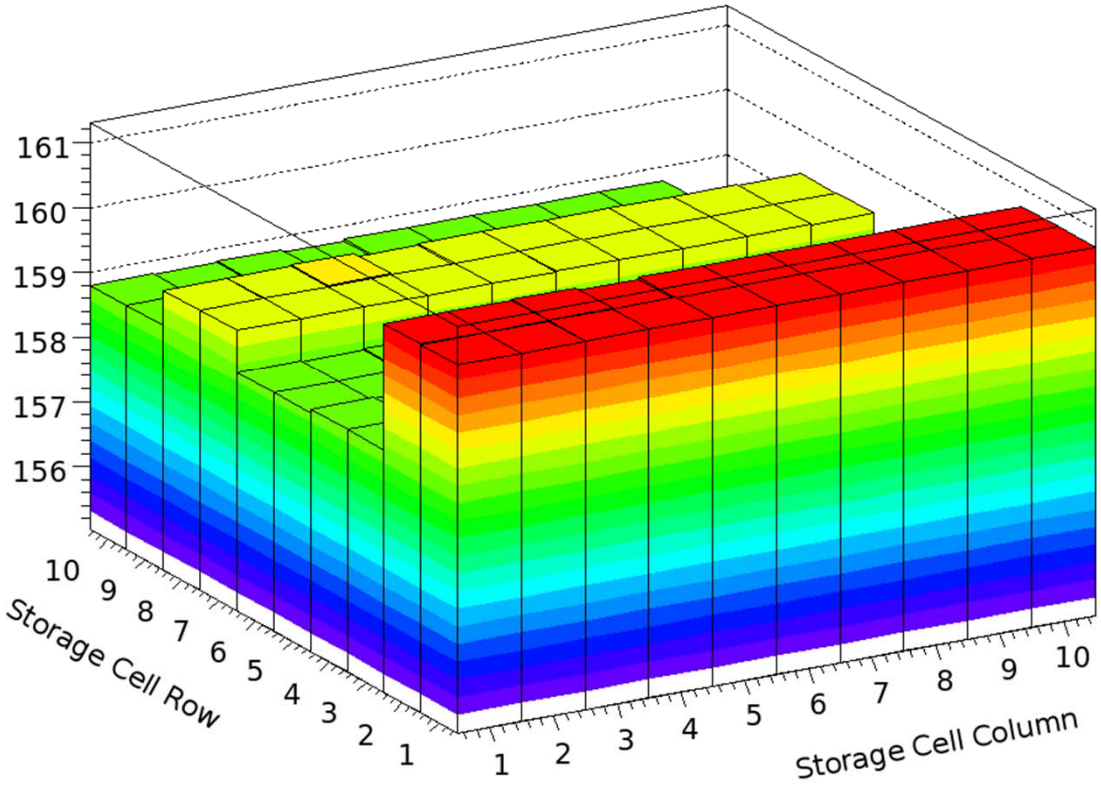
  - Write mode: Selecting single storage cell, writing value with the internal current source and different integration times

  - Read mode: Selecting single storage cell, precharging of the bus using "precharge mode", reading of value

- Fitting of the gain (arb. units)

AGIPD02 – Storage Cell Variations

Storage cell matrix – Fitted gain – Pixel x3 y3



- Considerable variations along the storage cell rows

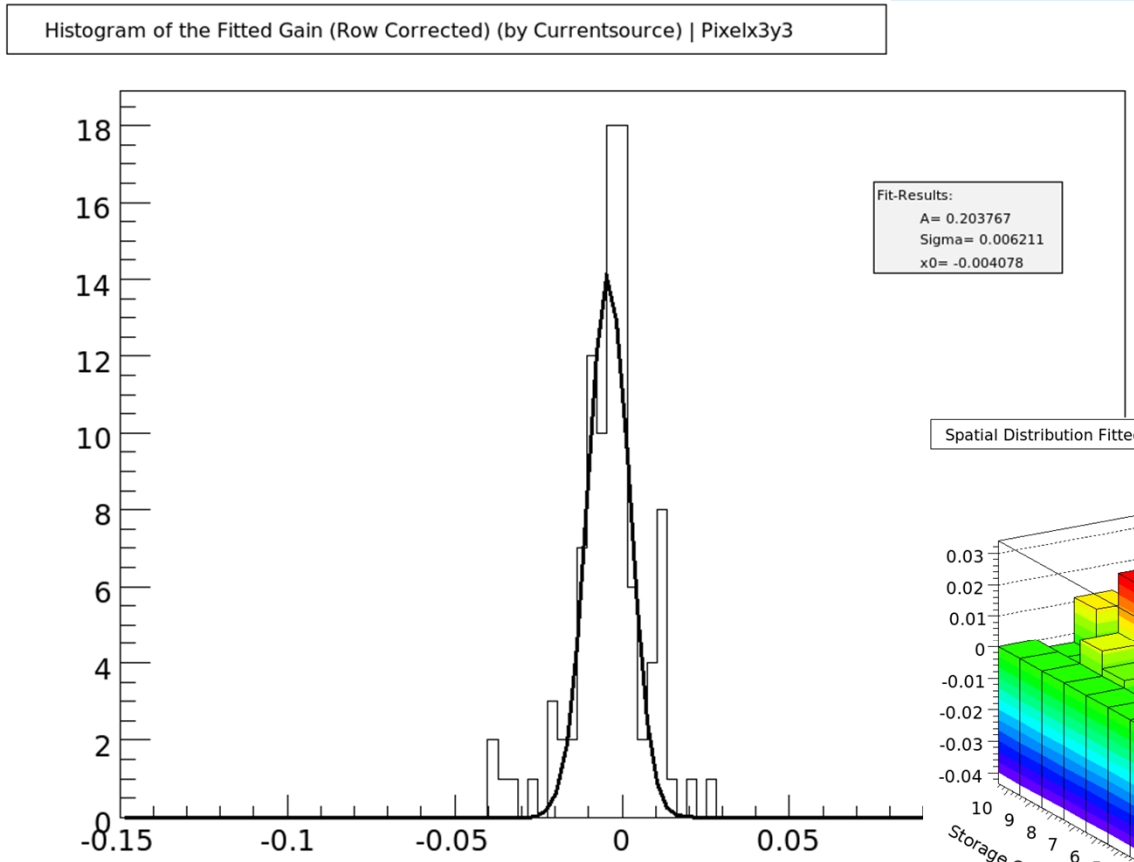
→ Puzzling behavior (maybe error in pattern?)

- Negligible variations along the columns

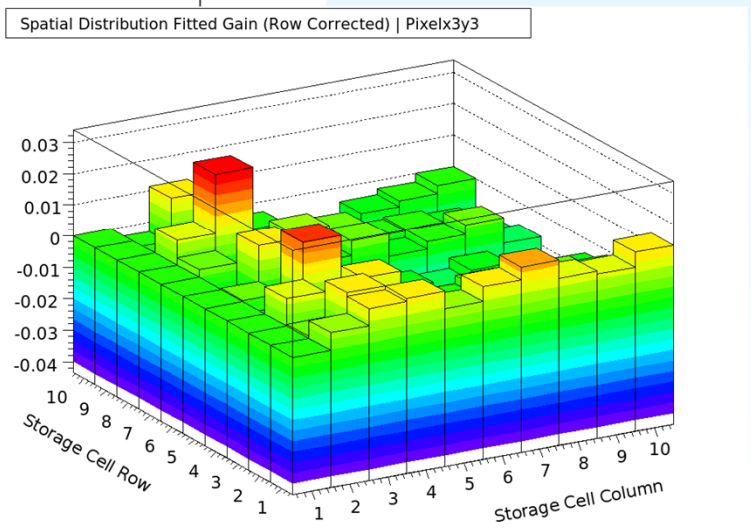
→**Rel. Variation: ±0.65 %**

→Applying simple correction by subtracting row offset value

AGIPD02 - Storage Cell Variations



Variation: ±0.01 %



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AGIPD02 – Storage Cell Variations

- Same measurement as before, but…
- *Writing Global – Reading Single*:

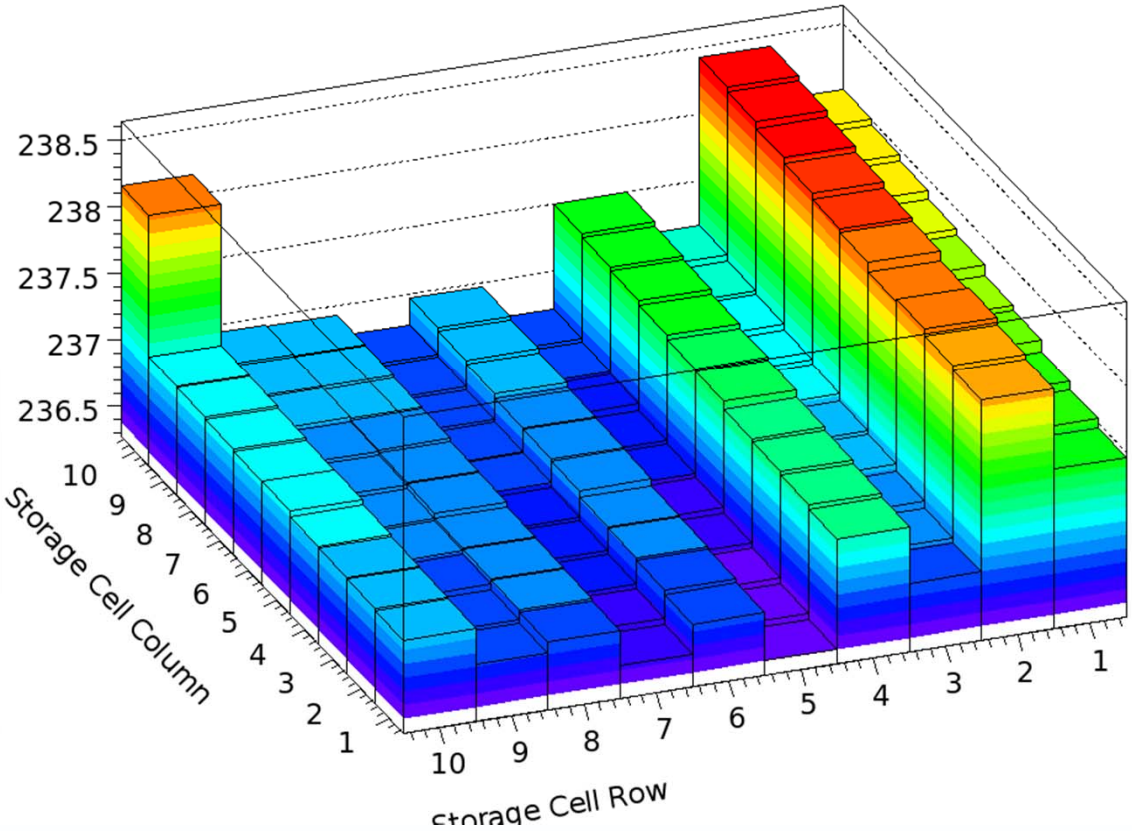
  - Write mode: Connecting **100** storage cells, writing value with the internal current source and different integration times

  - Read mode: Selecting single storage cell, precharging of the bus using "precharge mode", reading of value

- Measurement of realistic scenario:
  Writing on first storage cell,
  then reading sequentially of first storage cell

AGIPD02 – Storage Cell (SC) Variations

Storage cell matrix – Fitted gain – Pixel x3 y3



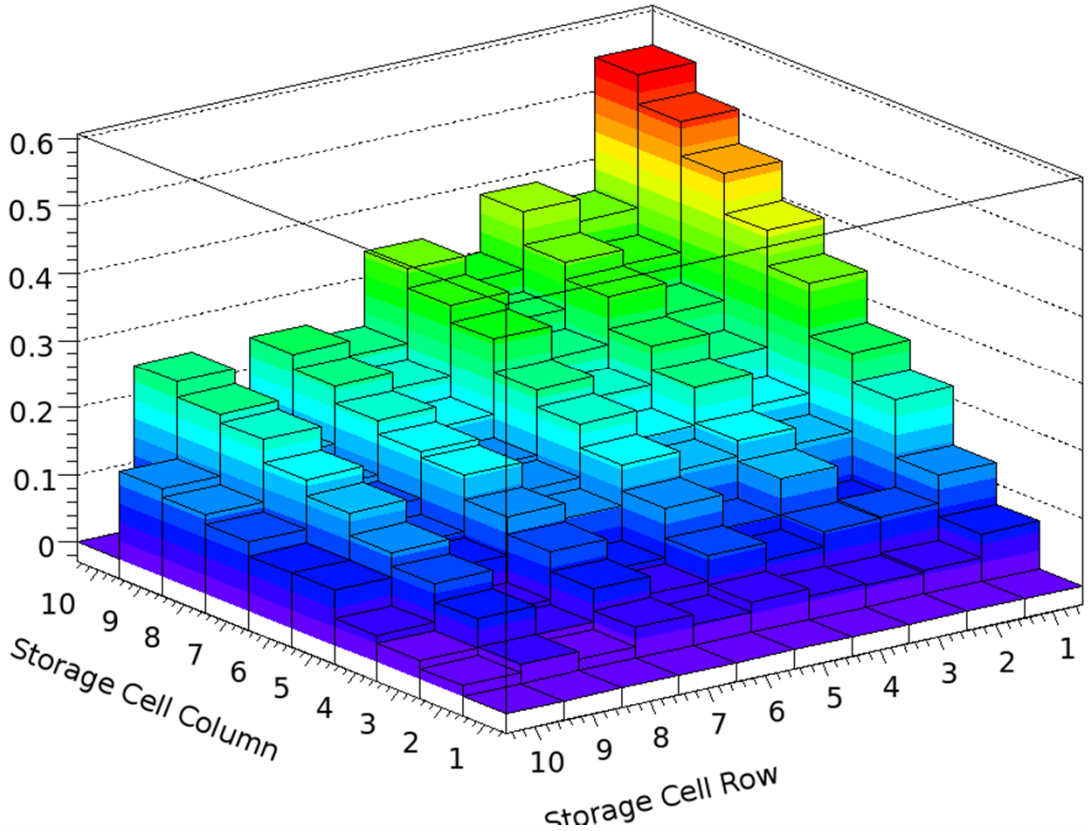
- Considerable variations along the storage cell rows
- Negligible variations along the columns

→**Rel. Variation: ±0.22 %**

→Applying simple correction by subtracting row offset value

AGIPD02 – SC variations (row correction)

Storage cell matrix – Fitted gain (row corrected) – Pixel x3 y3

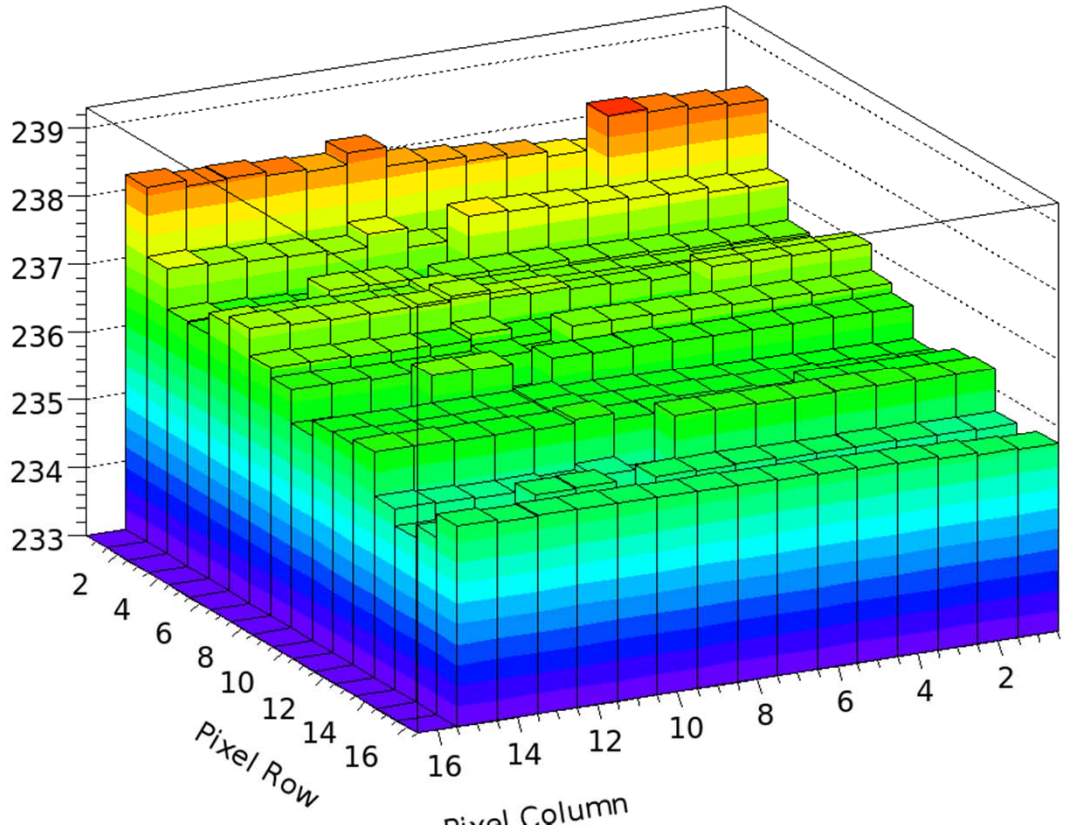


- After subtraction of "base value" (Column 1 value):

→ **Rel. Variation: ±0.05 %**

AGIPD02 – Pixel-2-Pixel Variations

Pixel matrix – Fitted gain – First storage cell



- "Realistic" measurement:

→Writing on globally on first cell
→ Reading first cell sequentially

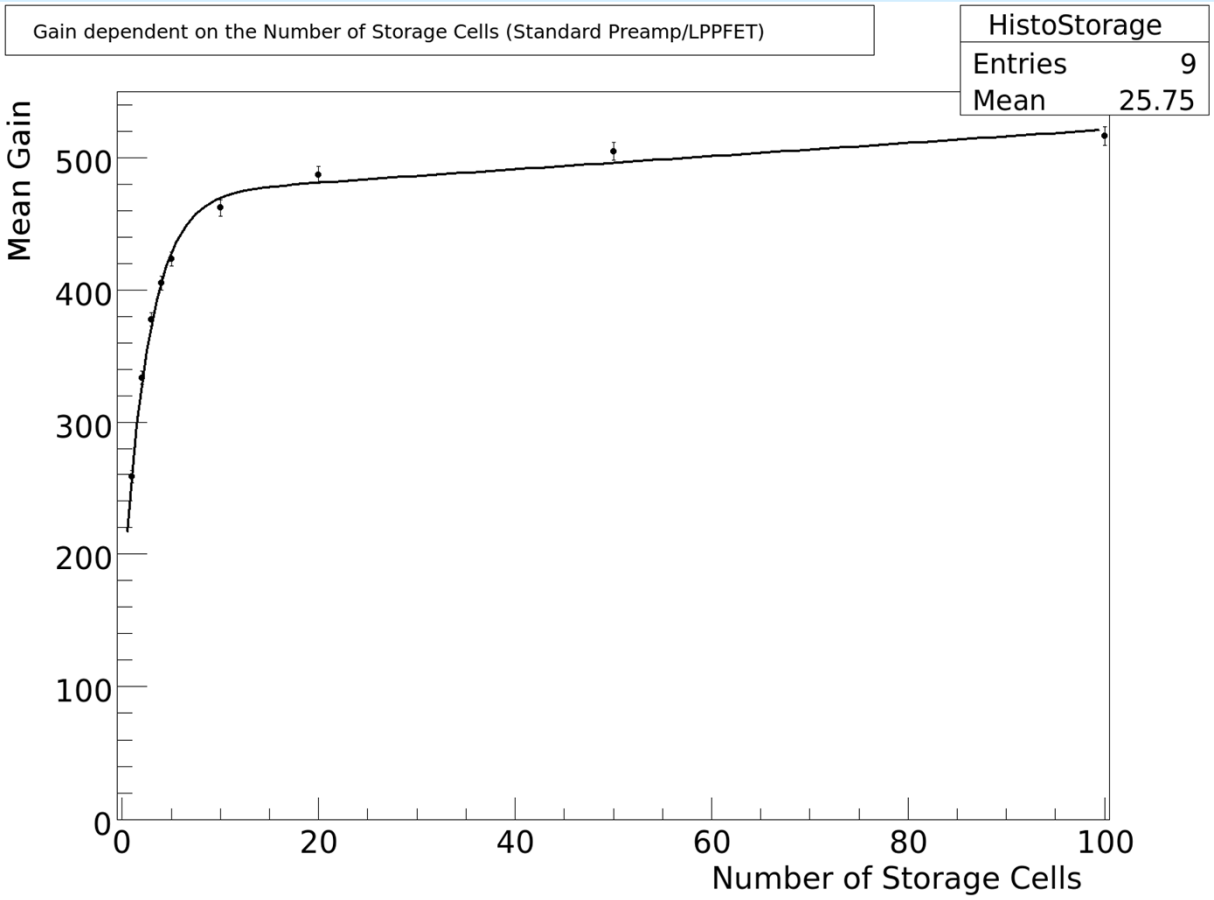
- Column 16: Active SC…
  …not activated

Results:

Mean gain:
(236.6 ± 0.7) ADC/int.time

→**Rel. Variation: ±0.28 %**

AGIPD02 - Pulseheight vs. Number of Storage cells



- Writing voltage with internal current source on different number of storage cells

- No precharging !!
→Less loss, when connecting more storage cells (to be expected!), as influence of parasitic capacitance of bus is reduced

- Repeatition of measurements with precharging of bus

Conclusions

- 'Write – Store – Precharge – Read' chain is working and controlable !
- No significant charge sharing or crosstalk visible
- Storage cells: Investigation of different Write-Read schemes

Common: Significant row-to-row variation
→ Puzzling two row dependence for SingleWrite-SingleRead, probabaly error in pattern

Negligible col-to-col variation

Leaking from storage cells visible

Single Write – Single Read: Rel. variation: 0.65 % (rms)
0.01 % (rms) (with simple offset correction)

Global Write – Single Read: Rel. variation: 0.22 % (rms)
0.05 % (rms)

Outlook

- Measurements of 'write-read processes' on storage cells using photons

→ Noise contributions from storage cells: Writing on storage cell – Precharging – Reading from single storage cell

→ Remeasure 'Single Write – Single Read' variations

- Investigation of dependence of gain vs. number of storage cell with precharging the bus

- … AGIPD03 !