# **Interface Electronics**

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#### **Outline**

- > Updates to interface electronics
- > Ideas for the backplane
- > Summary



#### **Two cables/quadrant:**

- >Ethernet cable: TCP/IP
- > Clock cable: RJ45
  - Bunch clock: 4.5MHz
    - Jump at "pre-warning for train" for ASIC and ADC
  - System clock: 99MHz continues: ADC\_clk < 49.5MS/s or less Continues running
  - Telegrams (train start & veto): allows 22bits/bunch
  - Status as return from detector head to C&C

Galvanic isolation at driver side



# News to interface: Reject from and to

- > Received from C&C
- Configured to ASIC with a CLK: 99MHz or 198MHz or ? needs

table free\_cells

- > Backend needs bunch\_nr(cell)
- Internal reject needs cell(bunch\_nr) Optional also to backend



# **News to interface: Layout**

#### Layout of digital part:

- > Length ~25-30cm (analogue part the same)
- Layout around XILINX need RAM on opposite side
- > Memory market: SODIMM modules much better than chips

But need height: Additional connector needed to generate the step



# **News on Interface: Layout**



27mm x 104mm

- Power for analogue part via power pins: need<10A, specs: 20A(40A) straight to wires
- Power for digital part: via 3+2 pins angled into PCB

specs: 2A/pin or 5A/pin

- > Option to return for sensing: but more complex cables. (5 pins)
- > SFP+ for the high speed data transfer (bi-directional fibres)
- > Remaining space with priorities:
  - JTAG
  - LED's

PCB's don't need to go to the end: More space than in the drawing



# Powering via external supply, regulator in detector head

Resistors in supply chain.

Component	resistivity	number	length	cross section	resistor
ZRMET	50mΩ, 15mΩ	12, 6			1.6mΩ
PCB / Cu-bar	$17 \mathrm{m}\Omega \mathrm{mm}^{2}/\mathrm{m}$		0.3m	4mm <sup>2</sup>	1.3mΩ
sub-D-Combo	< 1mΩ	1			1.0mΩ
cable	$17 \mathrm{m}\Omega \mathrm{mm}^{2}/\mathrm{m}$		5m	2.5mm² 🔇	34. mΩ
connector-supply	????				
				sum	40 mΩ

Dominant is cable

Current: <8A Two directions



# **Tolerable losses:**

- > External good quality power supply for analogue is possible
- > Less effort/space for DC/DC and filtering in analogue, NOT ZERO
- Digital need many voltages: DC/DC converter: Filter in detector head, good quality on supply side
- > Cable 5 x 2.5mm<sup>2</sup>: 12mm outer diameter: Sub-D-combo
- > If sense, than parallel thinner cable into same connector.





- 400 pin connector and not 500 pin avoids complexity of blind holes Option under investigation
- We need vacuum tightness, micro-via's from both sides
- bottom distance fits to connector analogue-digital-part: Everything behind sensor region **Peter Göttlicher** | Interface Electronics | October 5<sup>th</sup>, 2010 | Page 8/13

#### The connector as a whole: Details on next slides: $40 \times 10 \text{ pins}$ , $100\Omega$



power, spare Analogues, surrounded to GND or slow-signals

HV, power, digital control

- > 5 differential pairs for ASIC-control, spare region: up-to-date status?
- Slow control of PCB in vacuum via I2C+auxilary power enable to allow an easy power-off select as an option
- > HV and power (one voltage) included, might ease the assembly comments? Up-to-data current: 10 pins\*2A
- > GND definition somewhere in the vacuum:
  - GND and GND\_supply as different signals
  - GND and V with sense return
  - Power and HV supplie(s)/module



	A51-p	A51-n				V_supply	V_supply-Asic			
			А56-р	A56-n						
	А52-р	A52-n				A61-p	A61-n			
GND			А57-р	A57-n				enable		
	А53-р	A53-n				A62-p	A62-n			
			А58-р	A58-n	$\sim$			V_aux		
	А54-р	A54-n				A63-p	A63-n			
			А59-р	A59-n	Z			V-sense		
	А55-р	A55-n			<b>(</b> ]	A64-p	A64-n			
			A60-p	A60-n				G-sense		
								Static		
								signals		

#### **Analogue differential pairs:**

- Surrounded by GND
- > Only diagonal neighbour: here 500 pin offers more safety-margin
- Sometimes "static signals" on the diagonal



		A01-p			V_supply	-Asic				D1-p	D
/_supply-Asic							select	D2-p	D2-n		
		A02-p			A61-p	A61-n				D3-p	D
_supply-Asic							enable	D4-p	D4-n		
		A03-p			А62-р	A62-n				D5-p	D
_supply-Asic				$\sim$			V_aux	I2C_dk	I2C_data	GND_sup	ply
		A04-p			А63-р	A63-n		HV*1/4			
ND-supply				Z			V-sense		HV*1/2		
		A05-p			A64-p	A64-n				HV*3/4	
ND-supply				0			G-sense				H
	Static		•				Static				
	eignale						sionals	240V	480V	720V	Q
Spares							- grinerio	factor AC	to DC used	as safety n	nan

#### 5 differential pairs,

more on other end of connector, if needed

- Surrounded by GND or power
- > Only diagonal neighbour
- > Sometimes "static signals" beside

**POWER and GND** supply at edge to allow larger vias

HV: stepped to stay within connector defining 240V-AC + safety margin



#### Quantitatives for drops between quadrant-control and vacuum

#### Component resistivity number length cross section resistor Possible positions for bonding voltage regulators HDI $17 \text{m}\Omega \text{ mm}^2/\text{m}$ PCB in vacuum connector to <17 1mO $1.7 \text{ m}\Omega$ backplane 10 at quadrant to $17 \text{m}\Omega \text{ mm}^2/\text{m}$ $1.1 \text{ m}\Omega$ backplane/Cu-bar 0.4m 6mm<sup>2</sup> connector sideboard $\sim m\Omega$ 4 x 35µm x 5mm = side board. w/o $17m\Omega \text{ mm}^2/\text{m}$ $0.7 \text{mm}^2$ copper bar <0.2m $5 \,\mathrm{m}\Omega$ in vacuum with ~10 mΩ minimized sum

2 directions.

I<sub>max</sub>, I<sub>switched</sub> ?..... 0.5A / ASIC => 8A

160mV =>

Voltage regulators compensate cable drop and heat floating supply in rack

#### Summary

- > Details are updated: Keep every thing behind sensor
- > No contact to design of the PCB in vacuum, ... proposal, no decisions
- > Powering with reasonable losses in the cables