WP 2.5: Control system

> **Disclaimer**

> **Signals from Clock&Control**

> **Handling the control from WP76 inside interface electronics (WP2.4)**

>**Summary**

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Disclaimer

WP2.5 Control system

Long time ago

WP2.5 was given/taken away from AGIPD

……. Common WP for all XFEL 2D+….

There it is called Clock & Control

~~No more a WP2.5~~

Therefore only:

Signals from C&C

… what to do with it inside detector head

Signals from Clock & Control

- Clock & Control is a μTCA based design
  - Receiving signals from XFEL-accelerator and performance monitor
  - Translating to a limited number of signals for the detector head: Module + HDI/ASIC
- To Detector head
  - TCP/IP for slow control and FIRMWARE-boot: μC , FPGA
    processor of C&C gets the management and control of both
  - clocks from XFEL:
    - Train start: As early to power up (milli second?
    - System clock <~ 100MHz, synchronous to bunches (bunches at 4.5MHz)
    - Data stream per bunch : Telling a bunch number to reject
      random order, random delays
      or actual bunch number, consistency check
      and train number, …
  - return signal: Status like a busy.
- Interface electronics (quadrant) will do
  - book keeping
  - translation for ASIC
  - inclusion via modules into data stream
  - and via interrupting the μC to C&C-processors

Galvanic isolation at input of detector head: No additional antennas/GND-loop

Handling the control from WP76 inside interface electronics (WP2.4)

Limited contacts in all connectors, specially to the HDI and the module board, defines all concepts

- Slow control to the module: I2C with 3 additional address/mode lines,

  μC of quadrant control via that I2C-network all modules

- Slow control to HDI?

- Slow control containing power management for HDI/ASIC?

- Fast control: 3000 bunches/train*10trains/second*1bit/bunch= 30000 bits/train fast?

  3 dedicated LVDS pairs quadrant-FPGA

- Firmware boot quadrant to module-FPGA

  Allows updates, remote debugging, user/application specific codes, calculations…

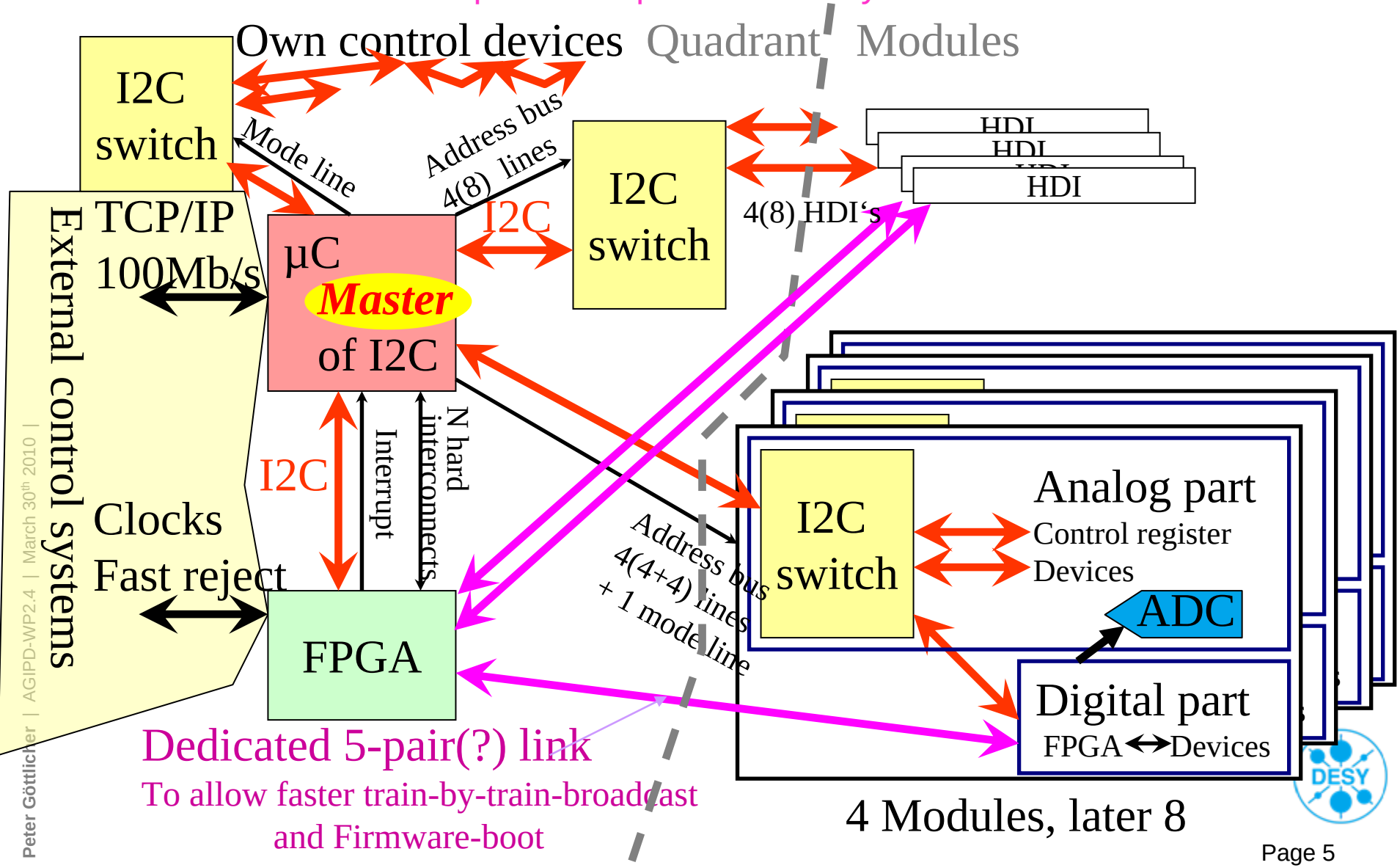
  2 more dedicated LVDS lines

- Fast clocks: ADC-conversions adjustable delay for scan in quadrant

C&C is master of everything via the TCP/IP

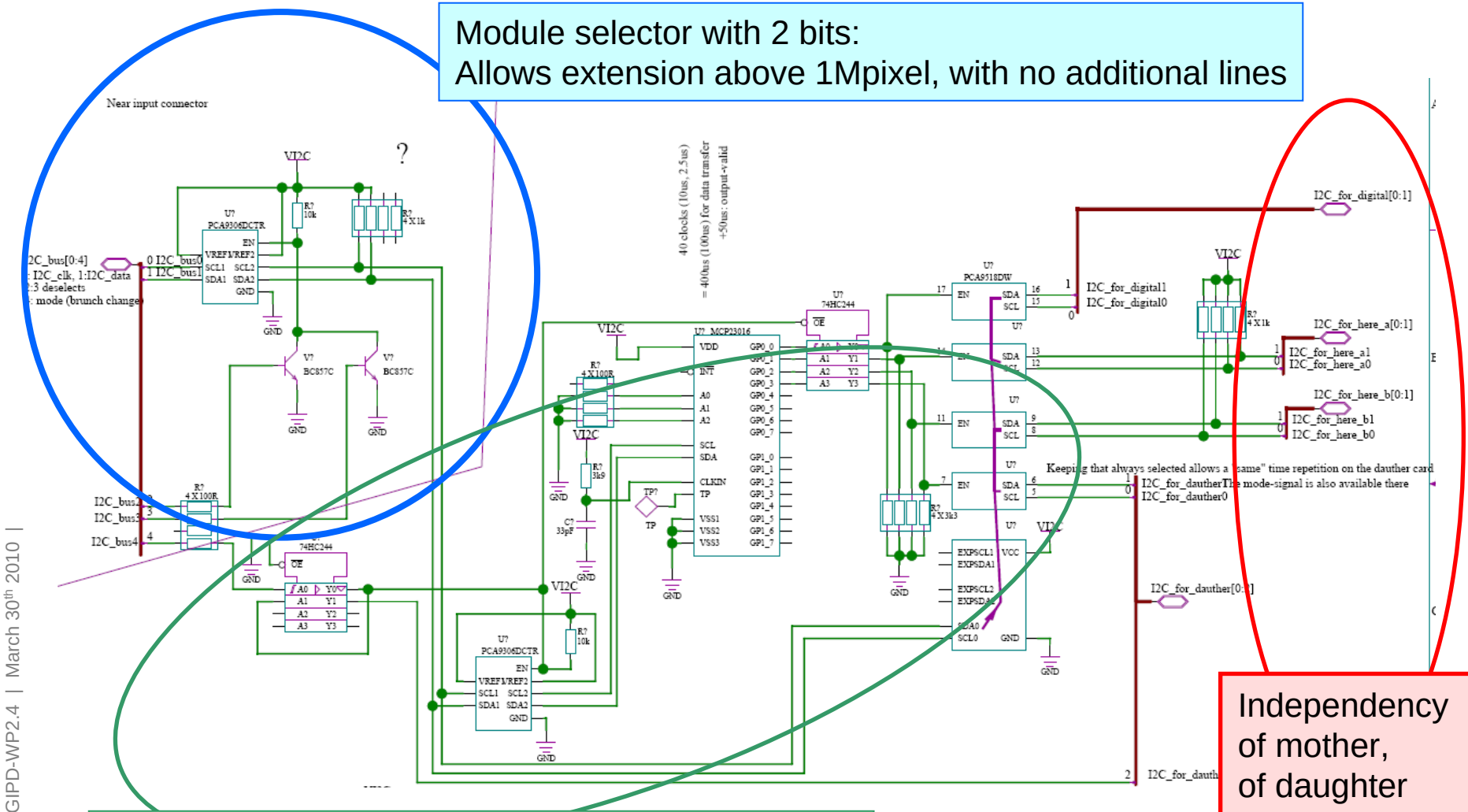
Reminder: Control concept - internal

- Main based on commercial I2C standards with segments
- Some links on custom protocol: special bunch sync.



I2C network

Module selector with 2 bits:
Allows extension above 1Mpixel, with no additional lines



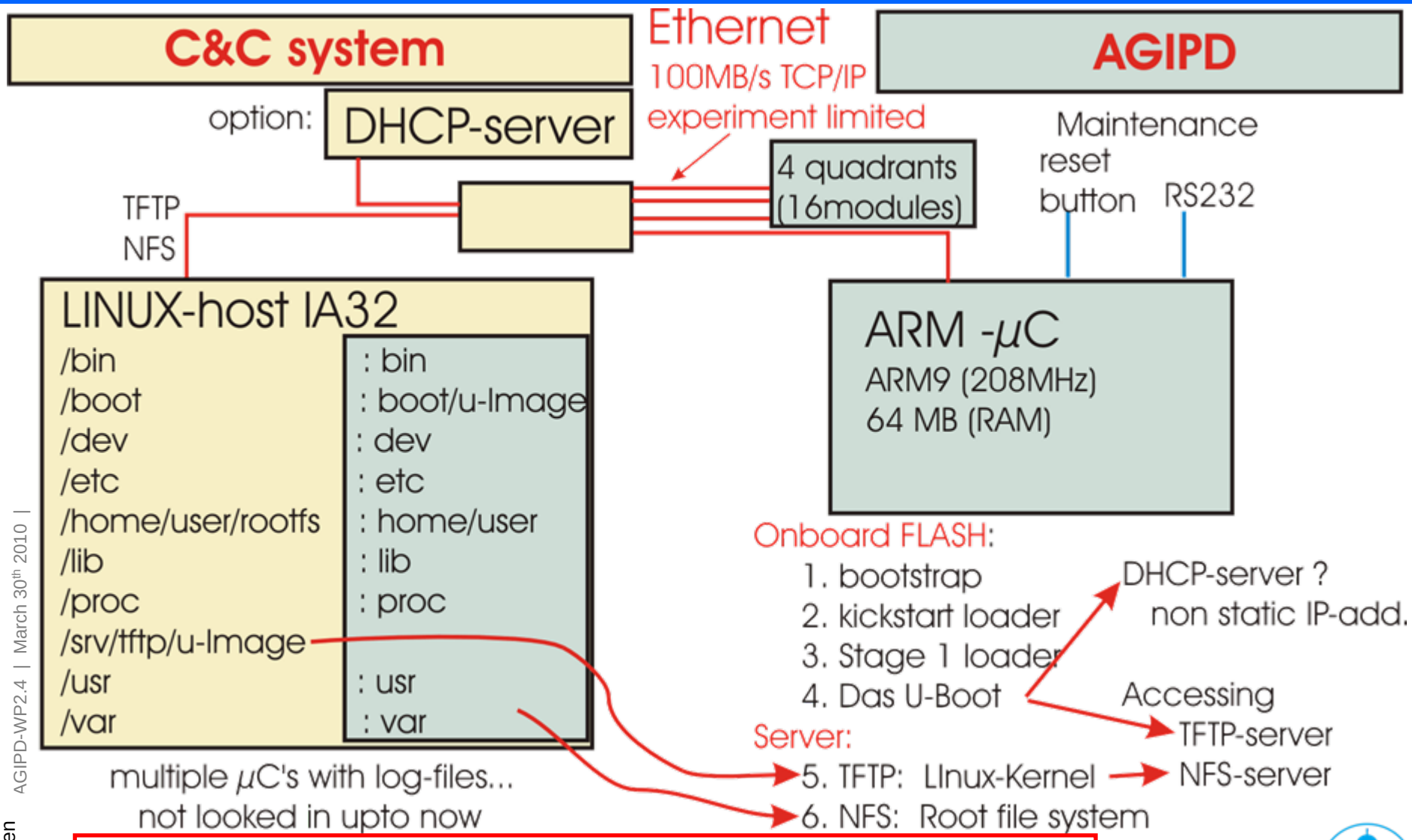
Mode bit allows to
Set internal brunches for
more internal chips, different logic levels/speeds
different od duplication of hardware

Independency
of mother,
of daughter
And digital part

Price:

Time for addressing !

Firmware management for microcontroller via C&C



Linux concept to get codes for µC onto C&C

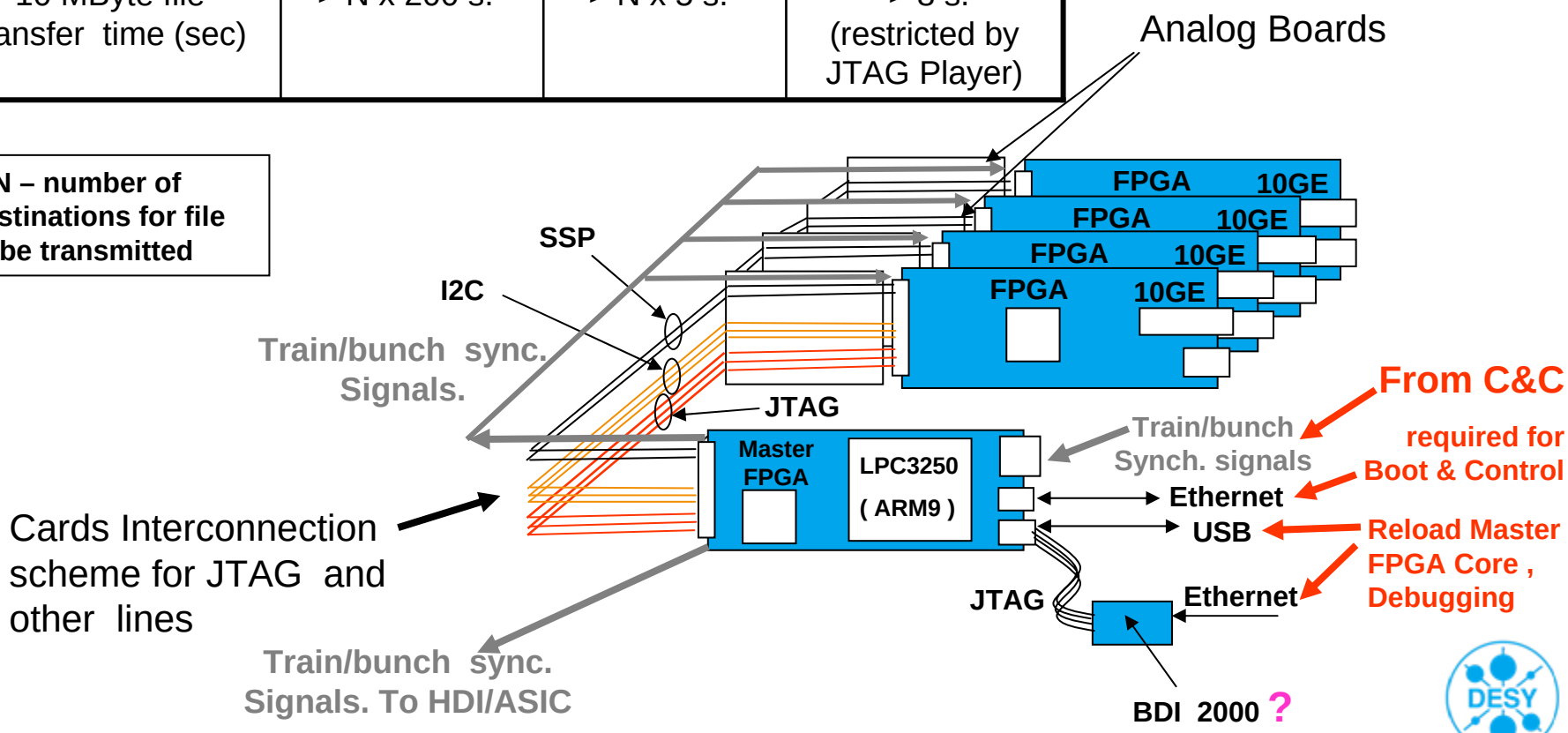
Driver needed to get interrupt to user level

Interconnection Topology, Data Transmission Rates and Line Count

Interface	I2C	JTAG	SSP (SPI)
Max bit/sec	~400 kb/s	~16 Mbit/s	> 50 Mbit/s
Total number lines (wires)	?	5	4
10 MByte file transfer time (sec)	> N x 200 s.*	> N x 5 s.*	> 8 s. (restricted by JTAG Player)

AGIPD internal: options inside detector head
One will be realized

*** N – number of destinations for file to be transmitted**



Summary

> WP2.5 not within AGIPD: See XFEL-WP76

> Next talk, by whom?

> Impact of WP76 to AGIPD:

- Quadrant communicates to C&C via TCP/IP and hard clocks
- Configures signals and distribute to ASIC/HDI and interface modules

  generates to correct relative timing
- WP76 master for FIRMWARE management, boot parameters, slow and fast control
- Internal slow communication via I2C: A network will be build up
- Internal train based communication via LVDS pairs: Quadrant to interface module

First the interface modules will be designed.

Quadrant follows and can be done long time by evaluation until spec's are fully settled.

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