REPORT ON

RADIATION DAMAGE IN CMOS STRUCTURES INTENDED FOR THE ADAPTIVE GAIN INTEGRATING PIXEL DETECTOR(AGIPD)

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ABSTRACT

The European XFEL is an 3.4-km-long facility which runs essentially underground and comprises three sites above ground. It will begin on the DESY site in Hamburg-Bahrenfeld and runs mostly underground to the XFEL research site, which is to be erected south of the town of Schenefeld (Pinneberg district, Schleswig-Holstein).
XFEL project is a fourth generation photon source and if compared it with other photon sources, the high peak brilliance and performance of this source would be unprecedented and open the doors for new areas in photon science.
With a pulse length below 100fs and an extremely high rate of 30000 flashes per second the European XFEL will have a worldwide unique time structure which enables researchers to make films of ultrafast processes.This demands the development of new detectors to the requirements imposed by the experiments while complying with the machine specific operation parameters.The Adaptive Gain Integrating Pixel Detector(AGIPD) is one response to the need of large 2D detectors,able to cope with the 5MHz repetition rate,as well as with the high dynamic range needed by XFEL experiments.

1. THE EUROPEAN XFEL

The European X-Ray Free Electron Laser(XFEL) under construction in Hamburg will provide fully coherent,< 100fs long X- ray pulses,with up to 10^{12} photons at 12 keV.The high intensity per pulse will allow recording diffraction patterns of small crystals in a single shot.2D detectors have to cope with a large dynamic range in the images,ranking from a single photon to $> 10^{4}$ photons/pixel.
Fig.1.1 shows that peak brilliance of the European XFEL compared to other synchrotron sources.

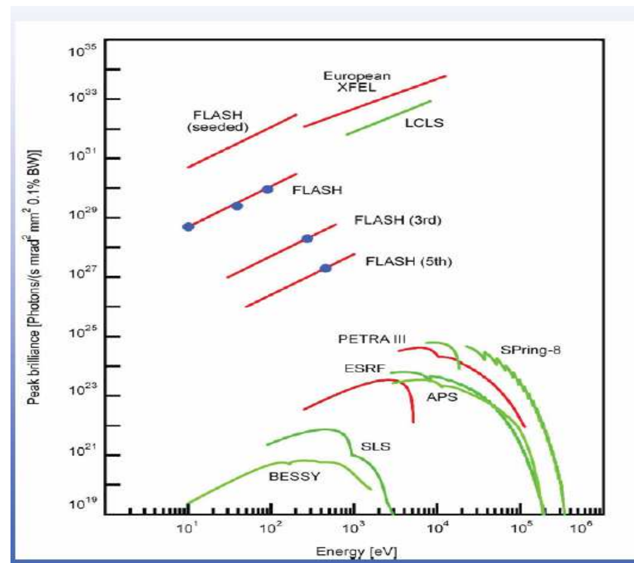


Figure1.1. Peak brilliance of the European XFEL compared to other synchrotron sources

Additional, the time structure of XFEL(c.f.fig.1.2):an electron bunch train with 10 Hz repetition rate,consisting of up to 3000 bunches with a 200 ns spacing.Because of that,the recorded images have to be stored for every pixel during the bunch trains and readout between bunch trains.AGIPD is one of 3 detector development projects supported by European XFEL to comply with these requirements.

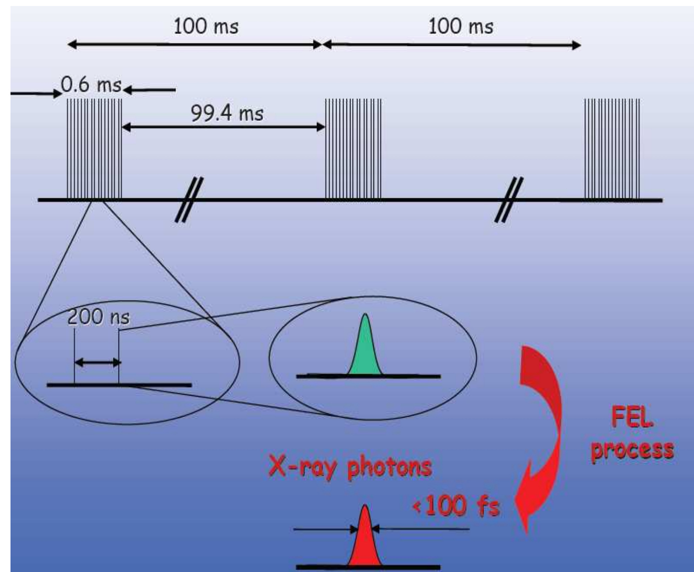


Figure1.2. Time structure of the European XFEL

2. THE AGIPD DETECTOR

The AGIPD project is led by PSI and is a collaboration between DESY – PSI – University of Bonn and the University of Hamburg. It is a project to build a pixellated solid state detector for the European XFEL. The goal is a 1000 by 1000 pixel detector, with 200 micron pixel size. The detector will be built with monolithic modules, as indicated in the figure 2.1 below;

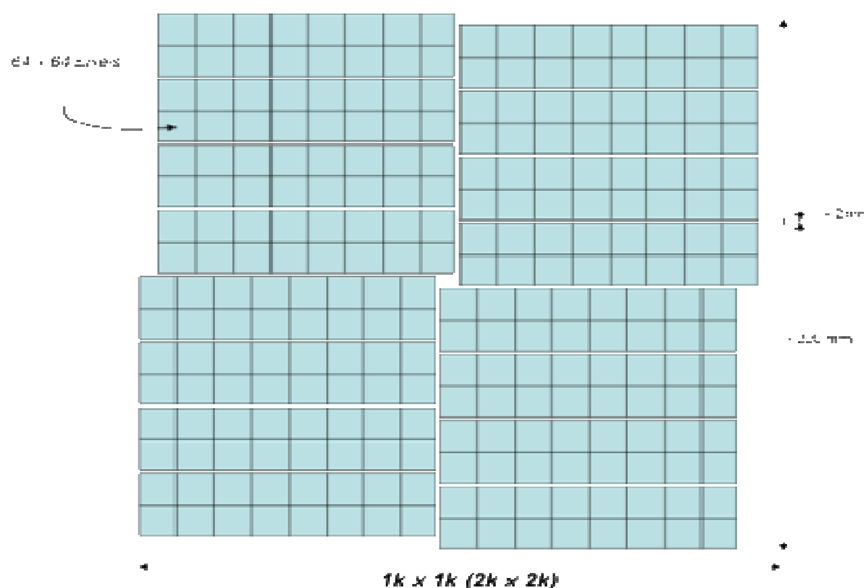


Figure 2.1. Sensor arrangement of the AGIPD detector

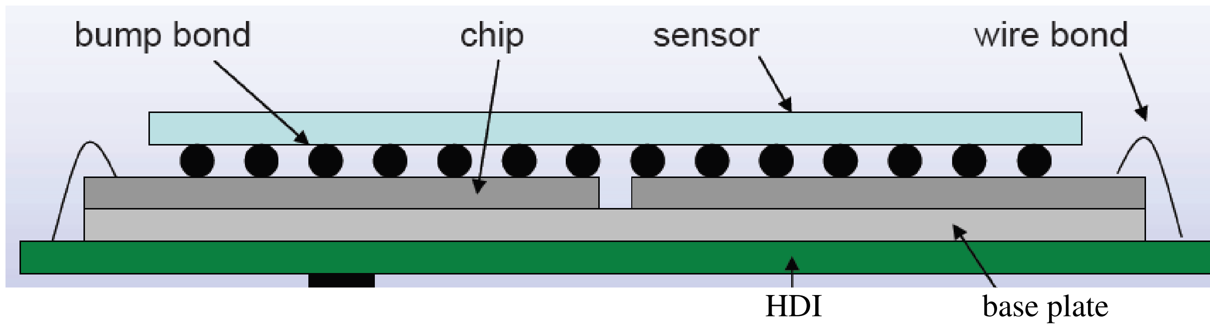


Figure2.2 Crossection of a AGIPD sensor module

The surfaces of each sensor is 102,6x25,8 mm^2 and does not contain any gaps or other dead area.The sensors are bump-bonded to 2x8 readout ASICS to form a module.A beam stop in front of the detector or a gas filled flight tube would cause a backround exceeding the actual signal by several orders of magnitude.Thus a central hole for the direct beam is required.
The analogue signals stored in the pipeline, an analoge memory,and then read out and digitized during the intervals between bunch trains. This pixel circuitry is shown in the following figure.
Each pixel in the ASIC has to cover a dynamic range from single photon sensitivity to 4×10^4 coincident photons. This high dynamic range cannot be implemented on a single gain stage—to detect the maximum number of photons, the gain of the readout amplifier has to be very small. However, to obtain single photon sensitivity, the gain has to be very high and the noise of the amplifier has to be low. Thus, a self-regulating, adaptive gain switching mechanism is employed.
However,since the readout of 200 frames from the chip will take several 10ms,signal drop caused by leakage currents in switches and capacitors becomes an issue and all analogue in formation is read before the encoded gain settings.The AGIPD consortium has identified this problem and is investigating leakage currents in the chosen 130 nm CMOS technology,also under the influence of temperature and radiation.

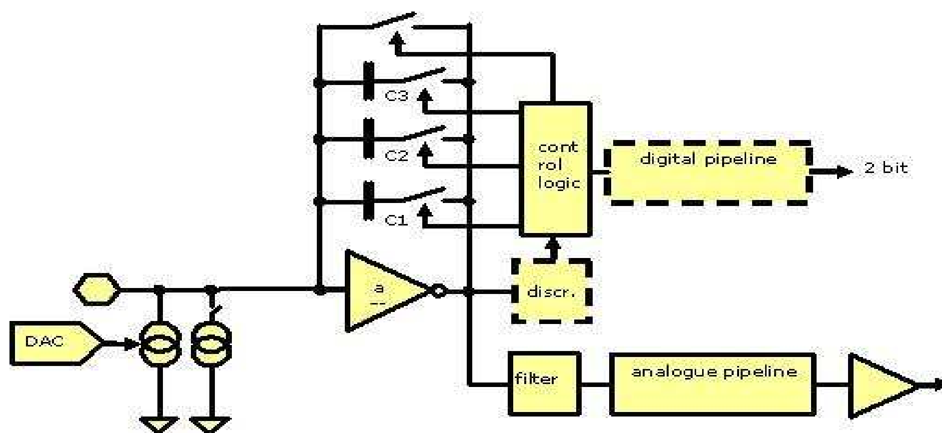


Figure2.3 Pixel circuitry of the AGIPD detector

3-RADIATION DAMAGE IN CMOS STRUCTURES

3.1 INTRODUCTION

In recent years a tremendous increase in use of electronic systems in space applications occured.This has drawn attention to the important influence of cosmic radiation on the characteristics of devices and circuits of the electronics systems.Taking into account the space-radiation environment in which the large number of electronic circuits are going to be introduced,investigations of the interdependence effects between the type, intensity,duration of irradiations typical of space environment have to be carried out on basic components like MOS and bipolar transistors.These basic components are indeedthe essential part of any circuit, thus the knowledge of irradiation effect on them is critical.
For this purpose, radiation damage in the CMOS transistors is investigated.

3.2 STRUCTURE OF CMOS TRANSISTORS

CMOS circuits use a combination of p-type and n-type metal-oxide-semiconductor field-effect transistors (MOSFETs) to implement logic gates and other circuits found in computers, telecommunications equipment, and signal processing equipment. Although CMOS logic can be implemented with discrete devices , typical commercial CMOS products are integrated circuits composed of millions (or hundreds of millions) of transistors of both types on a rectangular piece of silicon of between 10 to 400mm.[2]
The N device is manufactured on a P-type substrate. The P device is manufactured in an N-type well (n-well). A P-type substrate "tap" is connected to V_{SS} and an N-type n-well tap is connected to V_{DD} to prevent latchup.

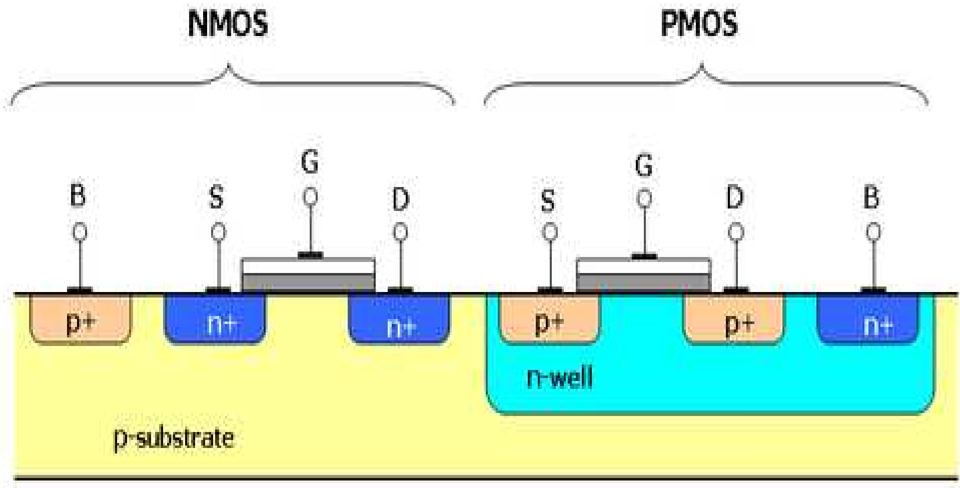


Figure3.2.1 Cross section of two transistors in a CMOS gate, in an N-well CMOS process

3. 3 CHARACTERISATION OF CMOS TRANSISTORS

3.3.1The operation of MOSFET

The operation of a MOSFET can be separated into three different modes, depending on the voltages at the terminals. In the following discussion, a simplified algebraic model is used that is accurate only for old technology. Modern MOSFET characteristics require computer models that have rather more complex behavior.

For an enhancement-mode, n-channel MOSFET, the three operational modes are:

Cutoff, subthreshold, or weak-inversion mode

When $V_{GS} < V_{TO}$:

where $\mathbf{V}_{TO}$ is the threshold voltage of the device.

According to the basic threshold model, the transistor is turned off, and there is no conduction between drain and source. In reality, the Boltzmann distribution of electron energies allows some of the more energetic electrons at the source to enter the channel and flow to the drain, resulting in a subthreshold current that is an exponential function of gate–source voltage. While the current between drain and source should ideally be zero when the transistor is being used as a turned-off switch, there is a weak-inversion current, sometimes called subthreshold leakage.

In weak inversion the current varies exponentially with gate-to-source bias V_{GS} as given approximately by

$$I_D \approx I_{D0} e^{\frac{V_{GS}-V_{th}}{nV_T}},$$

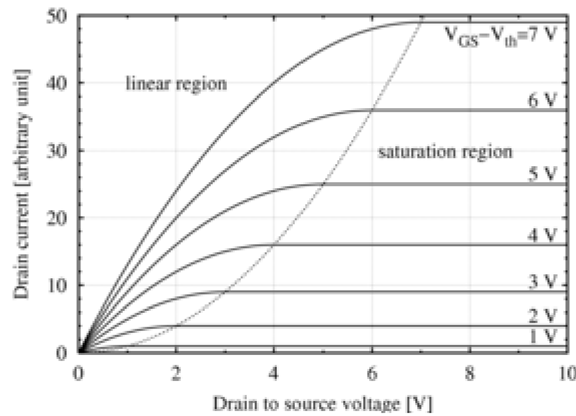
where I_{D0} = current at $V_{GS} = V_{TO}$ and the slope factor n is given by

$n = 1 + C_D / C_{OX}$,

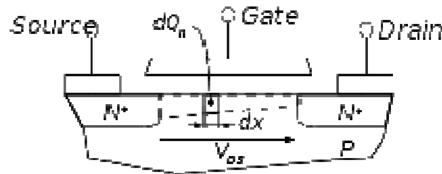
with C_D = capacitance of the depletion layer and C_{OX} = capacitance of the oxide layer. In a long-channel device, there is no drain voltage dependence of the current once $V_{DS} >> V_T$, but as channel length is reduced drain-induced barrier lowering introduces drain voltage dependence that depends in a complex way upon the device geometry (for example, the channel doping, the junction doping and so on). Frequently, threshold voltage $\mathbf{V}_{TO}$ for this mode is defined as the gate voltage at which a selected value of current I_{D0} occurs, for example, I_{D0} = 1 μA, which may not be the same $\mathbf{V}_{TO}$-value used in the equations for the following modes.

Some micropower analog circuits are designed to take advantage of subthreshold conduction.By working in the weak-inversion region, the MOSFETs in these circuits deliver the highest possible transconductance-to-current ratio, namely: $g_m / I_D = 1 / (nV_T)$, almost that of a bipolar transistor.

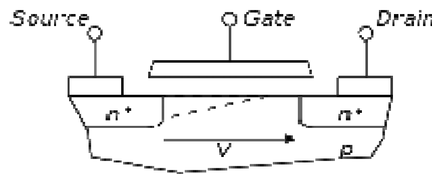
The subthreshold *I–V curve* depends exponentially upon threshold voltage, introducing a strong dependence on any manufacturing variation that affects threshold voltage; for example: variations in oxide thickness, junction depth, or body doping that change the degree of drain-induced barrier lowering. The resulting sensitivity to fabricational variations complicates optimization for leakage and performance.



MOSFET drain current vs. drain-to-source voltage for several values of $V_{GS} - V_{TO}$; the boundary between **linear** (**Ohmic**) and **saturation** (**active**) modes is indicated by the upward curving parabola.



Cross section of a MOSFET operating in the linear (Ohmic) region; strong inversion region present even near drain.



Cross section of a MOSFET operating in the saturation (active) region; channel exhibits **pinch-off** near drain.

Triode mode or linear region,

When $V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} - V_{th})$

The transistor is turned on, and a channel has been created which allows current to flow between the drain and the source. The MOSFET operates like a resistor, controlled by the gate voltage relative to both the source and drain voltages. The current from drain to source is modeled as:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

where μ_n is the charge-carrier effective mobility, W is the gate width, L is the gate length and C_{ox} is the gate oxide capacitance per unit area. The transition from the exponential subthreshold region to the triode region is not as sharp as the equations suggest.

Saturation or active mode

When $V_{GS} > V_{th}$ and $V_{DS} > (V_{GS} - V_{th})$

The switch is turned on, and a channel has been created, which allows current to flow between the drain and source. Since the drain voltage is higher than the gate voltage, the electrons spread out, and conduction is not through a narrow channel but through a broader, two- or three-dimensional current distribution extending away from the interface and deeper

in the substrate. The onset of this region is also known as **pinch-off** to indicate the lack of channel region near the drain. The drain current is now weakly dependent upon drain voltage and controlled primarily by the gate–source voltage, and modeled very approximately as:

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS}).$$

3.3.2 Threshold Voltage

The linearly extrapolated threshold voltage with zero substrate bias is in saturation:Gate and drain are connected to one voltage source,source and bulk are connected to ground.The voltage is swept in order to find the maximum slope of the square root of the drain current as a function of the gate voltage.A linear regression is performed around this operating point;

$$\sqrt{I_{DS}} = \sqrt{K'/2 * W_{eff} / L_{eff}} .(V_{GS} - V_{TO})$$

The voltage sweep is positive for n-channel devices and negative for p-channel devices.Then intercept point with the X-axis is taken as V_{TO} .

W_{eff} =Effective width of the transistor

L_{eff} = Effective length of the transistor

I_D = Drain current

V_{GS} = Gate-source voltage

V_{DS} = Drain-source voltage

V_{TO} = Threshold voltage

K' =Gain Factor

3.3.3 Gain Factor

KP is measured from the slope of the large transistor,where W_{eff} / L_{eff} ~ W/L.

The drain voltage is forced to 0.1 V,source and bulk are connected to ground.The gate voltage is swept to find the maximum slope of the drain current as a function of the gate voltage.A linear regression is performed around this operating point;

$$I_{DS} = K'.(W_{eff}/L_{eff}).V_{DS}.(V_{GS} - V_{TO} - V_{DS}/2)$$

$$K' = (dI_D/dV_{GS}).(1/V_{DS})*(L/W)$$

The voltage sweep is positive for n-channel devices and negative for p-channel devices.

3.4 N-MOS and P-MOS IONIZATION DAMAGE

In MOS transistors, the gate oxide is the most sensitive part. After irradiation electron-hole pairs are created. Holes are trapped in the oxide and traps are created at the Si/SiO2 interface. Holes trapped in the oxide induce a threshold voltage shift, negative for both NMOS and for PMOS transistors. The additional interface states will degrade both the transconductance and the subthreshold slope, inducing a further threshold shift. The threshold shift and the variation of sub-threshold slope also increases the off-state leakage current, and,consequently, the power consumption of the device.

The electrons are relatively mobile and are collected by either the gate or channel fairly rapidly. Holes typically move more slowly, hopping from site to site until they reach the silicon-oxide interface. Here many of the holes are trapped by defects near the Si-SiO_2

interface.These trapped holes (Figure 3.4.1) generate a fixed positive charge, which can affect the characteristics of the transistor, generating shifts in the operating threshold of the device. Interfaces states also act as scattering centres,thus reducing the mean free path of the charge carriers.In turn mobility and gain factor reduced.

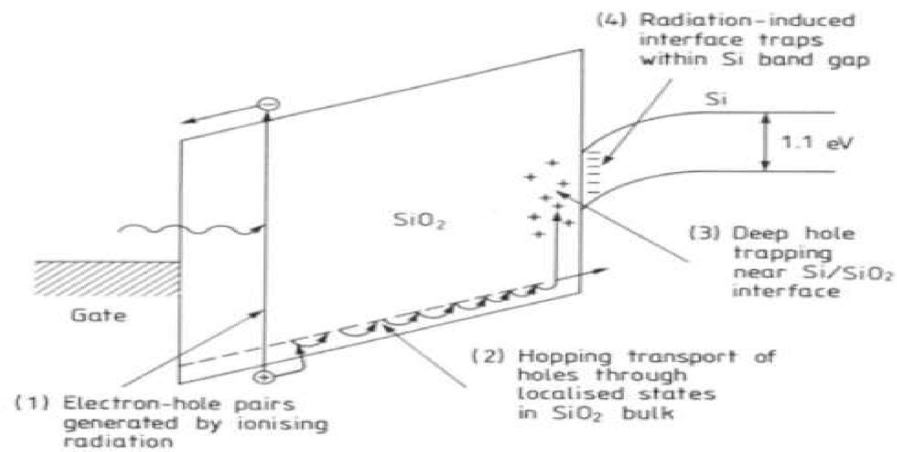


Figure 3.4.1 Energy band schematic of the motion of electrons and holes produced in a silicon gate oxide.

3.5 TEST&IRRADIATION ON THE HPAD 0.1 CHIPS

For the test measurement,Chip#5 and Chip#6 were irradiated up to 10 MGy at the DORISIII beamline F4 to identify critical points.Gain factor(K') and Threshold voltage(Vth) were calculated and visualised for with different doses(0Gy,1MGy,10MGy).

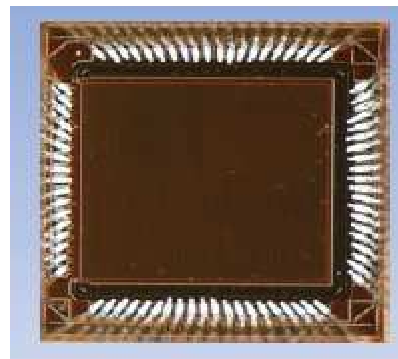


Figure3.5.1 HPAD 0.1 Chip

Figure3.5.2 DorisIII Beamline F4

3.5.1 Experimental Results

<u>Part1</u> K'(Gain factor) is measured from the slope of the large transistor,where W_{eff}/L_{eff}) ~ W/L.

$\mathbf{I}_{DS} = K'.(W_{eff}/L_{eff}).\mathbf{V}_{DS}.(\mathbf{V}_{GS} - \mathbf{V}_{TO} - \mathbf{V}_{DS}\mathbf{/2})$

$\mathbf{K}' = (d\mathbf{I}_D/d\mathbf{V}_{GS}).(1/\mathbf{V}_{DS})*(L/W)$ at 100mV

For DGNMOS transistor; W=7,0 µm and L=0,48 µm
For ZVTDGNMOS transistor; W=16 µm and L=0,56 µm
For DGPMOS transistor; W=9741,6 µm and L=5 µm

Gain factor of the transistors are calculated and visualized for different doses at the following figures.

<u>For 0 Gy:</u>

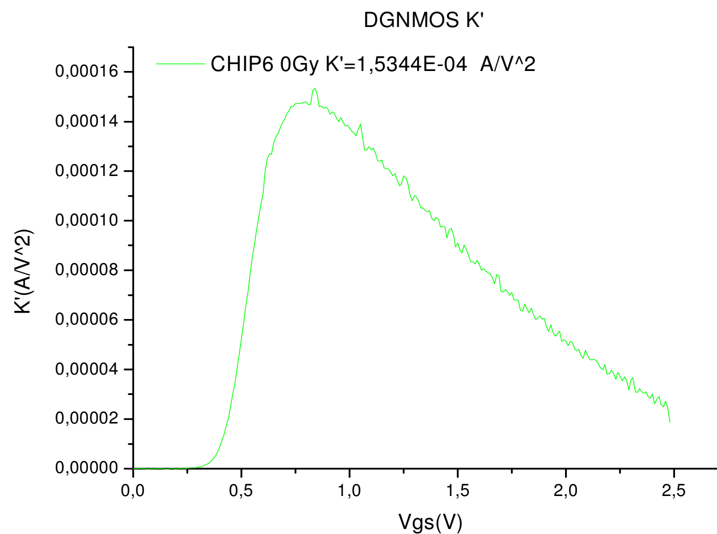


Fig.3.5.1.2 Gain factor of the DGNMOS used as current source in the ZVT sourcefollower for Chip6

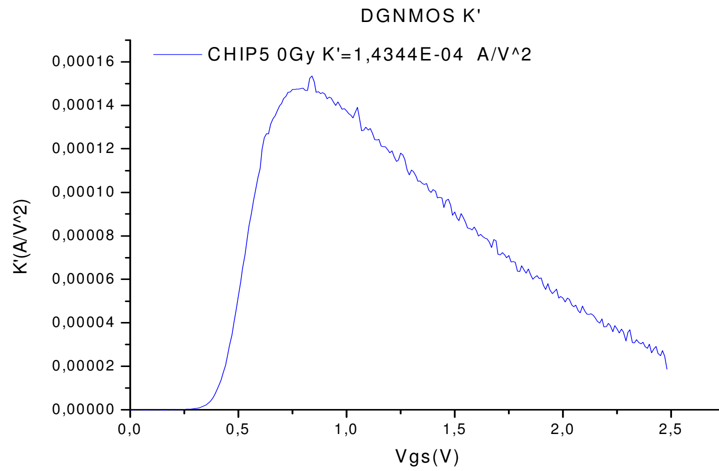


Fig.3.5.1.3 Gain factor of the DGNMOS used as current source in the ZVT sourcefollower for Chip5

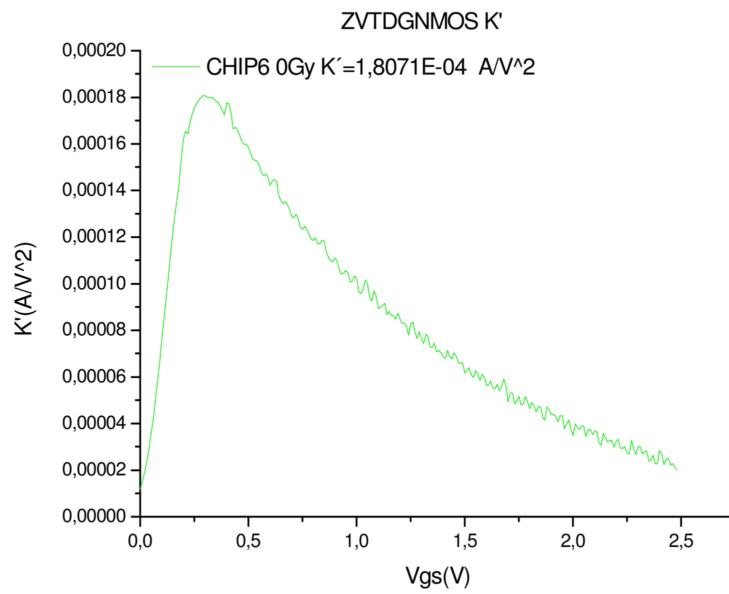


Fig.3.5.1.4 Gain factor of the ZVTDGNMOS used as current source in the ZVT sourcefollower for Chip6

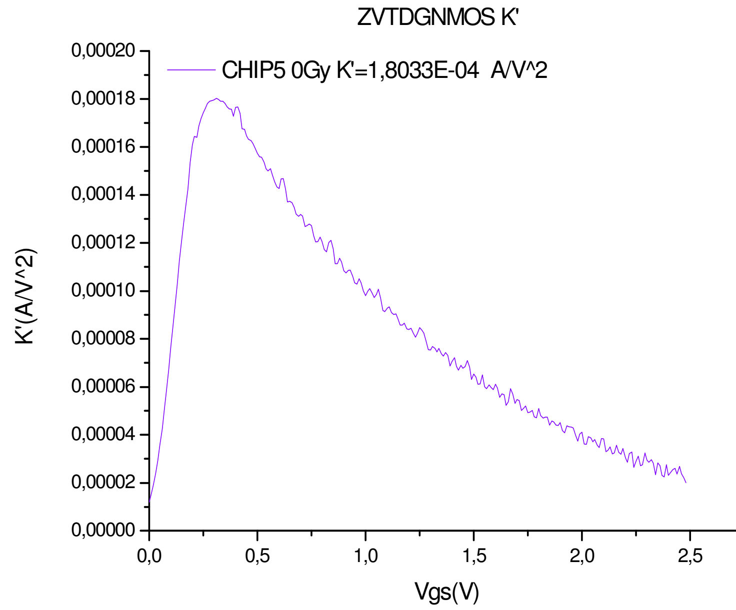


Fig.3.5.1.5 Gain factor of the ZVTDGNMOS used as current source in the ZVT sourcefollower for Chip5

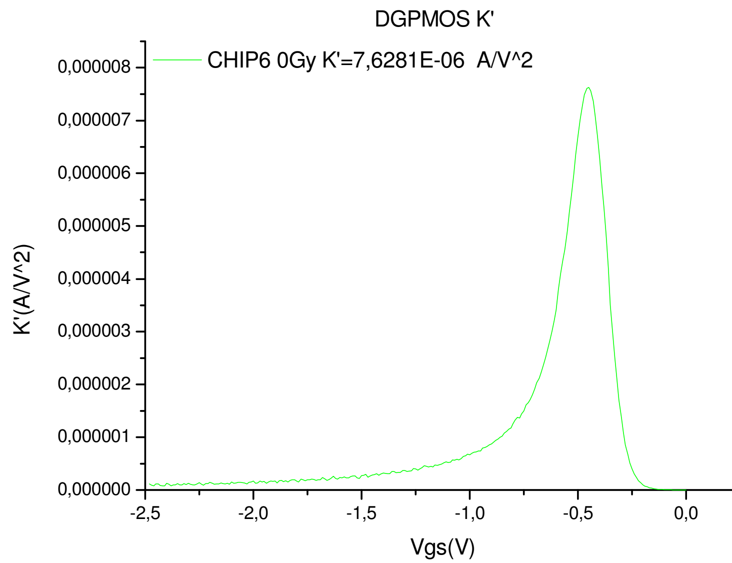


Fig.3.5.1.6 Gain factor of the DGPMOS used as current source in the ZVT sourcefollower for Chip6

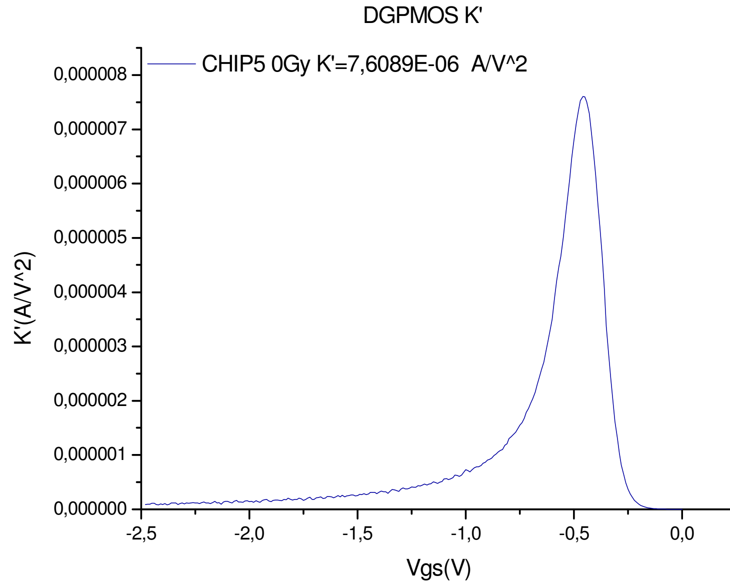


Fig.3.5.1.7 Gain factor of the DGPMOS used as current source in the ZVT sourcefollower for Chip5

For 1 MGy:

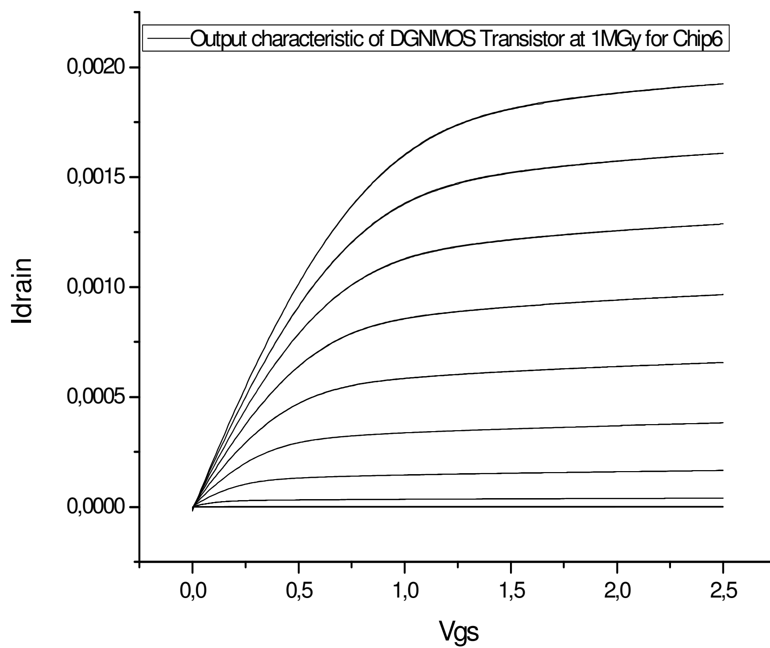


Fig.3.5.1.a Characteristic of the DGNMOS used as current source in the ZVT sourcefollower for Chip6

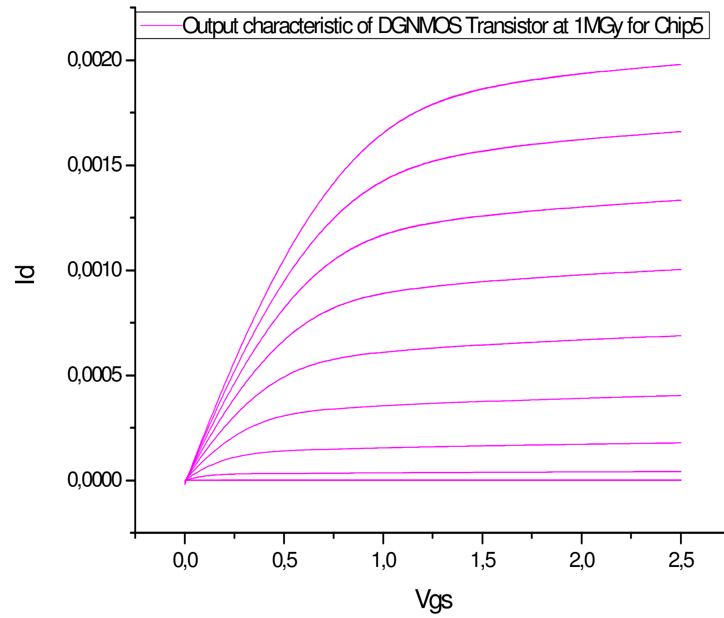


Fig.3.5.1.b Characteristic of the DGNMOS used as current source in the ZVT sourcefollower for Chip5

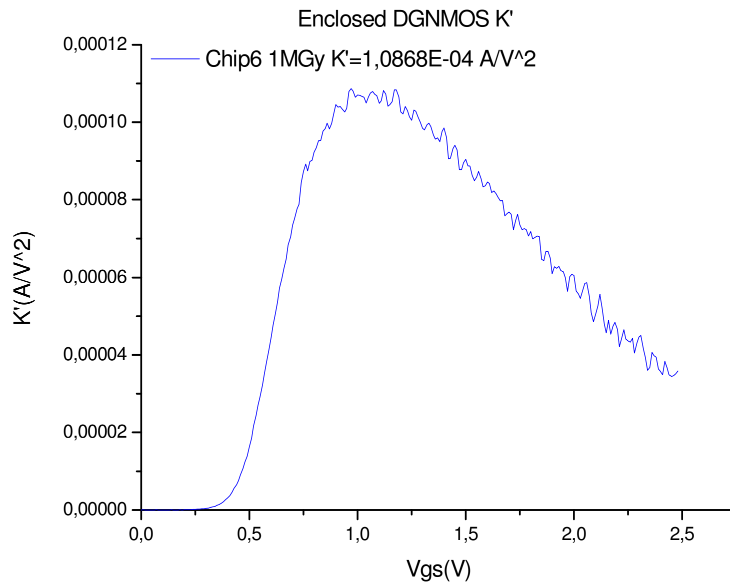


Fig.3.5.1.c Gain factor of the DGNMOS used as current source in the ZVT sourcefollower for Chip6

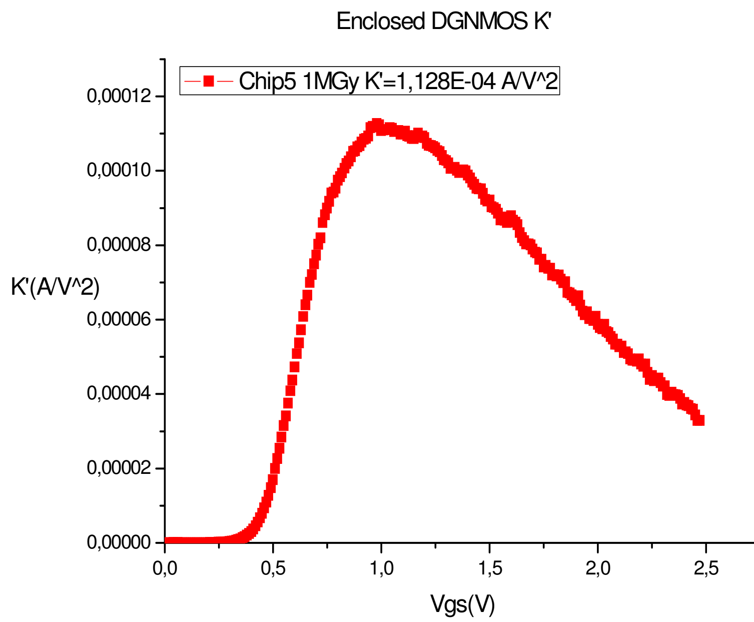


Fig.3.5.1.d Gain factor of the DGNMOS used as current source in the ZVT sourcefollower for Chip5

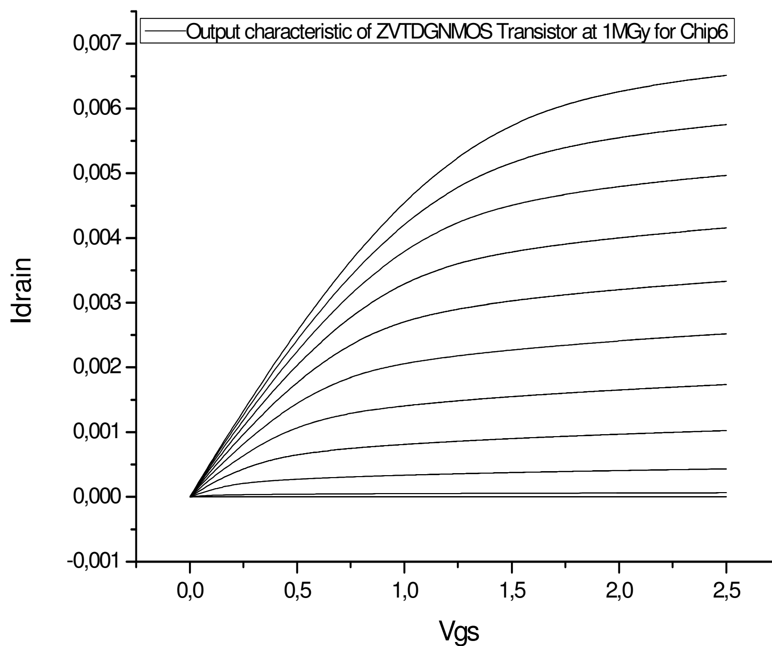


Fig.3.5.1.e Characteristic of the ZVTDGNMOS used as current source in the ZVT sourcefollower for Chip6

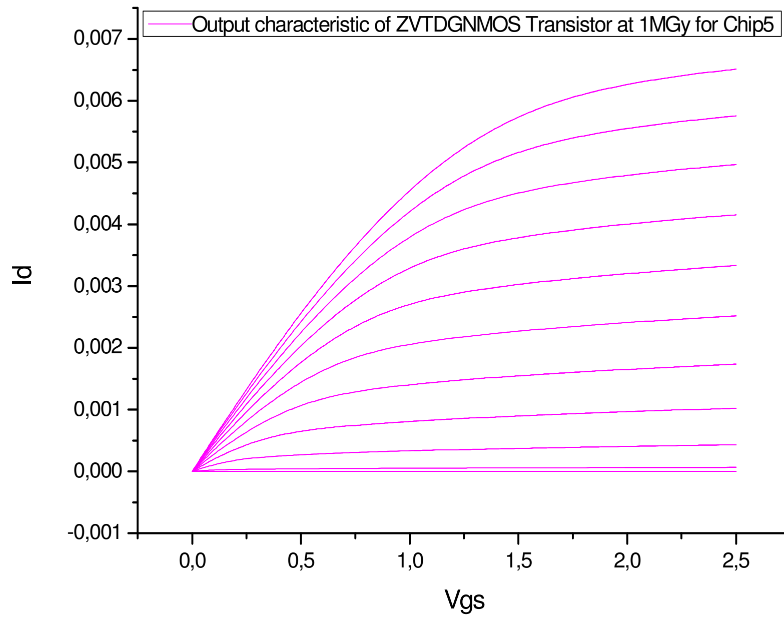


Fig.3.5.1.f Characteristic of the ZVTDGNMOS used as current source in the ZVT sourcefollower for Chip5

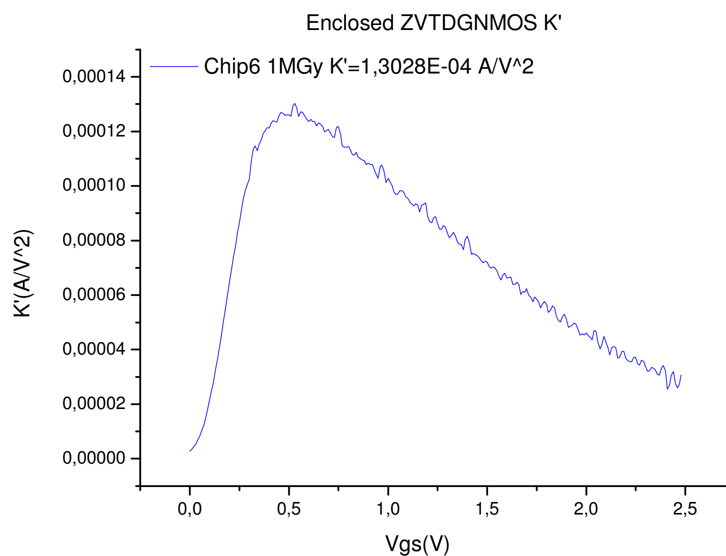


Fig.3.5.1.g Gain factor of the ZVTDGNMOS used as current source in the ZVT sourcefollower for Chip6

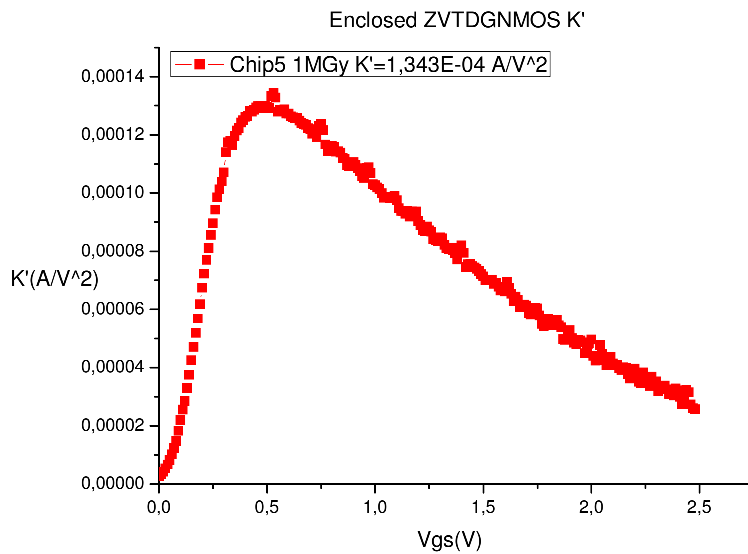


Fig.3.5.1.h Gain factor of the ZVTDGNMOS used as current source in the ZVT sourcefollower for Chip5

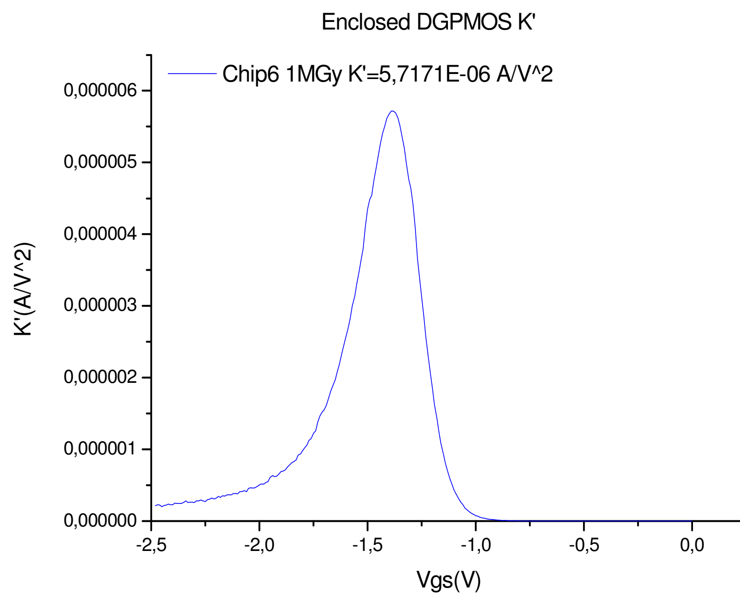


Fig.3.5.1.i Gain factor of the DGPMOS used as current source in the ZVT sourcefollower for Chip6

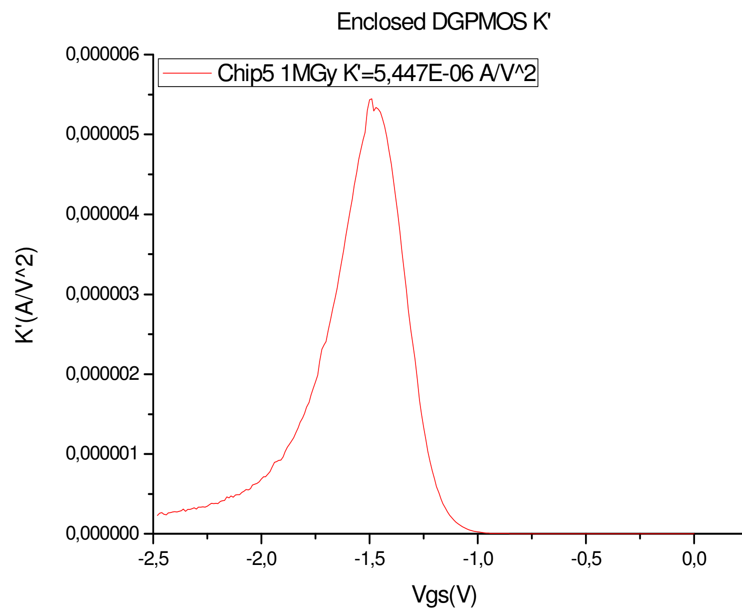


Fig.3.5.1.j Gain factor of the DGPMOS used as current source in the ZVT sourcefollower for Chip5

For 10 MGy:

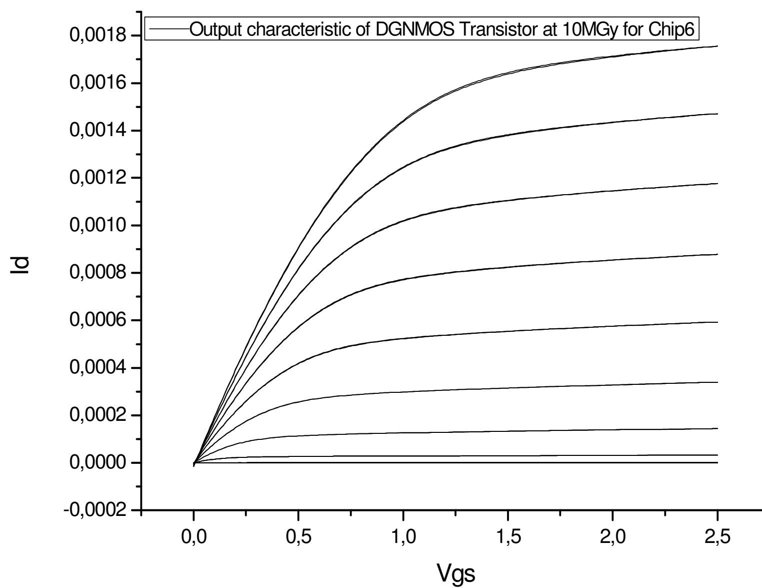


Fig.3.5.1.a Characteristic of the DGNMOS used as current source in the ZVT sourcefollower for Chip6

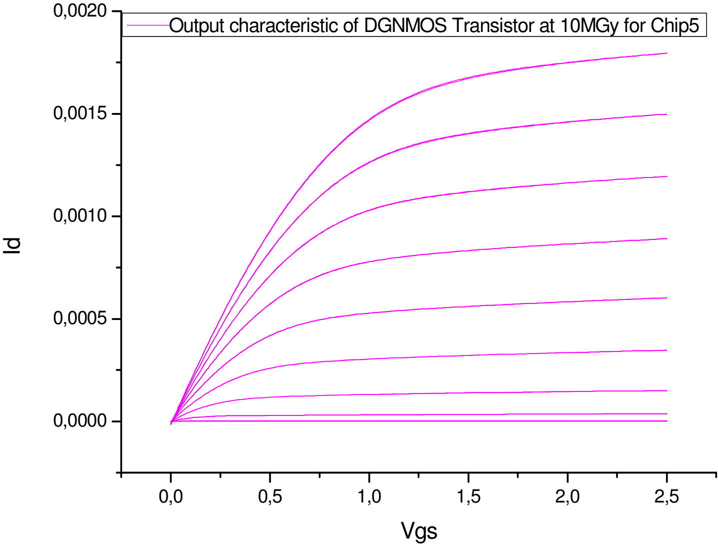


Fig.3.5.1.b Characteristic of the DGNMOS used as current source in the ZVT sourcefollower for Chip5

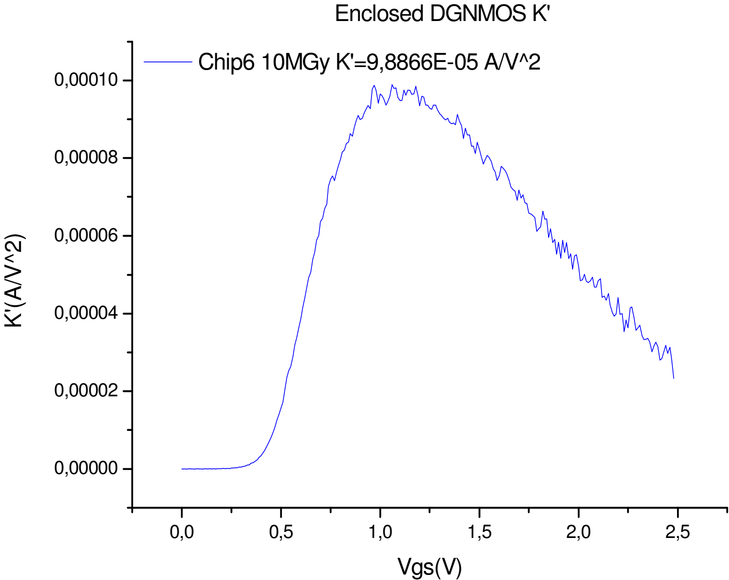


Fig.3.5.1.c Gain factor of the DGNMOS used as current source in the ZVT sourcefollower for Chip6

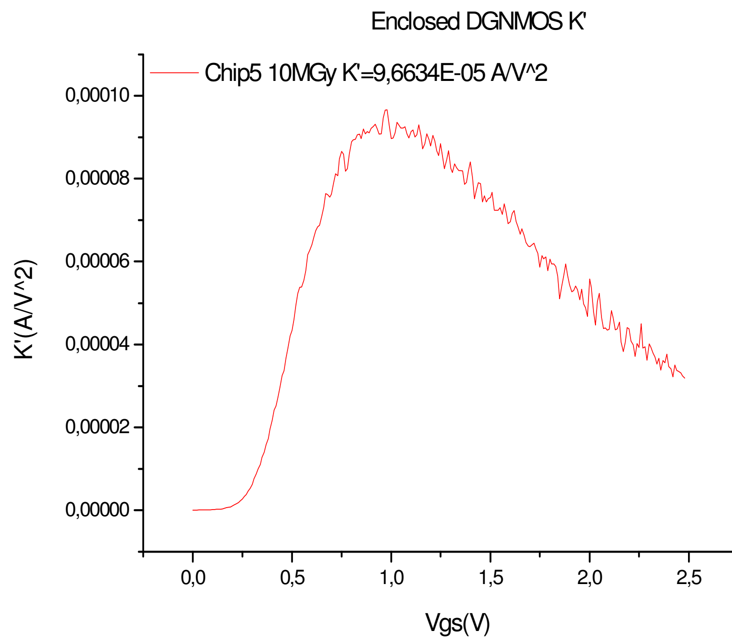


Fig.3.5.1.d Gain factor of the DGNMOS used as current source in the ZVT sourcefollower for Chip5

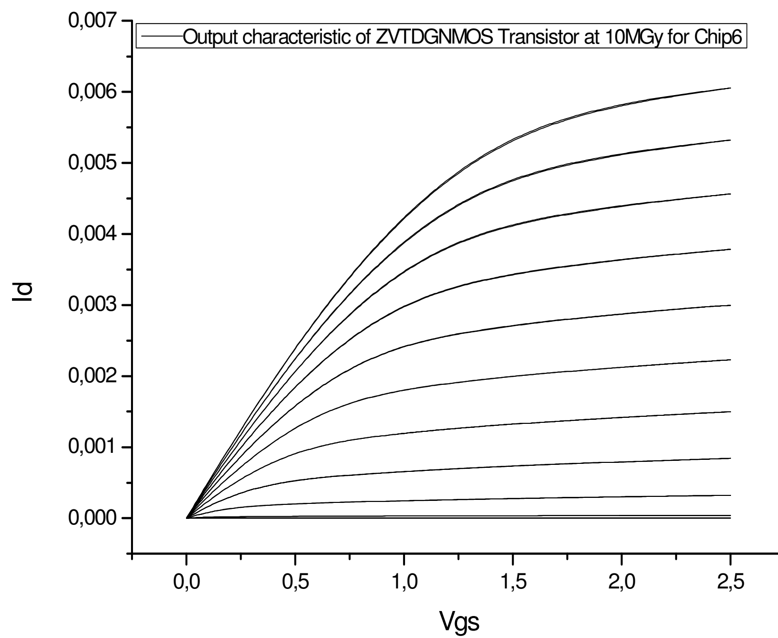


Fig.3.5.1.e Characteristic of the ZVTDGNMOS used as current source in the ZVT sourcefollower for Chip6

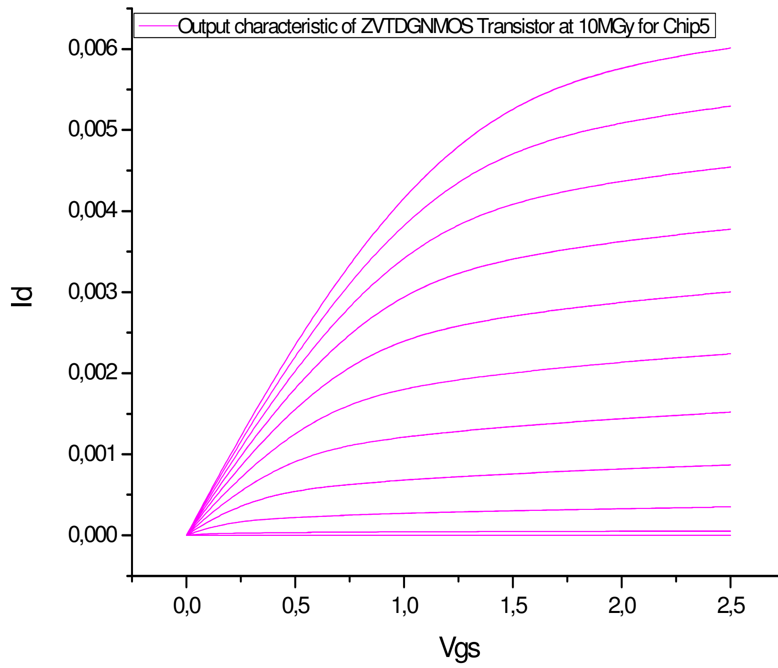


Fig.3.5.1.f Characteristic of the ZVTDGNMOS used as current source in the ZVT sourcefollower for Chip5

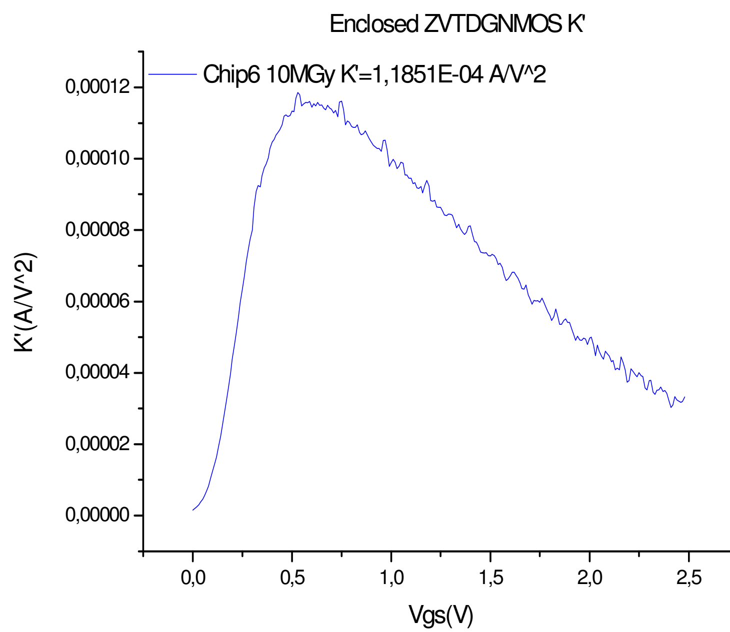


Fig.3.5.1.g Gain factor of the ZVTDGNMOS used as current source in the ZVT sourcefollower for Chip6

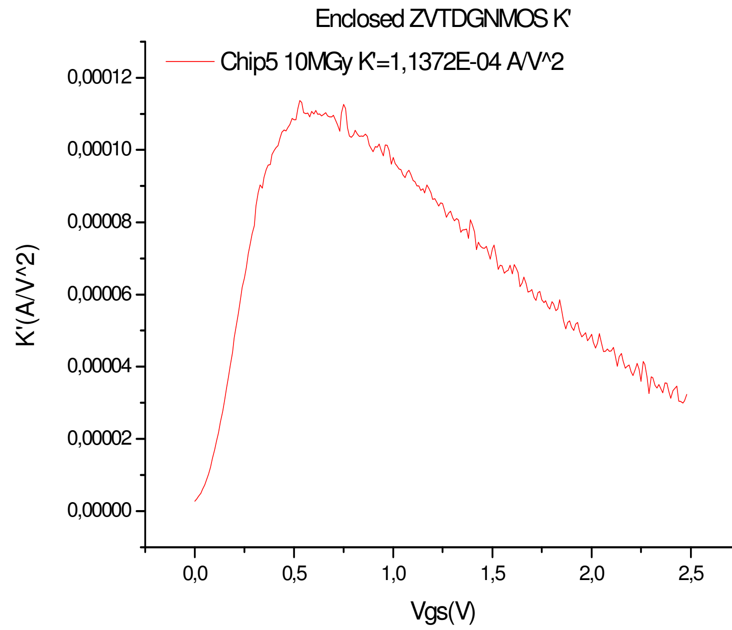


Fig.3.5.1.h Gain factor of the ZVTDGNMOS used as current source in the ZVT sourcefollower for Chip5

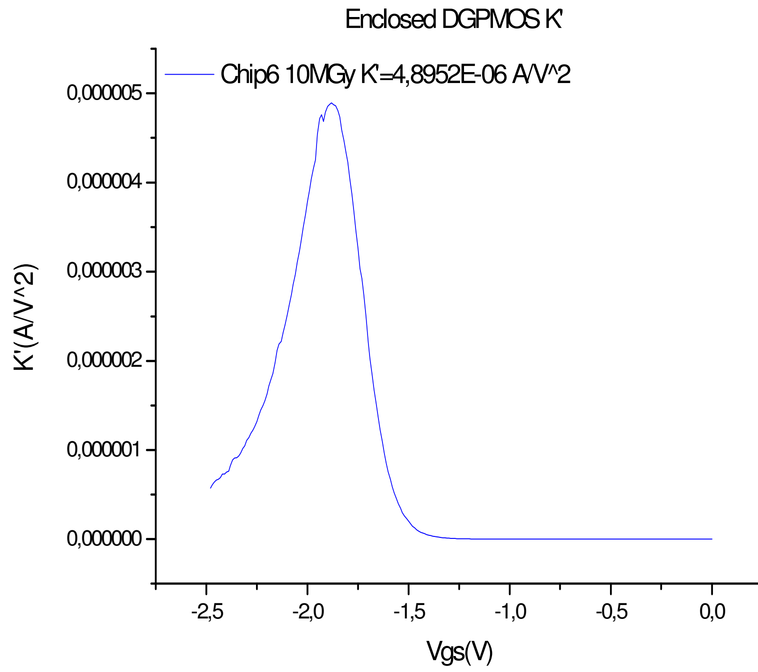


Fig.3.5.1.i Gain factor of the DGPMOS used as current source in the ZVT sourcefollower for Chip6

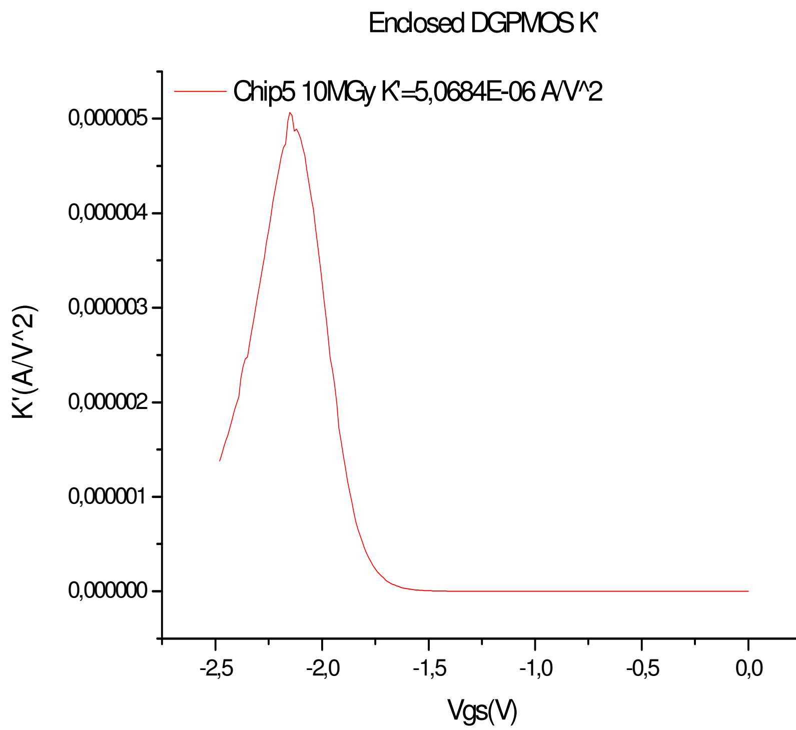


Fig.3.5.1.j Gain factor of the DGPMOS used as current source in the ZVT sourcefollower for Chip5

CHIP5	K'(A/V ^{2}) for 0 Gy	K'(A/V ^{2}) for1 MGy	K'(A/V ^{2}) for 10MGy
DGPFET	7,6089E-06	5,447E-06	5,6684E-06
DGNFET	1,4344E-04	1,128E-04	9,6634E-05
ZVTDGNFET	1,8033E-04	1,343E-04	1,1372E-04

CHIP6	K'(A/V ^{2}) for 0 Gy	K'(A/V ^{2}) for1 MGy	K'(A/V ^{2}) for 10MGy
DGPFET	7,6281E-06	5,7171E-06	4,8952E-06
DGNFET	1,5344E-04	1,0868E-04	1,1851E-04
ZVTDGNFET	1,8071E-04	1,3028E-04	9,6634E-05

Table3.5.1 Results for K'(Gain factor) from all figures

Error between chip#5 and chip#6 is nearly %9 .

<u>Part2</u> Threshold Voltage:
A linear regression is performed around this operating point;

$$\sqrt{I_{DS}} = \sqrt{K'/2*W_{eff}/L_{eff}}\ .(V_{GS} - V_{TO})$$

The voltage sweep is positive for n-channel devices and negative for p-channel devices.Then the intercept point with the X-axis is taken as V_{TO} .

Threshold voltages are calculated and visualised at the following figures for different doses.

<u>For 0 Gy:</u>

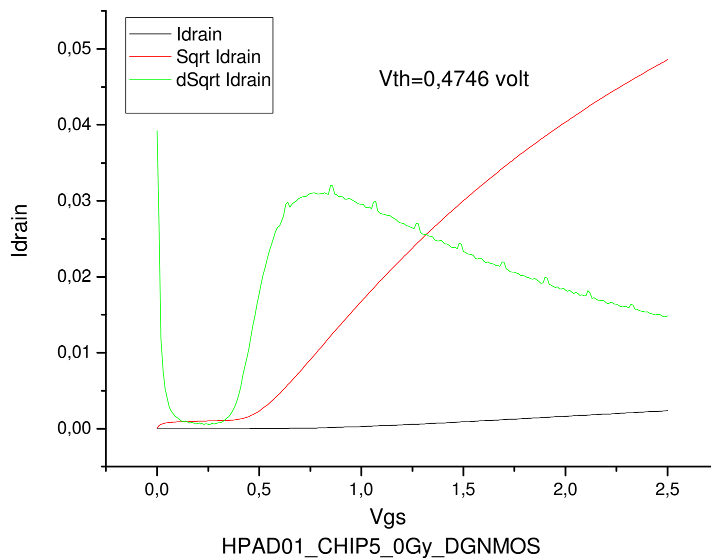


Figure.1 Drain current of DGNMOS at 0 Gy for Chip5

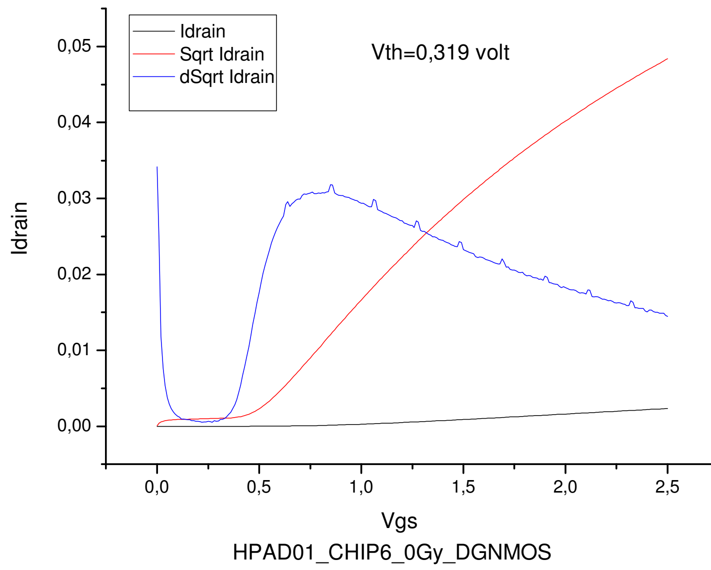


Figure.2 Drain current of DGNMOS at 0 Gy for Chip6

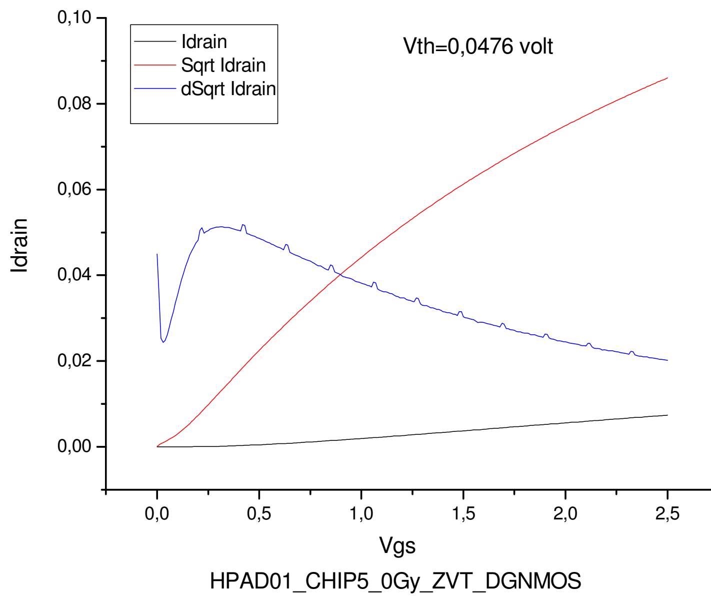


Figure.3 Drain current of ZVTDGNMOS at 0 Gy for Chip5

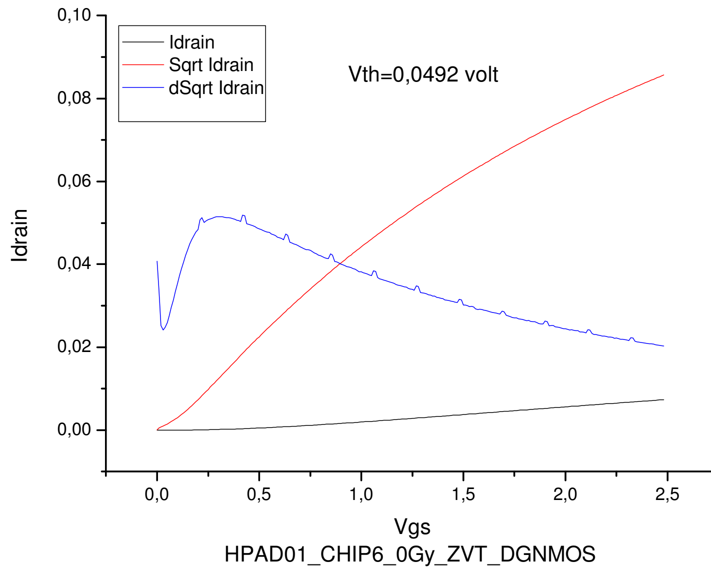


Figure.4 Drain current of ZVTDGNMOS at 0 Gy for Chip6

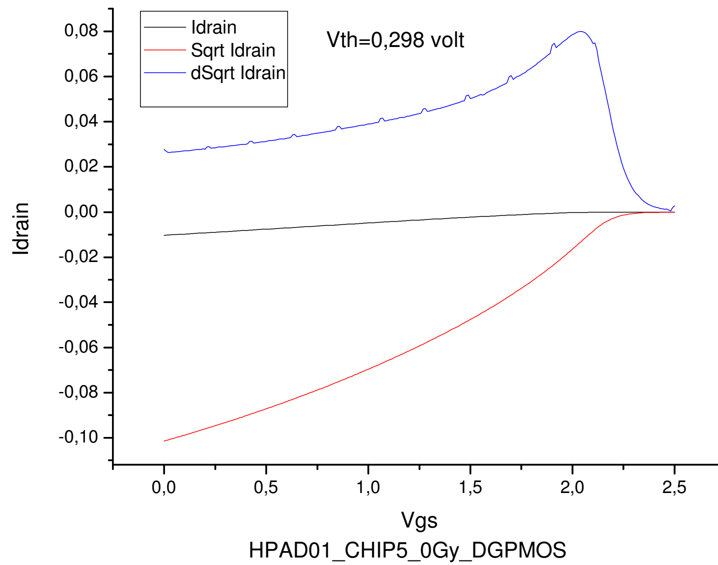


Figure.5 Drain current of DGPMOS at 0 Gy for Chip5

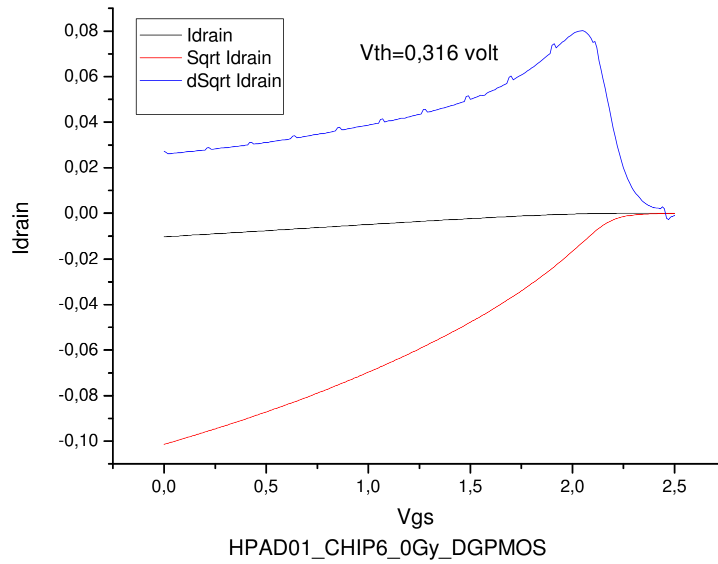


Figure.6 Drain current of DGPMOS at 0 Gy for Chip6

For 1MGy:

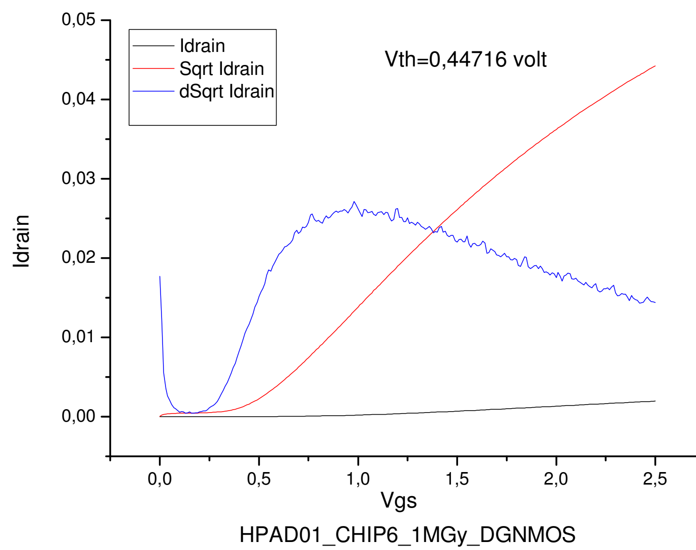


Figure.1 Drain current of DGNMOS at 1 MGy for Chip6

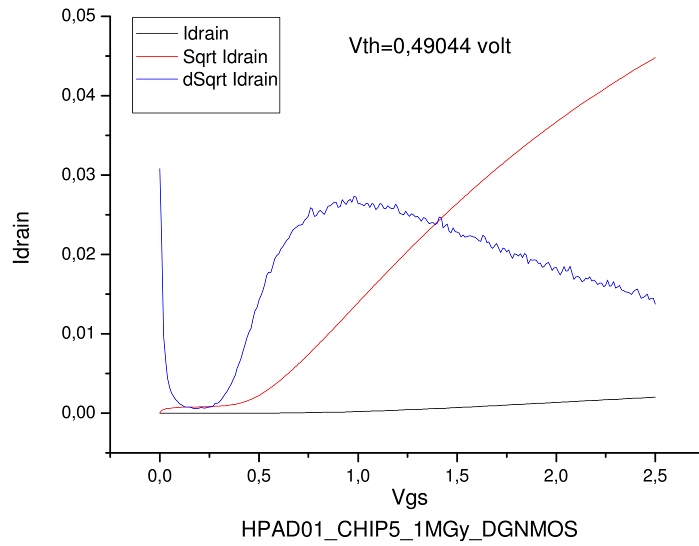


Figure.2 Drain current of DGNMOS at 1 MGy for Chip5

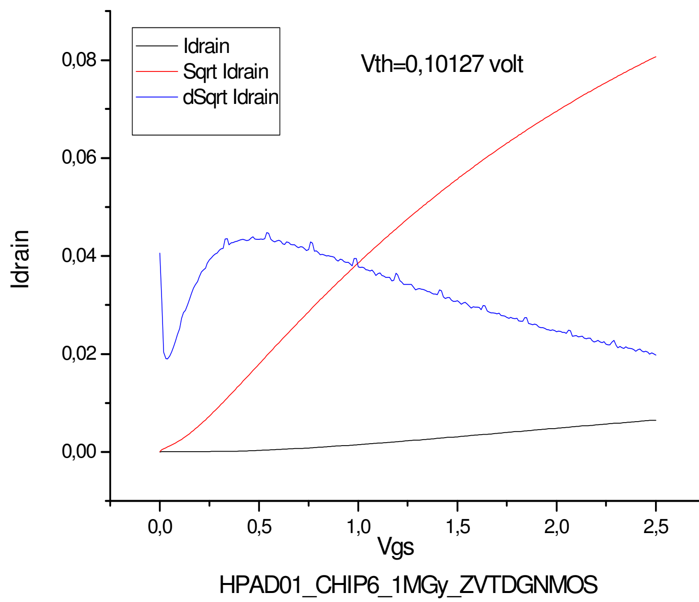


Figure.3 Drain current of ZVTDGNMOS at 1 MGy for Chip6

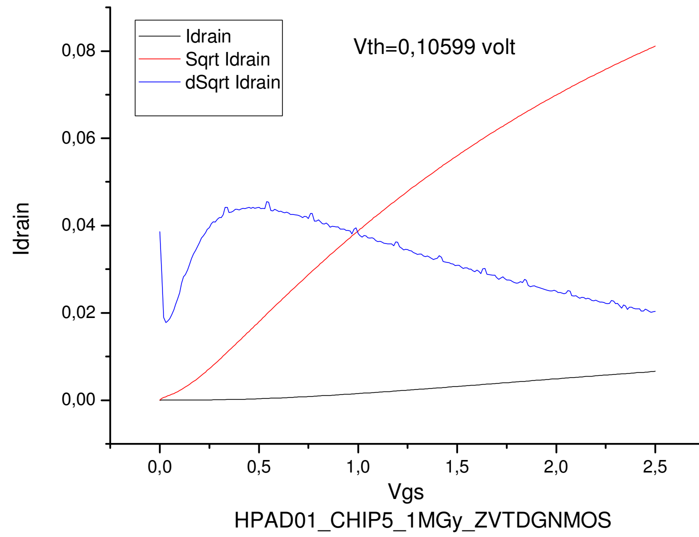


Figure.4 Drain current of ZVTDGNMOS at 1 MGy for Chip5

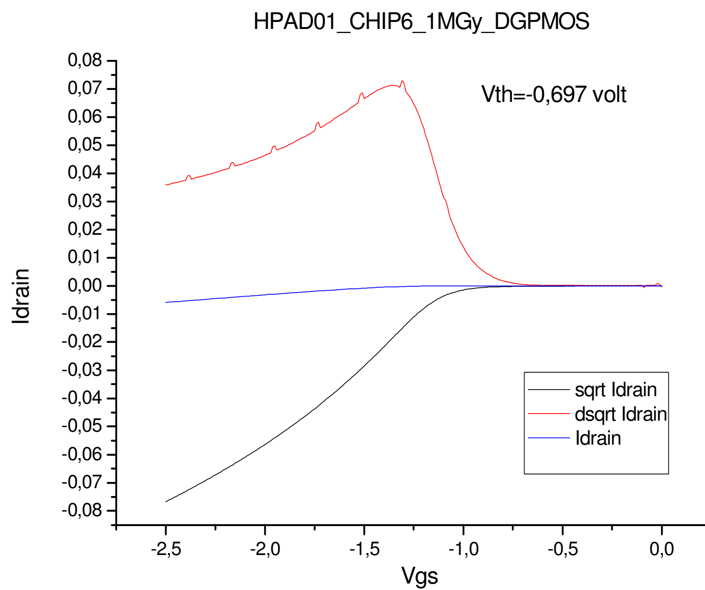


Figure.5 Drain current of DGPMOS at 1 MGy for Chip6

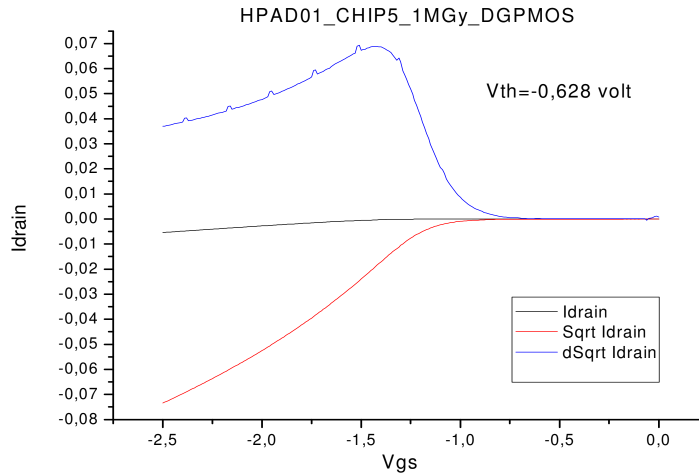


Figure.6 Drain current of DGPMOS at 1 MGy for Chip5

CHIP6	**V** $_{TO}$ (volt) for 0 Gy	**V** $_{TO}$ (volt) for 1MGy	**V** $_{TO}$ (volt) for 10 MGy
DGPMOS	-0,316	-0,6975	-1,226
DGNMOS	0,319	0,44716	0,4887
DGZVTNMOS	0,0492	0,10127	0,0942

CHIP5	**V** $_{TO}$ (volt) for 0 Gy	**V** $_{TO}$ (1volt) for 1MGy	**V** $_{TO}$ (volt) for 10 MGy
DGPMOS	-0,298	-0,628	-1,178
DGNMOS	0,4746	0,49044	0,4941
DGZVTNMOS	0.0476	0,10599	0,1876

Table3.5.2 Results for V_{th} from all figures

Error between chip#5 and chip#6 is nearly %6.

4-CONCLUSION

In this experimental work an readout ASIC(Application Specific Integrated Circuit),produced in the same technology as the AGIPD readout chip, is exposed to a substantial dose,since the sensor will absorb only more or less %90 of the photons.Therefore the accumulated dose in the innermost part of the detector can reach up to 100 MGy.In turn a test chips(Chip5 and Chip6) with capacitors and transistors in the choosen CMOS technology was irradiated at DORISIII beamline F4 to identify critical components.Threshold voltages and Gain factors

are evaluated and visualised to observe the radiation effects in the CMOS transistors before and after irradiation for different doses(0Gy,1MGy,10MGy).Consequently, the DGPMOS transistors are usable to about 1MGy (…10MGy).DGNMOS and ZVTNMOS transistors are usable to over 100 MGy. Experimental results compared and discussed with other results.

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