Analysis of electrical characteristics of gated diodes for the XFEL experiment

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Internal note (within AGIPD collaboration)

Abstract

Gated diodes are an important tool for the characterization of the Si-SiO_2 interface with respect to surfaced effects of Si sensors. Gated diodes were fabricated by CiS, Erfurt, Germany on high resistivity (3-4 kΩ cm) <111> oriented n-type silicon material and irradiated by 10 keV X-rays up to 1GGY at HASYLAB, DESY, Hamburg; the experimental measurements for the extraction of microscopic parameters; fixed oxide charges (N^{fix}_{ox}), interface trap density (D_{it}), capture cro-sections of D_{it} (σ_{eff}), width of gaussian σ^{rms}_{it},, and energy level E_c-E_{it} and surface current (I_{ox}) are performed. The interface states densities (D_{it} in cm^{-2} eV^{-1}) have been determined by measurements of the Thermally Dielectric Relaxation Current (TDRC) signal versus energy level (E_c-E_{it}). The aim is to use extracted parameters in Synopsys TCAD device simulation to reproduce measurement.The purpose of this paper is to analyze experimental measurements on non-irradiated and irradiated gated diode from the electrical characteristics of Al/SiO2/n-Si (MOS) capacitors. The Capacitance–Voltage (C/V_g) and Conductance–Voltage ($G/\omega/V_g$) measurement have been carried out in the frequency range of 10 kHz–800 KHz and bias voltage range of (+3 V) to (-85 V) at room temperature of 293K. It was found that both C and G/ω of the MOS capacitor was quite sensitive to frequency, and flatband voltage and oxide capacitance decreases with increasing frequency in strong accumulation whereas G increases with frequency. The change of the capacitance in the accumulation region at high frequency is resulting from the presence of high concentration of interface trap density or uncorrected series resistance (R_s) of the bulk Si and the change of the conductance is due to the change of the distribution of the charge carrier at Si-SiO_2 interface. In addition, the capacitance and conductance have been corrected at 10 kHz and 800 kHz for the effect of series resistance (R_s) to obtain the real capacitance and conductance of MOS capacitors for non-irradiated and irradiated with 5 MGy. The frequency dependent C/V_g and $G/\omega/V_g$ characteristics confirm that the N^{fix}_{ox}, D_{it}, E_c-E_{it}, σ_{it} (width of gaussian profile distribution of interface trap) and R_s of the MOS capacitors are an important parameters that strongly influence the electrical properties of MOS capacitors. There is good qualitative agreement observed in the simulation and the experiments.

Keywords: Gated diode, MOS capacitor, Si sensor, frequency, oxide charge, interface trap density.

1.0 **Introduction**.

Photon Science research at the 4th generation photon science European XFEL (X-ray Free Electron Laser) requires Si pixel sensors with unprecedented performance: Doses of up to 1 GGy 12 keV x-rays and a

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dynamic range from 1 to 10^5 12 keV photons per sub picosecond pulse and pixel of $(200\ \mu m)^2$ area. In this work, this is done within the AGIPD Collaboration [1-5], we present the analysis of electrical characteristics of gated diodes from the electrical characteristics of Al/SiO2/n-Si (MOS) capacitors for C/V_g and G/V_g characterization

A lot of study has been made on low and high resistivity MIS capacitor in order to understand C/V_g and G/V_g behavior versus frequency [6-8].

The behavior of C/V_g and G/V_g characterstics of gated diode can be understood by MOS capacitor (heart of the gate diode). The structure can yield considerable information regarding the properties of the dielectric used, the underlying silicon and the silicon/oxide (Si/SiO_2) interface. In order to extract these properties several capacitance-voltage (C/V_g) measurement techniques have been developed. These include (i) High Frequency (HF) C/V_g measurement (ii) Low Frequency (LF) or Quasi-static C/V_g measurement (iii) Pulsed C/V_g measurement and (iv) Capacitance-time (C/-t) measurement [9-20].

This work extends for the development of radiation hard pixel sensor for the Adaptive Gain Integrating Pixel Detectors (AGIPD) of the XFEL experiment.

This paper is organized as follows: introduction is given in section 1 and section 2 described the design of gated diode and method. In sub-section 2, we described the basic theory of oxide charges and interface trap density. Experimental measurement results and conclusion will be described in the section 3. Comparision of experimental data with Synopsys TCAD device simulation are shown in section 4.

2. Design of gated diode and method

Gate diode test field structures of 0.404 mm^2 x 300 μm^2 are used for the extraction of microscopic parameters. The C/V_g measurement is carried out by applying a dc voltage and a small ac signal to the gate contact (2 and 3 gate rings are connected) which drives the device from accumulation, depletion and into inversion [1-2] and the current-voltage (I/V_g) measurement is done by applying constant reverse bias on diode (p^+) ands varying gate voltage with respect to n^+ contact and it is shown in the schematic of the gated diode in Fig.1a. A C/V_g curve is considered high frequency if the probing frequency is 10 kHz. A typical HF C/V_g curve drive from accumulation, depletion and inversion is shown in Fig 1.1.

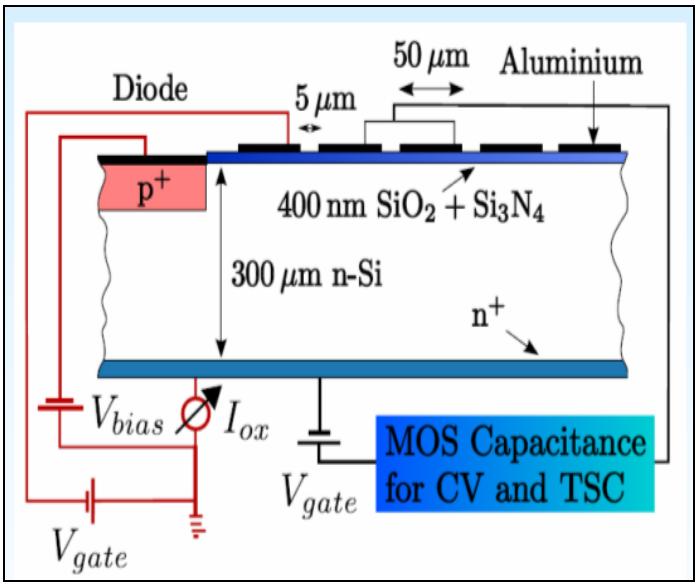


Figure 1a: Schematic of the gated diode (five gate rings) structure. Circuit for I/V_g and C/V_g measurements are shown in the left and right part of the structure (here the results are shown for the measurement performed immediately after irradiation).

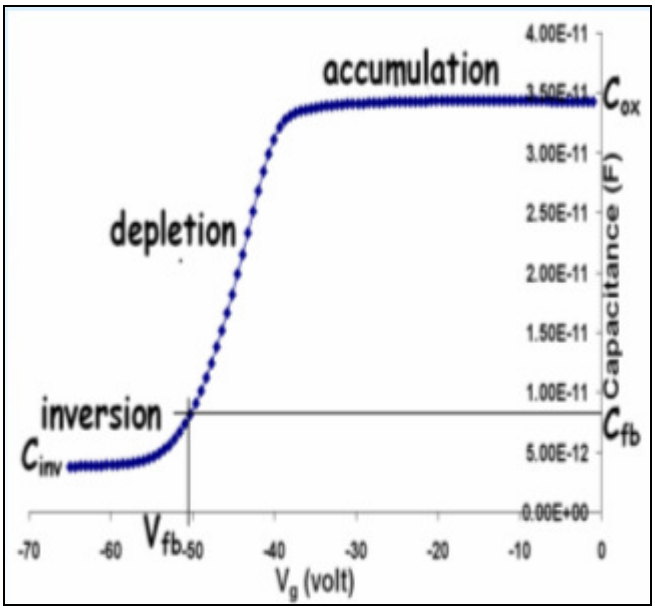


Figure 1 b: Typical Capacitance-Voltage (C/V_g) curve. In Fig 1.1, C_{ox}- oxide capacitance [F], C_{inv}- HF inversion capacitance, V_{fb} – flat band voltage and C_{fb}- flatband capacitance.

2.1 The Ideal MOS structure

In the real MOS structure (no charges in oxide and no interface trap density), the C/V_g curve of a typical MOS capacitor will exhibit a shift due to the work function difference (ϕ_{MS}). This is a difference of metal work function (Φ_M) and semiconductor work function (Φ_S)
In Ideal case,

$$V_{fb} = \phi_{MS} = \phi_M - \phi_S \qquad [1]$$

In addition to the work function difference, the charges in the insulator and at the Si/SiO_2 interface also contributed to the distortion of an ideal C/V_g curve. The presence of these charges is unavoidable in an ideal or real MOS structure. In typical MOS structures the charges are located in various parts of the insulator and the Si/SiO_2 interface as shown in Fig 1c.

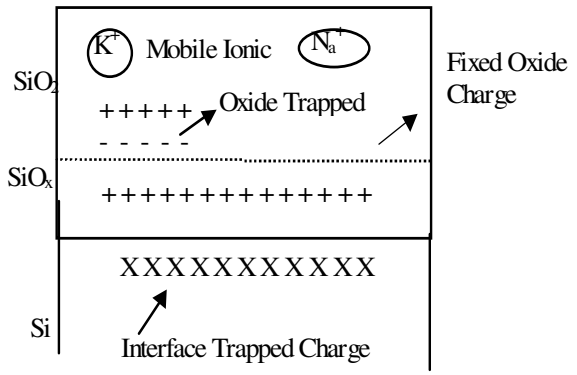


Figure 1c : Charges and their location for thermally oxidized silicon.

Thus, the C/V_g curve will shift further by V_{fb} (due to N^{fix}_{ox}, interface trap density (N_{it} in cm^{-2}) and Φ_{MS}). V_{fb} is given by

$$V_{fb} = \phi_{MS} - \frac{N_{ox}^{\ eff} qA}{C_{ox}} \qquad [2]$$

where $N_{ox}^{\ eff} = N_{ox}^{\ fix} + N_{it}$ = effective interface charge (cm^{-2}).

V_{fb} = flatband shift due to N^{eff}_{ox} alone.

C_{ox} = Capacitance of the oxide layer (F).

A- Gate area for gated diode.

2. 2 Classification of the insulator and the Si/SiO_2 interface charges

In this section, the basic classification of the insulator and the Si/SiO_2 interface charge that will distort the ideal C/V_g curve will be discussed. There are four general types of charges associated with the the Si/SiO_2 system [12]. They are interface trap charge, fixed oxide charge, oxide trap charge, mobile oxide charge.

The **interface trap charge N_{it}** is the charge, which is due to (1) structural, oxidation-induced defects, (2) metal impurities, or (3) incomplete dangling bonds and absorption of foreign material at the silicon surface. The interface trap charge can be positive or negative charges and located at the Si/SiO_2 interface. Theory has been predicted that each incomplete silicon bond will create an interface trap. The density of the interface trap charge can be reduced when the surface is thermally oxidised.

This is attributed to the bonding of the SiO_2 to the silicon surface atoms. This property of the silicon-dioxide system is unique and is one of the major reasons for using thermally grown SiO_2 for insulating purposes.
Typical values for N_{it} lie in the range of $5x10^9$ to 10^{11} cm^{-2}, depending on the orientation of the silicon crystal and on the process history in non-irradiated device and after irradiation, it will increase up to few $10^{12} - 10^{13}$ cm^{-2}. The lowest interface trap density is found on <100> oriented crystal. The interface trap can be positively charged or negatively charged depending whether the trap is acceptor or donor type. An acceptor-type trap becomes negatively charged when it gains an extra electron and becomes neutral when it loses the extra electron. A donor-type trap becomes positively charged when it losses an electron and neutral when it regains the lost electron. It has been found that donor lie in the lower part of band gap and acceptor in the upper part of the band gap of Si.

This increases the slope of the C/V_g curve. Under small signal low frequency, it will respond and it will oscillate about the mean position of the Fermi level and this is capable of increases (High Resistivity Silicon -HRS) and decreases (Low Resistivity Silicon-LRS) interface state density and this will also shift the C/V_g curve with frequency and it depends upon the interface state density.

The **fixed oxide charge** $\mathbf{N^{fix}_{ox}}$ is a positive charge, due primarily to structural defects in the oxide layer less that 25Å from the Si/SiO_2 interface. This charge is immobile under an electric field. However, it is affected by temperature above 500°C and by the ambient atmosphere. Typical values for $\mathbf{N^{fix}_{ox}}$ in non-irradiated device are in the order of 10^{10}-10^{11} charges per cm^{-2}, depending on process conditions and after irradiation, this will increase up to few 10^{12} cm^{-2}. $\mathbf{N^{fix}_{ox}}$ is not affected by the thickness of the oxide. However, it increases when the structure is exposed to high energy radiation.
The density of the fixed oxide charge can be reduced and may be saturate up to some value by high temperature annealing. This fixed oxide charge gives flat band shift and also increases the slope of the C/V_g curve from the ideal MOS C/V_g curve.

The **oxide trap charge** $\mathbf{N_{ot}}$ is due to imperfections throughout the bulk of the oxide layer. It can be positive or negative depending whether holes or electrons are trapped in the bulk of the oxide. Trapping may result from ionising radiation, avalanche injection, or other similar processes and the threshold voltage can be shifted in either direction.

Under ionizing radiation effect, hole traps are positively charges and thus it can be model as fixed positive oxide charges at the SiO_2/Si interface.

The **mobile oxide charge** $\mathbf{N_m}$ is the most significant charge component in the insulator. It is due to ionised impurities such as sodium (N_a^+) and, to a less extent, potassium (K^+) and lithium (Li^+). The alkali ions, and in particular sodium, are troublesome and difficult to control. Sodium is a widely distributed impurity in many metal and laboratory and is easily transmitted by human contact. It can migrate in silicon dioxide even at room temperature. Negative ions such as Cl^-, F^- may also be present in the insulator but are not believed to be mobile at temperatures below roughly 500°C.

The mobile oxide charge gives hysterics effect [2] .

The effect of these various charges associated with the SiO_2/Si system can be determined by using different C/V_g measurement. For instance, HF C/V_g measurement is used to determine the effective interface charge N_{ox}^{eff}, by assuming all the insulator charge located at the silicon surface. The effective interface charge will cause the similar shift in the CV curve as that of the actual insulator charge of unknown distribution. Whereas the Quasi-static CV method can be also used to determine the distribution of the interface trapped charge throughout the band gap.

2.3 Theoretical calculation

In this section, we described the most commonly used equations for the understanding and calculation of parameters for MOS capacitors for C/V_g characterization. Under HF signal (f ~ 1 MHz), interface trap will give no respond to the small signal ac excitation and thus,
high frequency capacitance can be calculated by following expression;

$$C_{HF,inv} = \frac{C_{ox} C_D}{C_{ox} + C_D} \qquad [3]$$

where C_D is depletion layer capacitance.

$$C_{HF,inv} = \frac{1}{\frac{1}{C_{ox}} + \frac{x_{d,T}}{\varepsilon_S}} \qquad [4]$$

where $x_{d,T}$ [1] is the maximum depletion width in MOS capacitor (electric field at $x_{d,T}$ =0). With the comparison of above equation, C_D can be determined.

The interface generation current (I_{ox}) is caused by the surface generation/recombination of free charge carrier with interface trap,

$$I_{ox} = q_0 n_i S_0 A \quad [5]$$

where q_0 is elementary charge, n_i is intrinsic carrier concentration.
Assuming a homogeneous distribution of interface states across the band gap, S_o is given as

$$S_0 = \sigma_{eff} v_{th} \pi K_B T D_{it\ midgap} \quad [6]$$

where σ_{eff} is the effective capture cross-section of charge carrier, v_{th} is the thermal velocity of charge carrier, k_B is Boltzmann constant, T is temperature and D_{it} is interface trap density at mid gap of Si (cm^{-2} eV^{-1}).
Assuming homogeneous distribution of interface trap in the band gap of Si, D_{it} can be replaced by Nit and $\Delta E \approx E_g$ or $E_g/2$ (depends upon the range of energy levels where the interface traps (donor/acceptor or both) are active.)

$$N_{it} = D_{it} \Delta E \quad [7]$$

The capacitance (C) and conductance (G/ω) curve for non-irradiated and irradiated gate diode can be corrected for series resistance and other interfacial effects from [9].
The corrected capacitance (C_c) and conductance (G_c) is made by following expression;

$$a = G_m - (G^2_m + \omega^2 C^2_m) R_S$$

$$R_S = \frac{G_{ma}}{G^2_{ma} + \omega^2 C^2_{ma}}$$

$$C_c = \frac{(G^2_m + \omega^2 C^2_m) C_m}{a^2 + \omega^2 C^2_m} \quad [8]$$

$$G_c = \frac{(G^2_m + \omega^2 C^2_m) a}{a^2 + \omega^2 C^2_m}$$

where C_m, G_m, ω and R_s is the measured capacitance, conductance, frequency and series resistance.

2.3.1 Two Gaussian distribution of interface trap model for surface damage effect in Si sensors

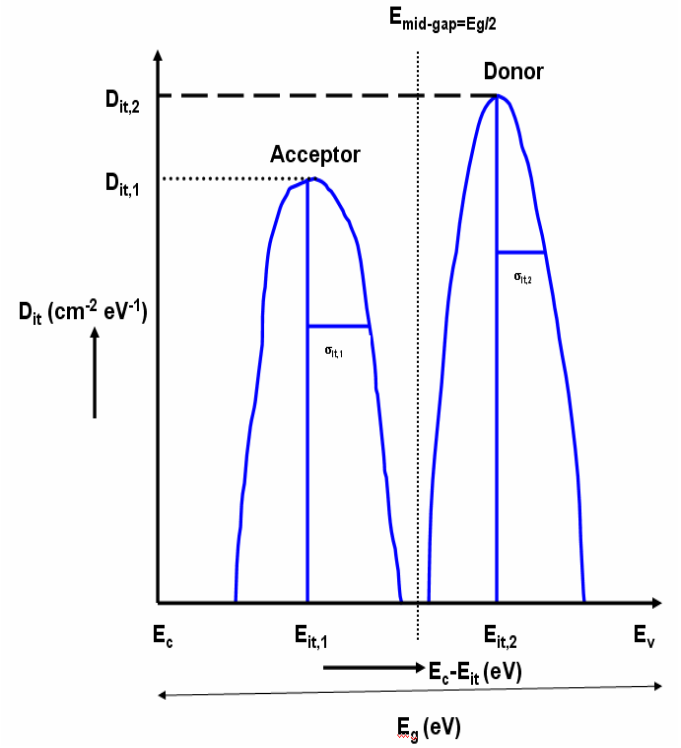


Figure.2: Two Gaussian distribution of interface trap model for TCAD simulation of surface damage effect in Si sensors.

From the TDRC measurements, we got the information about the interface trap verus energy level and its parameters like D_{it}, E_c-E_{it}, σ_{it} (width of gaussian profile distribution of interface trap). Fig.2 describes the two Gaussian distribution of interface trap model for TCAD simulation.
For this, the required distribution of density of states (DOS) for two gaussian distribution of interface trap in the band gap of Si is given by ,

$$DOS = [D_{it,1} e^{-0.5\left(\frac{E - E_{it,1}}{\sigma_{it,1}}\right)^2} + D_{it,2} e^{-0.5\left(\frac{E - E_{it,2}}{\sigma_{it,2}}\right)^2}] \quad [9]$$

this will be implemented into Synopsys TCAD device simulator to reproduce the measurements and simulation of radiation damage effects by 12 keV x-rays .

3. Results and conclusion

A lot of progress has already been made in order to understand the radiation hardness of silicon sensors for XFEL environment and the important observation has been found that after a few MGy of irradiations, saturation of charge occurs [4].

It is interesting to see the behaviours of capacitance and conductance versus frequency up to 5 MGy irradiation doses [4].

Here, we present our new result and views about the capacitance and conductance before and after irradiation.

3.1 Non-irradiated result: C/V_g as function of frequency

In non-irradiated gated diode, we have found that the decrease of oxide related capacitance (C_{ox}) with increase of frequency in Fig.3a. This is due to uncorrected series resistance of the bulk (R_{SB} for high frequency model [21]). We have performed the correction in capacitance using equation 7 only at 10 kHz and 800 kHz, it has been found that after correction, there is no change in C_{ox} and no shift in the C/V_g (co change in flat nad voltage) curve with increasing frequency. This is due to low interface trap concentration.

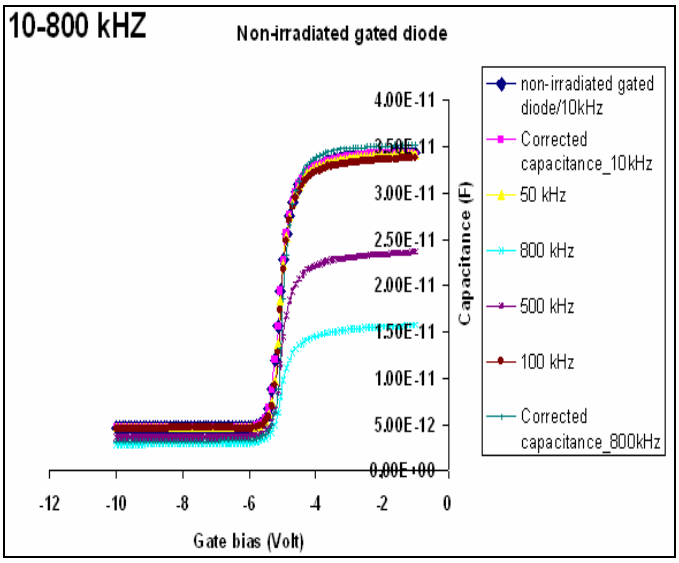
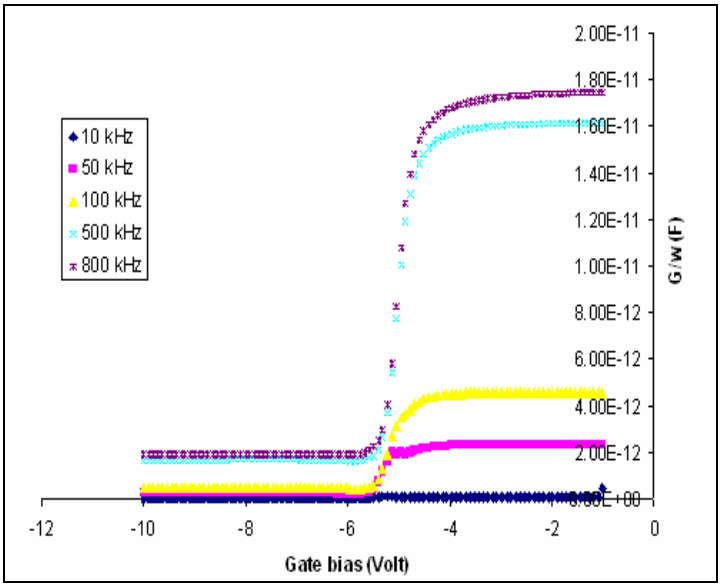


Figure 3a: C/V_g as function of frequency for non-irradiated gated diode.

3.2 Non-irradiated result: G/V_g as function of frequency

G/V_g as a function of frequency is shown in Fig.3b. It is observed that G increases with frequency. This shows that there is no peak in the G/V_g curve at high frequency so we have to correct the series resistance in the accumulation region of MOS using equation 8 and 9.



a

Figure 3b: G/V_g as function of frequency for non-irradiated gated diode.

Fig.4a and Fig.4b show the corrected conductance at 10 and 800 kHz. There is peak observed at certain bias and it is increases with frequency. The peak of the G/V_g curve depends upon the distribution of the charge carrier at the Si-SiO_2 interface and it is seen that peak is at around flat band voltage. This also confirms from simulation [Sri].

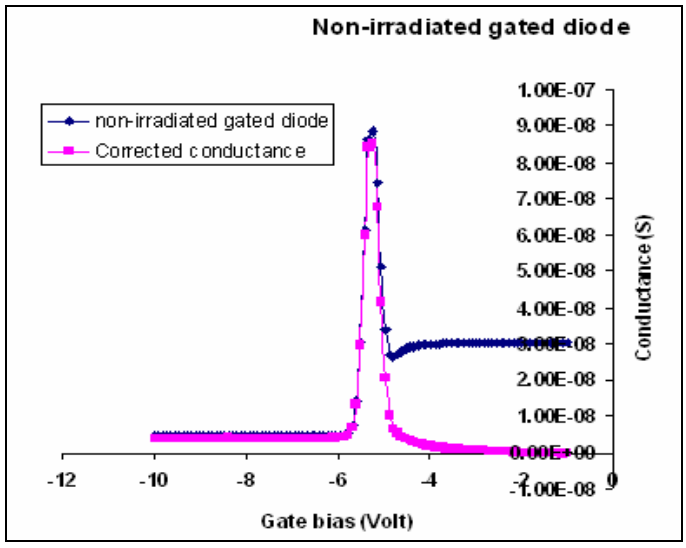


Figure 4a: Corrected conductance as function of gate bias at for non-irradiated gated diode at 10 kHz.

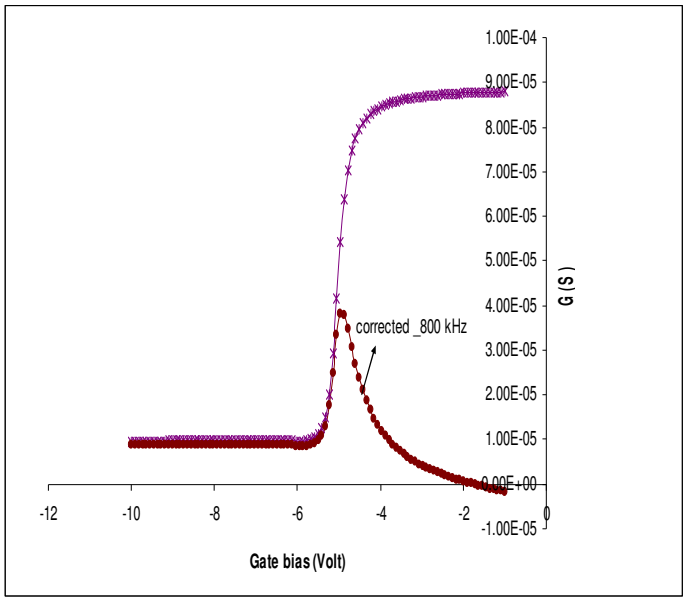


Figure 4b: Corrected conductance as function of gate bias at for non-irradiated gated diode at 800 kHz.

3.3 Irradiated result: C/V_g , G/V_g as function of frequency

In our previous results [3], we have shown the shift of the C/V_g curve with frequency for an irradiated gate diode [4]. It is interesting to see in Fig. 5, there is a peak of the C/V_g curve at around flatband voltage at 10 kHz with irradiation doses from 0.5 MGy to 10 MGy. , this is due to increase of the charge distribution at Si-SiO_2 interface. But for 10 MGy, there is decrease of the peak and flat band voltage and this is because of the decreases of the charge distribution after 5 MGy. [4]

In Fig. 6a, we have shown the $G/\omega/V_g$ curve for 5 MGY for different frequency. Similar behaviours are achieved as per Fig.2, G/ω increases with frequency.

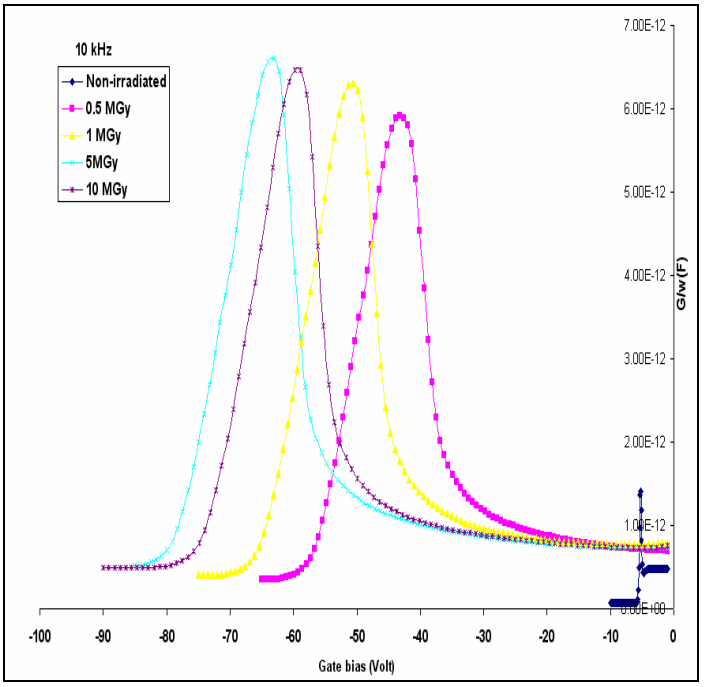


Figure 5: conductance (G/ω) as function of gate bias at for different irradiated gated diode at 10 kHz.

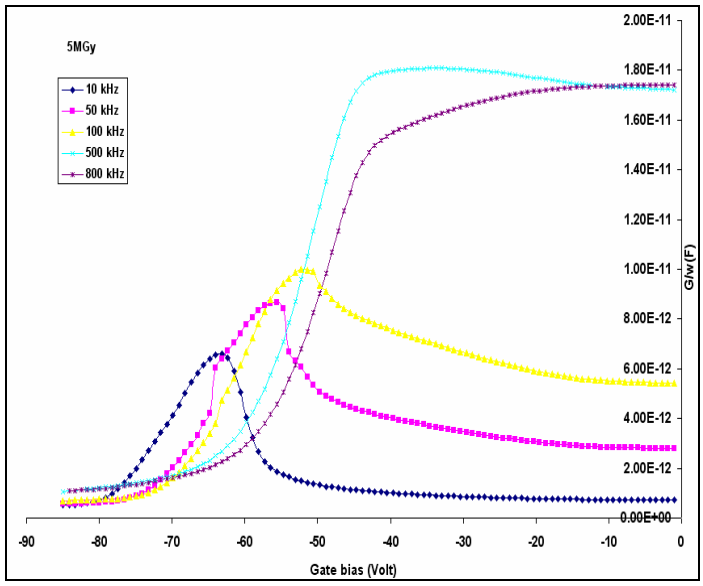


Figure 6a: Conductance (G/ω) at different frequency as a function of gate bias for 5 MGy irradiated gated diode.

and there is shift in the peak of the conductance curve observed towards lower gate voltage with increasing frequency. The conductance peak is visible at lower frequency but at higher frequency like at 800 kHz, it is not clear. Therefore, we corrected the conductance (shown in fig.6b) for 10 and 800 kHz, it can be seen the the peak is clear for both frequency and shift of the peak towards lower gate voltage.

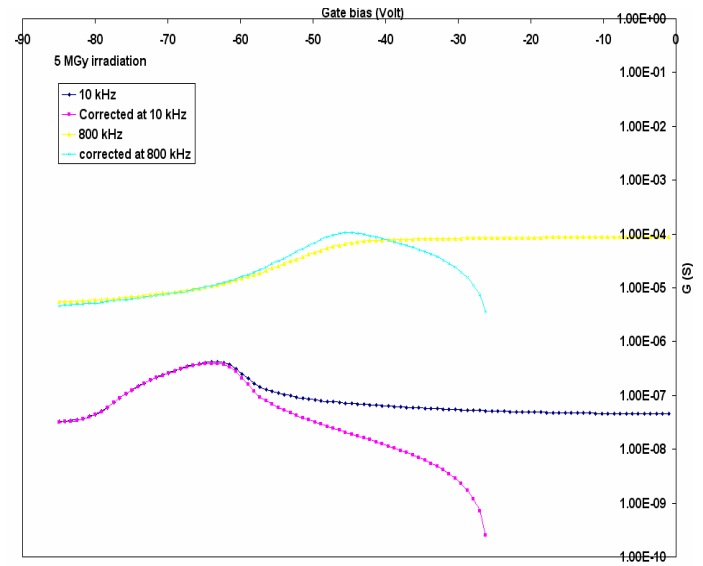


Figure 6b: Conductance (G) at 10 and 800 kHz frequency as a function of gate bias for 5 MGy irradiated gated diode.

In Fig.7, we have only corrected the capacitance of 5 MGy irradiated gate diode at 10 kHz and 800 kHz and two important things is observed from the real corrected capacitance.

There is no change in uncorrected and corrected capacitance is observed for low frequency of 10 kHz. Thus, this can be optimum frequency for the gated diode measurement whereas at high frequency of 800 kHz, there is change in uncorrected and corrected capacitance at 800 kHz. It can be seen that in Fig.7 , a peak in the accumulation region observed, may be this is due to the mechanism that charge transfer through the Si-SiO_2 interface or we can correct the capacitance from model [21].

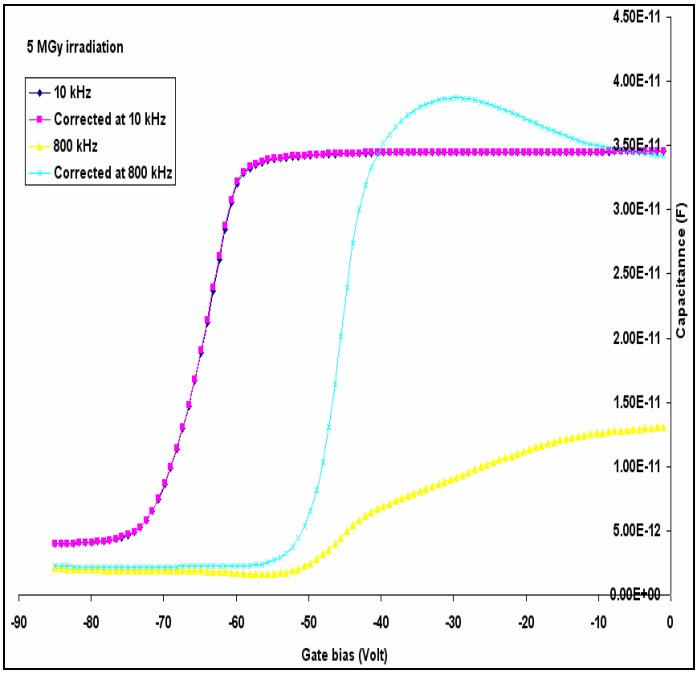


Figure 7: Corrected capacitance at 10 and 800 kHz as function of gate bias for 5 MGy irradiated gated diode.

4. Comparision of simulation and experiment

There is good agreement observed between simulation and experiment for non-irradiated MOS test structure and already shown detailed results in [Sri] and also reported first set of results on comparison with 0.5 MGy irradiated MOS test structure as function of frequency [21]. Now, we have new set of experimentally measured

microscopic parameters which is based on two Gaussian distribution of interface trap model for surface damage effect in Si sensors for the comparison of test structures results and simulation and prediction of the Si sensors in the XFEL environment and this is underway.
This experience is used in the design of radiation tolerant segmented detectors p^+n or n^+n (first design idea though simulation [22]) for AGIPD. The optimized design of first prototype pixel p^+n silicon pixel sensor for AGIPD is underway.

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