Simulation of MOS Capacitor for C/V_g Characterization

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Internal note (within AGIPD collaboration)

Abstract

For the European XFEL a silicon pixel detector with a high dynamic range (10^5 12 keV photons per pixel per pulse) and a radiation tolerance up to 1GGy ($\approx 10^{16}$ 12 keV photons/cm^2) will be built. In the absence of bulk damage (threshold energy $\gtrsim$ 300 keV), the study of surface damage in silicon pixel detectors due to x-ray irradiation is very important for the long term performance of these devices. The gated diode test-structures fabricated by CiS (Institut für Milcrosensorik GmbH, Erfurt, Germany) are used for surface damage analysis and the current-voltage (I/V_g) and capacitance-voltage (C/V_g) characteristics as function of gate bias and frequency have been measured for different doses. The aim is to determine the relevant surface damage parameters (oxide charge density N_{ox} and interface trap density D_{it} at Si-SiO_2 interface) for detailed comparison of experimental data and simulations of MOS test structures and the microscopic parameters will be also implemented in TCAD for the simulation of radiation hard silicon pixel detector development for AGIPD (Adaptive Gain Integrating Pixel Detector). The C/V_g technique is broadly used to study the surface charge effects (N_{ox}) and the interface trap behaviour on the slope of the C/V_g. In the present work, very preliminary simulation results and observations on the MOS-test structures are presented using ISE T-CAD DESSIS 2-D device simulator. The simulation results are found in good agreement with the experimental data.

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Keywords: Gated diode, MOS capacitor, Si sensor, Surface damage, Capacitance, Conductance, Simulation.

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1. Introduction

European X-Ray Free-Electron-Laser experiment, X-FEL at DESY, Hamburg will be expected to start in 2013 and provide fully coherent, < 100 fs long X-ray pulses. The high intensity per pulse will allow recording diffraction pattern of single macromolecules or small crystal in single shot [1]. For AGIPD (Adaptive Gain Integrating Pixel Detector) of XFEL, $n^+n^-p^+$ Si pixel sensors are proposed as first design idea [2] for higher performance in the presence of high instantaneous photon fluxes.

In the absence of bulk damage, surface damage affects the performance of Si pixel sensors and it will degrade the macroscopic performance of used Si sensors after irradiations in terms of change of depletion voltage due to delayed depletion depth (15-20 V full depletion voltage increase), increases of surface current due to increases of dominant interface trap density near to mid gap of Si (shot noise), change of interstrip capacitance due to change of fixed positive oxide charges in oxide and interface trap (change of noise), and change of interstrip resistance due to change of surface current (change of spatial resolution) [2-3]. Therefore, systematic investigations of surface damage on sensors are very crucial for long term performance of XFEL experiment.

Physicists have already reported the effect of surface damage on current-gate voltage (I/V_g) and CMOS capacitance-gate voltage (C/V_g) characteristics of gate controlled diode [4-6]. Several attempts has been made to describe the donor and acceptor nature of interface trap using conductance- gate voltage (G/V_g) technique and it has been found that donors lie just below half of the band gap and acceptors are in the upper half of the band gap [7]. A lot of efforts have been made already made in order to study the effect of interface trap on C/V_g and G/V_g characterstics of MOS capacitor but detailed understanding of theses effect is not well understood [8-10]. Therefore simulation is recommended for detailed understanding of surface charge effects (oxide charge density, and interface charge trap density).

Here, we have shown the 2-D detailed simulation of MOS test structure for C/V_g analysis to see the effect of different physical and process parameters using ISE T-CAD DESSIS 2-D

device simulation. Within the framework of AGIPD collaboration [11], 2-D numerical device simulation has emerged as a practical means for approaching the design of radiation-hardened devices. In particular, device simulations can allow fast and relatively inexpensive predictions of detector performance in various radiation environments. In this work, the simulator has been rigorously calibrated against experimental data.

This paper is organized in this way, in sections 2 below, test structure design are summarized. Simulation procedures are presented in section 3. Result and discussions are covered in section 4. Conclusions are eventually drawn in section 5.

2. Test structure design

For simulation purpose, we have considered a simple two-dimensional geometry of test structure, consisting of a Metal-Oxide-Semiconductor (MOS) of gate width of 50 μm and device depth (W_N) of 50 μm is shown in Fig.1a. Fig.1b shows the rectangular grid of MOS capacitor of 50 x 50 μm^2. The gate area of 4.04 x 10^{-3} cm^2 is normalized from the design of gated diode fabricated at CiS (Institut für Milcrosensorik GmbH, Erfurt), Germany.

In MOS test structure, the doping concentration (N_D) was set to $1.28x10^{12}cm^{-3}$, corresponding to a resistivity of ~ 3.4 kΩ cm) of a high resistivity n-type Si substrate and the N_D was 6.28 $x10^{12}cm^{-3}$ (experimentally calculated from the slope of $1/C^2$ versus V_g in the depletion region of MOS) in the depletion region of MOS test structure (up to 20 μm from Si-SiO_2 interface). Therefore non-uniform doping profile obtained in the bulk of Si material. The insulator SiO_2 thickness (t_{ox}) was taken to 0.405 μm in the simulation. The value of oxide charge density (N_{ox}) was taken from the experimental measurement (from flat band voltage, V_{fb}) of non-irradiated gated diode and interface charge trap density (N_{it}) of 2.1 x 10^{10} cm^{-2} was calculated from the experimental measured surface current (I_{ox}). The MOS test structure is assumed to be an ideal (only N_{ox}) and in practical non-irradiated MOS test structure (both N_{ox}, N_{it} present). In simulation, it was assumed that there was donor, acceptor interface trap at

mid band gap of silicon, acceptor and donor interface trap at trap energy level (E_t) of 0.16 eV from conduction band (homogeneous distribution in the band gap of Si), and also double acceptor at 0.16 eV and 0.26 eV from the conduction band just to check the shape of the C/V_g characterstics in the different section of simulated results. The effective-capture cross-section (σ_{eff}) of charge carrier of 7 x 10^{-17} cm^2, time constant (τ_{eff}) of 130 μs , surface recombination velocity (S_0) of 2.4 cm/sec and thermal velocity of charge carriers (v_{th} (n/p)) of 2 x 10^7 cm/sec was used for all simulations of non-unirradiated MOS test structure. In the present work, time constant is modelled as effective life time of charge carriers. For small-signal AC analysis for C/V_g characteristics simulation of MOS test structure is performed at TCAD default temperature ($T_{lattice}$=300K), we have applied 0.1 volt AC voltage with DC gate contact voltage of -1 to -12 volt for three range of frequency (f) i.e. 5, 10 and 15 kHz.

Homogeneous (reflecting) Neumann boundary conditions are applied on the non-contacted outer ages of the structures. The ohmic contact on the backside is on ground and the front side of MOS with aluminium gate are implemented by Dirichlet boundary conditions. $Ø_{MS}$ (work function difference between aluminium metal and n-Si) of -0.69 volt was used for given doping concentration.

3. Simulation procedures

The above-mentioned MOS test structure design is used to study the effect of different physical and process parameters on the C/V_g characteristics of MOS test structure using the two-dimensional device simulation software program ISE T-CAD DESSIS [12].

Simulations in 2-D were performed using a device simulation software package ISE-T-CAD of Integrated Systems Engineering (ISE). Subprograms MDRAW-ISE and DESSIS-ISE of ISE-TCAD were used to perform the physical simulations and subprograms TECPLOT-ISE and INSPECT-ISE were used for the visualization and analysis of the result data, respectively.

DESSIS-ISE: DESSIS-ISE simulates the electrical characteristics of semiconductor devices. It contains a comprehensive set of physical models, handles 2D and 3D geometries, mixed-mode circuit simulation with compact models, and numeric devices. In addition, one is able to perform mixed-mode transient simulations in 3D to study the charge collection characteristics of the detector structure. At each simulation step, the Poisson equation along with the continuity equations is solved using a Newton iteration method. A quasi-stationary simulation is used to ramp the bias voltage in a way that at each bias step the simulation is restarted after alternation of the parameter values and the boundary conditions.

INSPECT-ISE: INSPECT-ISE permits the analysis of the simulated x–y data, the extraction of characteristic data from TECPLOT-ISE. The final plots can be printed in ps or encapsulated ps (eps) form and .png form.

DESSIS solves the Poisson equation, the continuity equation, the energy–balance equation and the lattice heat equation for holes and electrons and traps. All of the above equations describe the static and dynamic behaviour of charge carriers and interface trap in semiconductors under the influence of the electric field. The physical models used throughout the simulations were picked up from the ISE-DESSIS physical model library.

Doping dependent Shockley-Read-Hall (SRH) recombination, Auger recombination, charge trap model at Si-SiO_2 interface, impact ionization, doping-dependent mobility, high field saturation models, surface recombination, lucky physical model for gate current is taken into account in the present simulation.

For C/V_g characteristics of MOS test structure, we have done mixed mode simulation i.e. device and SPICE (Simulation Program of Integrated Circuit with Emphasis) in ISE T-CAD DESSIS. For small signal AC analysis to obtain small signal admittance (Y) matrix, it will current response at a node to a small signal voltage (v) and can be expressed as follows,

$$i = Y.v = (G + j\omega C).v \qquad [1]$$

, where i is small signal current vector (at all nodes) and v is voltage vector.

The capacitance will be measured in parallel mode and AC analysis of MOS test structure gives the conductance (G) and capacitance (C) matrix for every gate voltage. Oxide capacitances (C_{ox}), high frequency inversion capacitance (C_{inv}), flat band voltage (V_{fb}) (for known N_{ox} from experimental result), interface trap density (N_{it}) (for single level trap of homogeneous distribution) calculation was done from standard equation for this numerical modelling just for cross check our simulated result [13-14].

4. Result and discussions

In this paper, numerical device simulation has been exploited in order to see the effect of various physical and process parameters (N_{ox}, N_{it}, f, resistivity ρ, interface trap types) , which is taken into account for surface damage analysis on C/V_g characteristics.

Fig.2a shows the C/V_g characteristics of an ideal (no interface trap only N_{ox}) and practical non-irradiated MOS test structure (with N_{ox} and N_{it} both). When there was only N_{ox} used then V_{fb} was -5.32 volt but when I have taken the single level acceptor trap at mid gap of Si with N_{ox} then V_{fb} was -5.69 volt. It has been found that C/V_g curve is stretched (depletion region) in the presence of interface trap due to movement of Fermi level in Si band gap and V_{fb} is modified up to 0.37 volt due to interface trap. Therefore, we can say flat band voltage (V_{fb}) will be modify by N_{ox} and N_{it} both and there is no change observed in CMOS oxide capacitance (C_{ox}) and high frequency inversion capacitance (C_{inv}).

Fig.2 (b) shows the G/V_g of non-irradiated MOS test structure in presence of acceptor trap at mid gap and no trap only N_{ox} (ideal MOS). In order to understand the G/V_g characteristics, we can divide G/V_g characteristics into three zones i.e. conductance in accumulation region (**$G_{accumulation}$**), conductance peak (**G_{peak}**) **and** conductance in inversion region (**$G_{inversion}$**).

For the first zone, **$G_{accumulation}$** is same for an ideal MOS and practical MOS test structure and it is related to the bulk/series resistance (R_s) of the bulk silicon material. It is observed that R_s remain constant for same device depth (W_N). **G_{peak}** is very sensitive to interface trap concentration at certain gate bias, traps will be active and thus giving rise to their long peak

in the presence of traps (practical MOS test structure). $\mathbf{G_{inversion}}$ is affected by constant doping concentration in the depletion region of MOS test structure and measurement temperature. It has been found that that $\mathbf{G_{peak}}$ is at almost around V_{fb} because interface traps are very sensitive at this gate bias and thus giving long peak.

Fig.3 shows the comparison of data and simulation of C/V_g characteristics for practical MOS test structure at three different frequencies (5 , 10 and 15 kHz) for single level donor interface trap at mid gap with same trap concentration as per the previous acceptor interface level trap. There is in good agreement observed with experimental data for three different frequencies. Thus, we can say that the simulator has been rigorously calibrated against experimental data. It has been found that there is no frequency dispersion effect in strong accumulation (change of C_{ox} with frequency) for this frequency range in non-irradiated MOS test structure because of low N_{it}.

In Fig.4, the influences of different interface trap types on C/V_g characteristics are shown. It has been found that interface trap modified V_{fb} but different trap shows a little change in slope of the C/V_g curve in the depletion to inversion region because of fixed low N_{it}.

The influence of N_{ox} is clearly visible in Fig.5 just for cross-check our simulated result, when N_{ox} increases from 1.97 x 10^{11} cm^{-2} to 2.67 x 10^{11} cm^{-2} (N_{ox} experimental) at 10 kHz frequency then V_{fb} also increases. It is well known effect flat band shift will observe when increasing N_{ox}.

In Fig.6, C/V_g characteristics for High resistivity Silicon, HRS (3.4 kΩ cm) is differ from low resistivity silicon, LRS (200 Ω cm) and it is due to high potential drop and increase of debye length.

5. Conclusions

We have shown the good description of C/V_g characterstics as function of low frequency where the interface trap will respond and there is good agreement observed in the experiment results and simulation. It should be noted that the very preliminary simulation results on non-irradiated MOS capacitor for C/V_g characterization are presented for the surface charge and

resistivity effect and the detailed comparison of experiment and simulation for irradiated MOS capacitors at different high frequency are under way.

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FIGURE CAPTION

Figure.1a: Cross-section of MOS test structure used in the simulation work.

Figures.1b: Rectangular grid of MOS test structure (50 x 50 μm^2).

Figure.2 (a): C/V_g characteristics of non-irradiated MOS structure in presence of acceptor trap at mid gap and no trap only N_{ox} (Ideal MOS).

Figure.2 (b): G/V_g of non-irradiated MOS test structure in presence of acceptor trap at mid gap and no trap only N_{ox} (Ideal MOS).

Figure.3: C/V_g of non-irradiated MOS test structure in the presence of donor level trap at mid gap of Si for three frequency (a) 5 kHz (b) 10 kHz (c) 15 kHz : comparison with data from experiment.

Figure.4: C/V_g of non-irradiated MOS test structure at one fixed frequency 10 kHz for different traps types.

Figure.5: C/V_g of non-irradiated MOS test structure at one fixed frequency 10 kHz for different oxide charge density.

Figure.6: C/V_g of non-irradiated MOS test structure at one fixed frequency 10 kHz for single level acceptor trap, E_c-E_t=0.16 eV (from conduction band) for two resistivity (low and high) of Si material.

LIST OF FIGURES

FIG.1 a

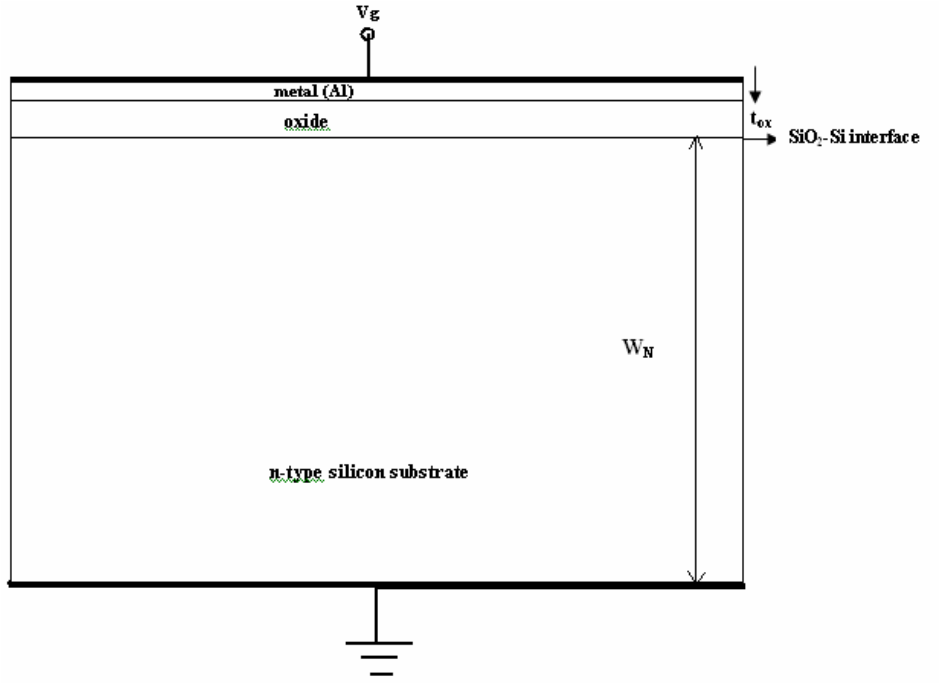


FIG.1 b

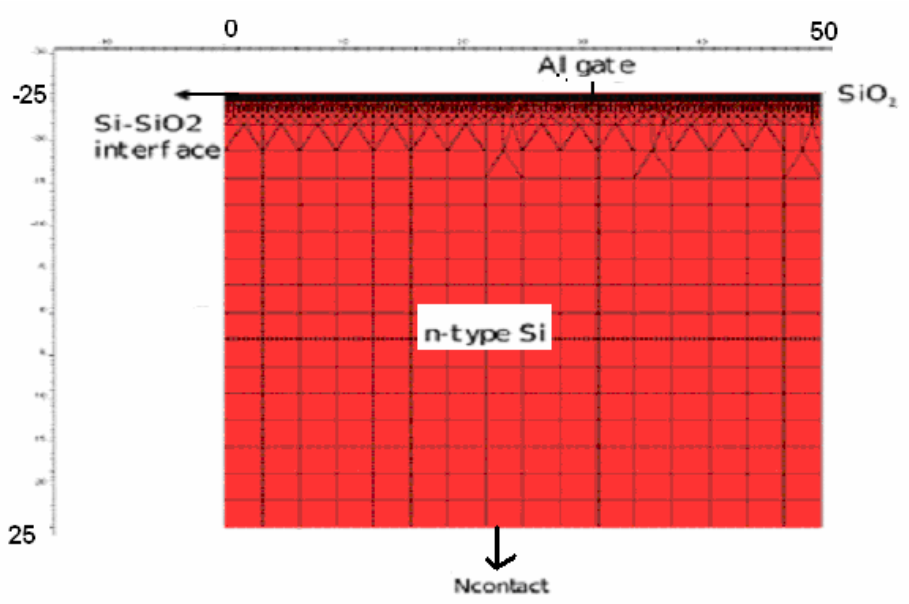


FIG.2 a

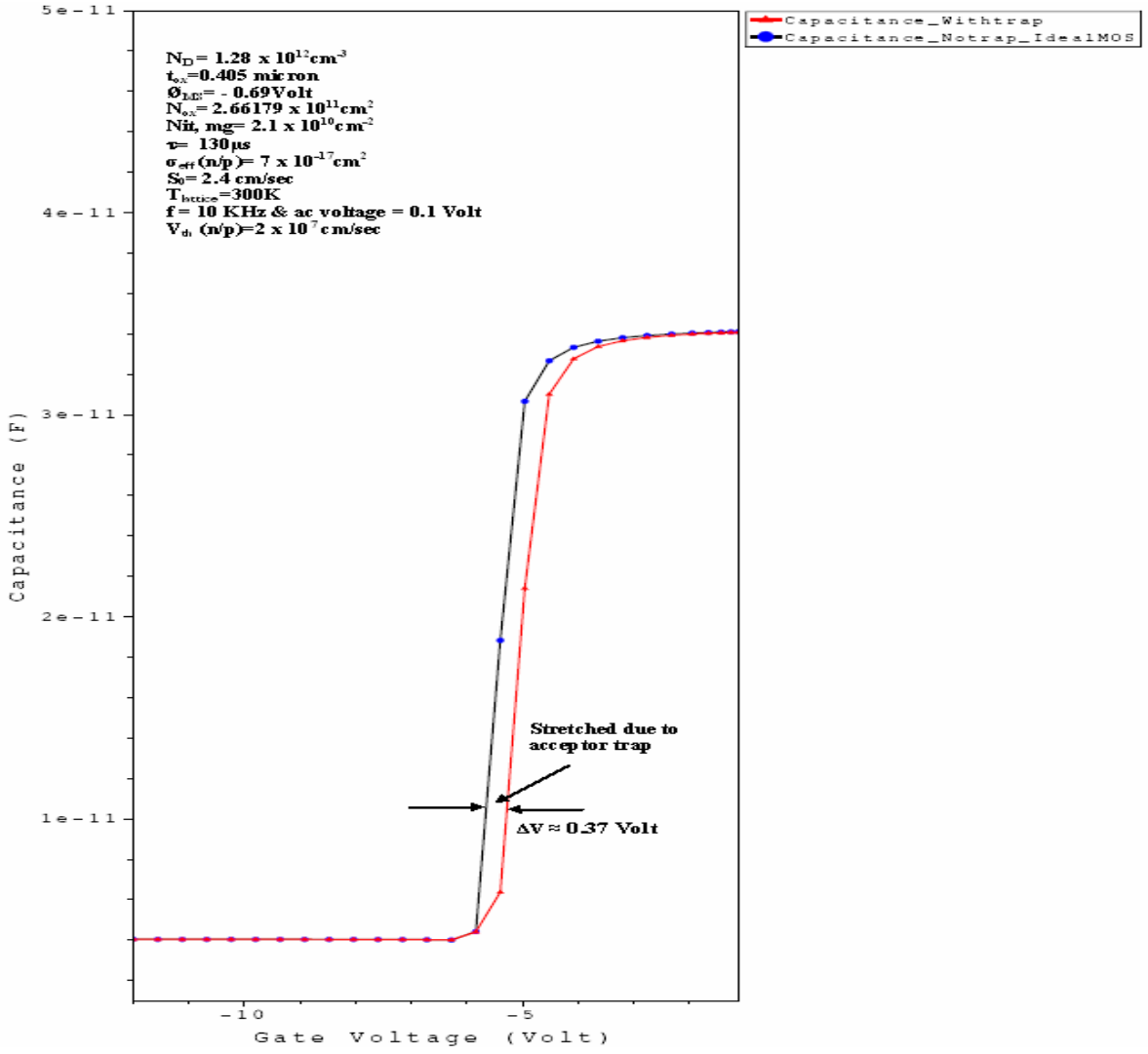

Capacitance_Withtrap
Capacitance_Notrap_IdealMOS
N_D= 1.28 x 10^{12}cm^{-3}
t_{ox}=0.405 micron
$Ø_{MS}$= - 0.69Volt
N_{ox}= 2.66179 x 10^{11}cm^{-2}
Nit, mg= 2.1 x 10^{10}cm^{-2}
τ= 130μs
$σ_{eff}$ (n/p)= 7 x 10^{-17}cm^{2}
S_0= 2.4 cm/sec
$T_{lattice}$=300K
f = 10 KHz & ac voltage = 0.1 Volt
V_{th} (n/p)=2 x 10^{7} cm/sec
Stretched due to acceptor trap
ΔV ≈ 0.37 Volt
Capacitance (F)
5e-11
4e-11
3e-11
2e-11
1e-11
-10
-5
Gate Voltage (Volt)

FIG.2 b

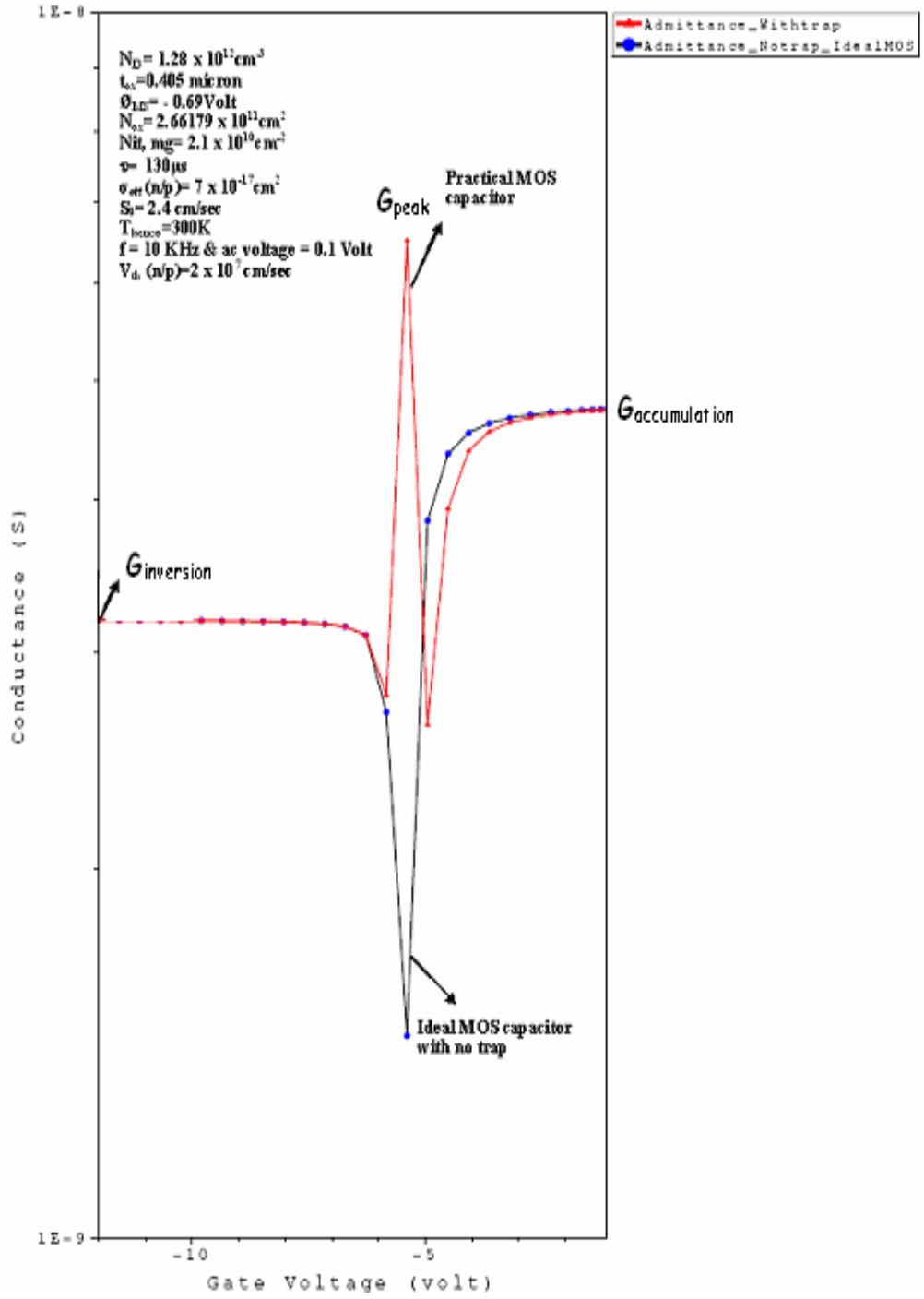
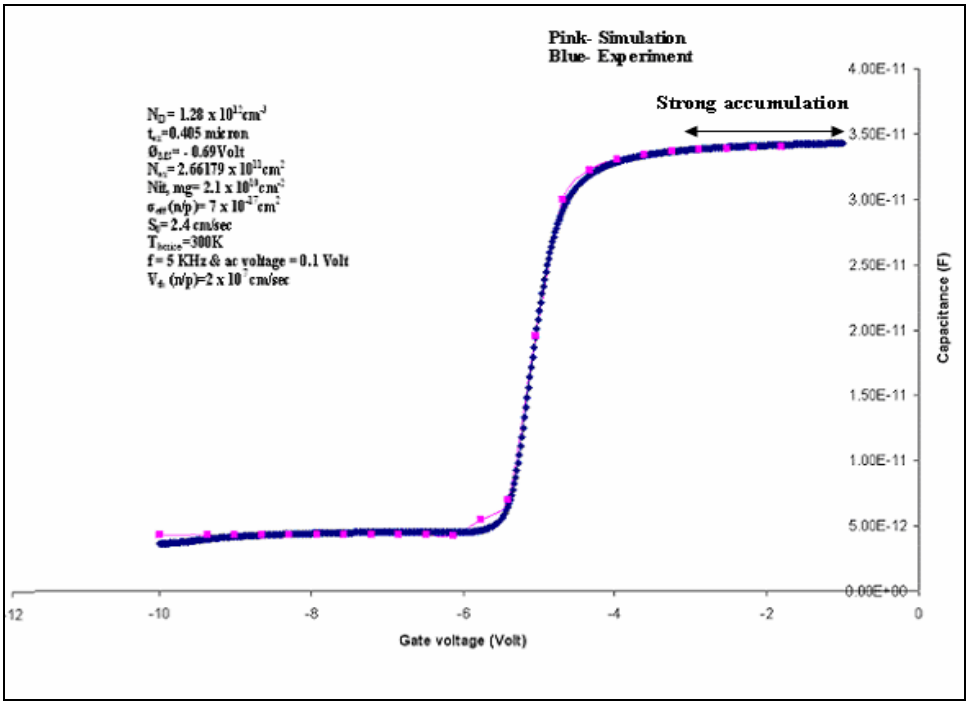
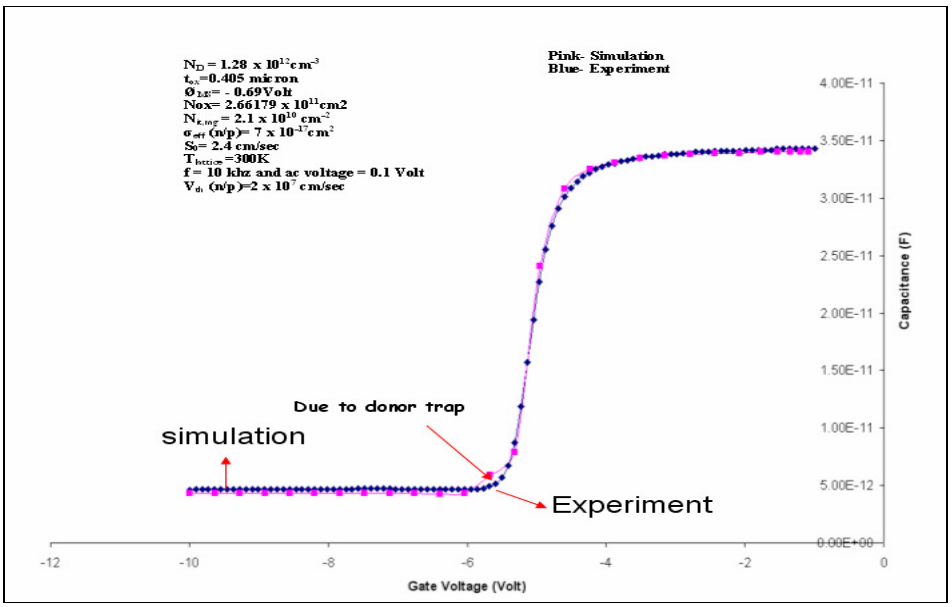

Admittance_Withtrap
Admittance_Notrap_IdealMOS
N_D= 1.28 x 10^{12}cm^{-3}
t_{ox}=0.405 micron
Φ_{MS}= - 0.69Volt
N_{ox}= 2.66179 x 10^{11}cm^{-2}
Nit, mg= 2.1 x 10^{10}cm^{-2}
τ= 130µs
σ_{str} (n/p)= 7 x 10^{-17}cm^{2}
S_0= 2.4 cm/sec
$T_{lattice}$=300K
f = 10 KHz & ac voltage = 0.1 Volt
V_{th} (n/p)=2 x 10^{7} cm/sec
G_{peak}
Practical MOS capacitor
$G_{accumulation}$
$G_{inversion}$
Ideal MOS capacitor with no trap
1E-0
1E-9
-10
-5
Conductance (S)
Gate Voltage (volt)

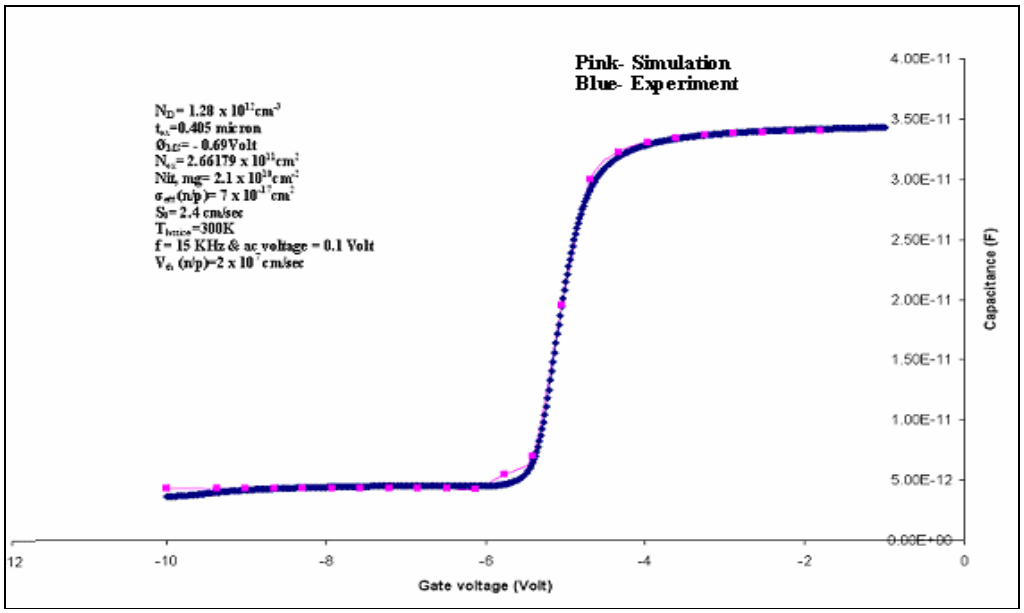
Fig.3


Pink- Simulation
Blue- Experiment
N_D= 1.28 x 10^{15}cm^{-3}
t_{ox}=0.405 micron
$\emptyset_{MS}$= - 0.69Volt
N_{ox}= 2.66179 x 10^{11}cm^{-2}
Nit, mg= 2.1 x 10^{11}cm^{-2}
$\sigma_{n/p}$ (n/p)= 7 x 10^{-17}cm^{2}
S_0= 2.4 cm/sec
T_{heat}=300K
f = 5 KHz & ac voltage = 0.1 Volt
V_{th} (n/p)=2 x 10^{7} cm/sec
Strong accumulation
4.00E-11
3.50E-11
3.00E-11
2.50E-11
2.00E-11
1.50E-11
1.00E-11
5.00E-12
0.00E+00
Capacitance (F)
12
-10
-8
-6
-4
-2
0
Gate voltage (Volt)

(a)


Pink- Simulation
Blue- Experiment
N_D = 1.28 x 10^{12}cm^{-3}
t_{ox}=0.405 micron
$Ø_{MS}$= - 0.69Volt
Nox= 2.66179 x 10^{11}cm2
$N_{it,mg}$ = 2.1 x 10^{10} cm^{-2}
σ_{eff} (n/p)= 7 x 10^{-17}cm^{2}
S_0= 2.4 cm/sec
$T_{lattice}$=300K
f = 10 khz and ac voltage = 0.1 Volt
V_{th} (n/p)=2 x 10^{7} cm/sec
Due to donor trap
simulation
Experiment
Capacitance (F)
Gate Voltage (Volt)

(b)


Pink- Simulation
Blue- Experiment
N_D= 1.28 x 10^{11}cm^{-3}
t_{ox}=0.405 micron
$Ø_{MS}$= - 0.69Volt
N_{ox}= 2.66179 x 10^{11}cm^{-2}
Nit, mg= 2.1 x 10^{10}cm^{-2}
σ_{eff}(n/p)= 7 x 10^{-17} cm^{2}
S_0= 2.4 cm/sec
$T_{lattice}$=300K
f = 15 KHz & ac voltage = 0.1 Volt
V_{th} (n/p)=2 x 10^{7} cm/sec
Capacitance (F)
Gate voltage (Volt)

(c)

FIG.4

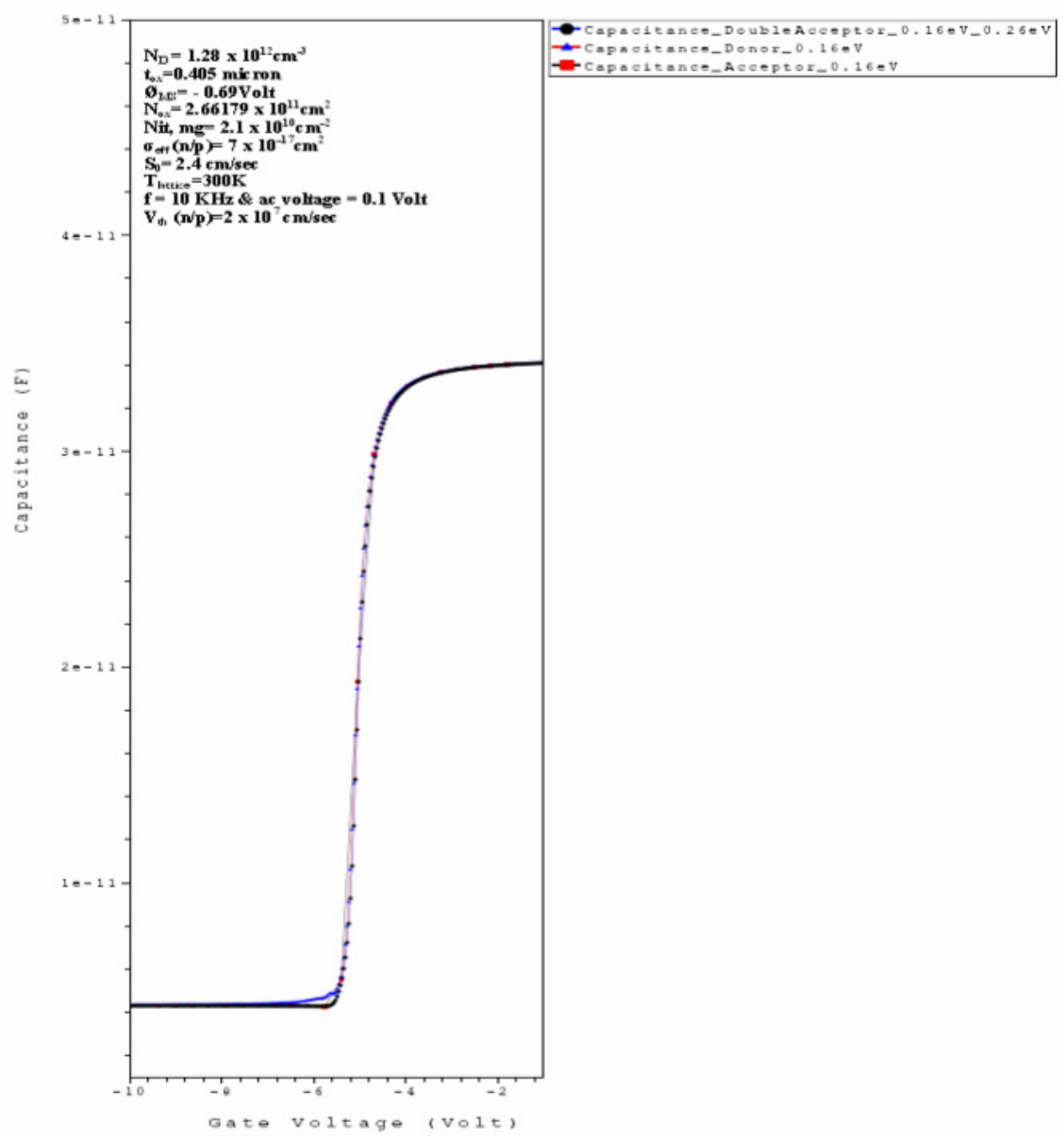

Capacitance_DoubleAcceptor_0.16eV_0.26eV
Capacitance_Donor_0.16eV
Capacitance_Acceptor_0.16eV
N_D = 1.28 x 10^12 cm^-3
t_ox=0.405 micron
Ø_MS= - 0.69Volt
N_ox= 2.66179 x 10^11 cm^-2
Nit, mg= 2.1 x 10^10 cm^-2
σ_eff (n/p)= 7 x 10^-17 cm^2
S_0= 2.4 cm/sec
T_lattice=300K
f = 10 KHz & ac voltage = 0.1 Volt
V_th (n/p)=2 x 10^7 cm/sec
5e-11
4e-11
3e-11
2e-11
1e-11
Capacitance (F)
-10
-8
-6
-4
-2
Gate Voltage (Volt)

FIG.5

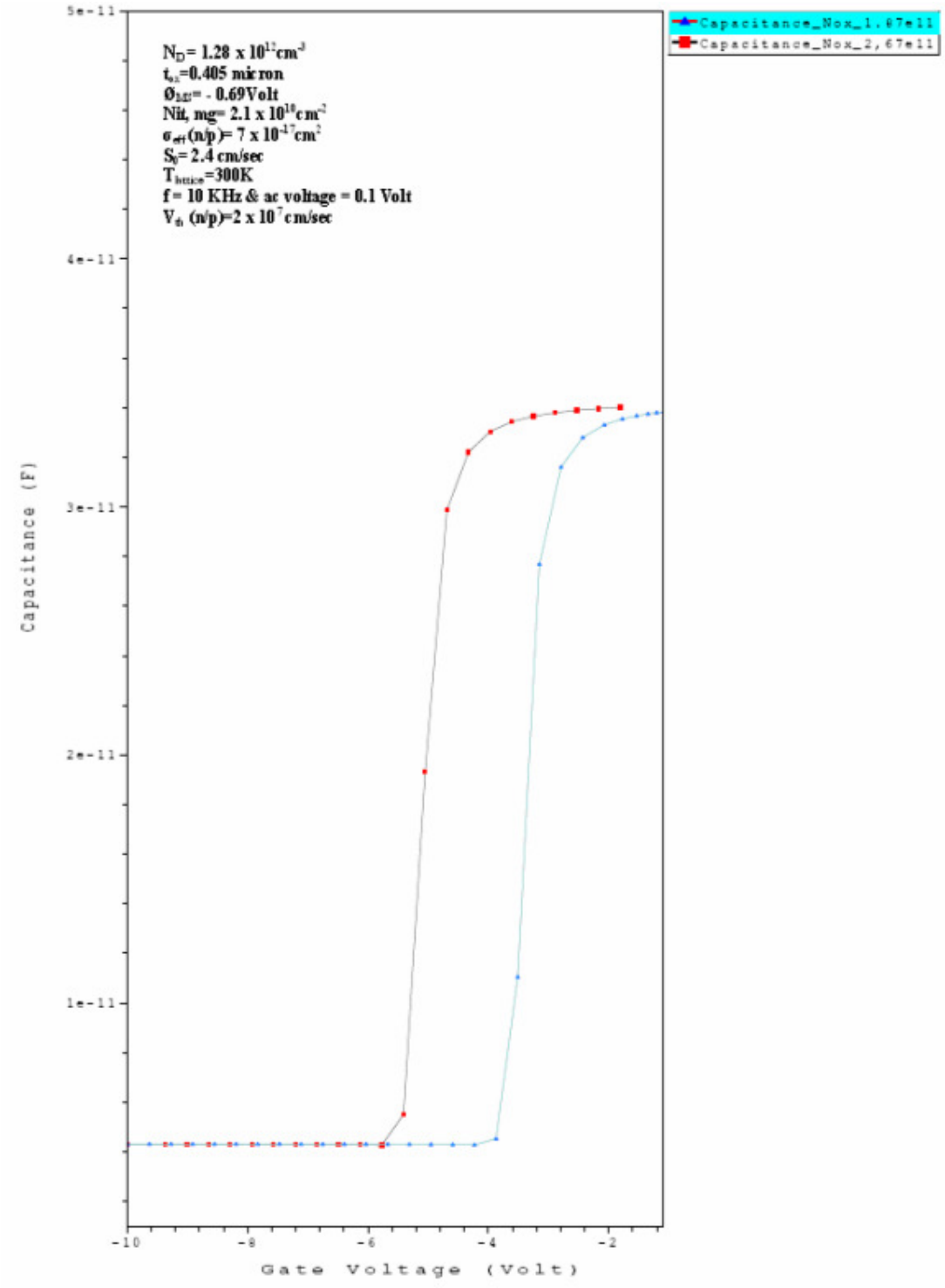
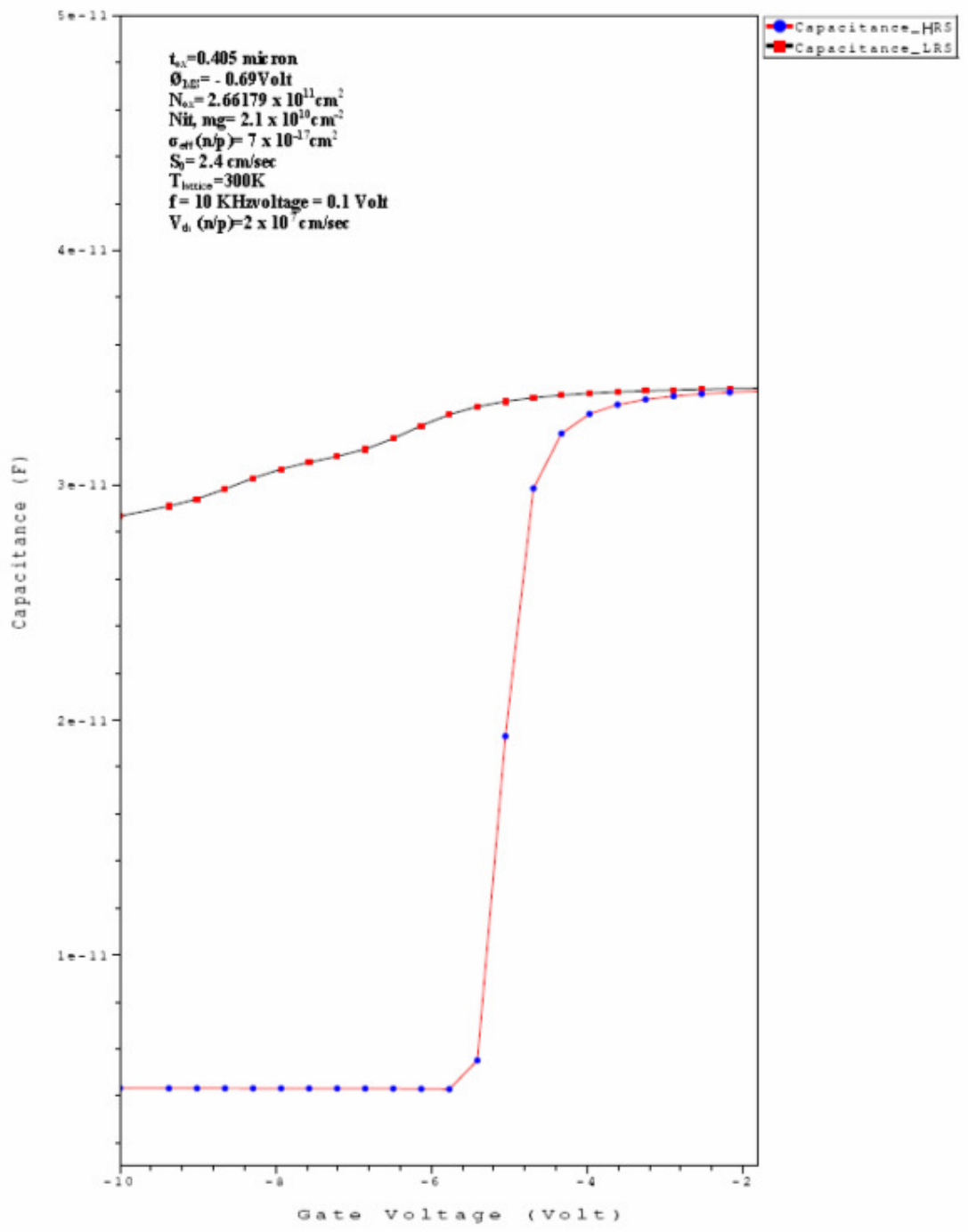

Capacitance_Nox_1.67e11
Capacitance_Nox_2.67e11
N_D= 1.28 x 10^{12}cm^{-3}
t_{ox}=0.405 micron
$Ø_{MS}$= - 0.69Volt
Nit, mg= 2.1 x 10^{10}cm^{-2}
σ_{eff} (n/p)= 7 x 10^{-17}cm^{2}
S_0= 2.4 cm/sec
$T_{lattice}$=300K
f = 10 KHz & ac voltage = 0.1 Volt
V_{th} (n/p)=2 x 10^{7} cm/sec
Capacitance (F)
5e-11
4e-11
3e-11
2e-11
1e-11
-10
-8
-6
-4
-2
Gate Voltage (Volt)

FIG.6


Capacitance_HRS
Capacitance_LRS
t_{ox}=0.405 micron
$Ø_{MS}$= - 0.69Volt
N_{ox}= 2.66179 x 10^{11}cm^{-2}
Nit, mg= 2.1 x 10^{10}cm^{-2}
σ_{eff} (n/p)= 7 x 10^{-17}cm^{2}
S_0= 2.4 cm/sec
$T_{lattice}$=300K
f = 10 KHzvoltage = 0.1 Volt
V_{di} (n/p)=2 x 10^{7} cm/sec
5e-11
4e-11
3e-11
2e-11
1e-11
Capacitance (F)
-10
-8
-6
-4
-2
Gate Voltage (Volt)