Numerical Modelling of the Frequency Behaviour of Irradiated MOS Test Structure

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Internal note (within AGIPD collaboration)

Abstract: In future European X-Ray Free-Electron-Laser (XFEL) experiment at DESY, Hamburg will set new standards in luminosity for X-ray synchrotron sources, and Si pixel detectors with a high dynamic range in the images (one to $>10^4$ photons/pixel) and a radiation tolerance of 1GGy ($\approx 10^{16}$ 12 keV photons/cm^2) will be used. Surface radiation damage studies of X-Rays in sensors are important for radiation hardening of sensors for three year of XFEL operation. Test structures (gated diode and CMOS capacitors) were fabricated by CiS, Erfurt, Germany, irradiated up to 1GGy, and the Current-Voltage (I/V_g), Capacitance-Voltage (C/V_g) measurements as function of gate bias and frequency and TDRC (Thermally Dielectric Relaxation Current) measurements have been performed for the study of ionization radiation effects in the SiO_2 and at the Si-SiO_2 interface. C/V_g and G/V_g technique is widely used for the study of radiation induced surface charges in the MOS test structure. In this paper, we have performed simulation of irradiated MOS test structure as a function of frequency (50-800 kHz) using microscopic parameters obtained from the measurements using ISE T-CAD DESSIS 2-D device simulator. It should be noted that very preliminary simulation results and observations are presented here.

Keywords: device simulation, surface damage, MOS capacitor, frequency, capacitance, interface trap.

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1. Introduction

The expected run of European XFEL experiment in 2013 at DESY, Hamburg, Germany this will open new solutions in fourth generation of photon sciences. In the absence of bulk damage ($E_\gamma <$ threshold for bulk damage is 300 keV) in Si pixel sensors, the surface damage due to X-ray irradiations are very important for the long term performance of the sensors. The sensors should be more radiation tolerant against surface damage [1-4].

The common way of classifying radiation effects from a physical point of view is based on the distinction between bulk damage and surface damage. The most common ionizing radiation surface effects in the oxide are charge trapping, i.e. charge freezing in the oxide, leading to recombination centers formation and increase of interface state density at the Si-SiO_2 interface. The shift in flat band voltage of MOS test structure is due to increase of oxide charge density and also increase of interface trap density and they will change the electric field distribution [2]. Dark current is main source of noise and it will come through high interface trap density, which impacts on the read-out electronics and may result in an increase of noise. Actually interface traps are electrically active defect located at the interface between oxide and Si; capable of trapping and de-trapping charge carriers, thus interface traps have an adverse effect on device performance.

Here, the some of the important microscopic theory of oxide charge density (N_{ox}) and interface traps density (N_{it}) are presented. Actually, the oxide trapped charge density is also known as *E'* centers and indicated by N_{ox} and the interface state density as P_b centers and indicated by N_{it}. *E'* is oxide charges in the bulk of SiO_2 and in the

SiO_2 -side of the interface (form 500 down to 5 nm far from the Si). . E' comes from an oxygen vacancy that implies a Si dangling bond and it is also often addressed as $O_3 \equiv Si$ and P_b center lie on Si- SiO_2 interface and are due again to a dangling bond, this is called interface trap. Interface traps are unstable and can be positively or negatively charged. Oxide traps are stable and always positive. It is worth to notice that between 1 and 10 atomic layers in the SiO_2 near the interface hybrid traps have been found; these traps show an intermediate behavior between the E' and the P_b, and for this reason they have been called border traps [5]. Apart from this, the interface traps employed are the donor and acceptor states modeled according to the known P_{b0} centers. The donor states are centered at 0.25eV above the silicon valence band maximum and acceptor states 0.3eV below the conduction-band minimum [5]. The donor states are neutral when filled with electrons and positively charged when empty. On the other hand, the acceptor states are negatively charged when filled with electrons and neutral when empty. The effect due to P_{b1} centers has been neglected for the obscurity in band gap distribution of this trap species.

The C/V_g and G/V_g techniques are widely used as function of frequency for the understanding of radiation induced interface trap. Very rare attempts has been made to describe the donor and acceptor nature of interface traps and also frequency behavior of irradiated MOS test structure [2,6] using 2-D TCAD device simulation tool.

An important tool for the study of the frequency response of irradiated MOS test structure is ISE-TCAD DESSIS 2-D device simulator version 2005.10 [7]. In this work, the simulator has been rigorously calibrated against experimental data reported in literature. In sections 2 below, device design and high frequency model for C/V_g

characterization is summarized. Simulation procedures are presented in sections 3 and theoretical calculation and high frequency (HF) model for the correction in capacitances and conductance's for the MOS test structure is discussed in section 4. Simulation results are covered in section 5. Conclusions are finally given in section 6.

2. Device design and high frequency (HF) model for C/V_g characterization

For simulation purpose, we have considered simple two-dimensional MOS test structure of 0.0404 mm^2 x 300 μm is shown in Fig.1a and Fig.1b shows its high frequency model used for the modelling of non-uniform doping profile of bulk Si (this gives good description of C/V_g as function of frequency [2]). The concentration of the bulk n-type impurities is constant and set to 6.28 x 10^{12} cm^{-3} in the 20 μm from Si-SiO_2 interface, and 1.28 x 10^{12} cm^{-3} in the bulk of Si corresponding to a resistivity of ~ 3.4 kΩ cm. Table.1 shows the list of geometrical parameters used in the present simulation of MOS test structure design and Table.2 represents the some of the useful parameters taken from experimental measurements. In all simulations of 0.5 MGy irradiated MOS test structure, we have used the N_{ox} = 2.48 x 10^{12} cm^{-2} from experiment and assumed, single level of acceptor interface trap concentration (N_{it}), 3.93x10^{13} cm^{-2} at level of E_c-E_t=0.4 eV (assumed for simulation) from the conduction band in the band gap of Si material and the effective capture-cross-section ($\sigma_{eff} = \sigma_n = \sigma_p$) of charge carriers (electron and holes) for capture by acceptor trap which typically have value of 7x 10^{-17} cm^2. The simulated gate area is normalized to the experimentally measured gated area for the good description of C_{ox}. At these contact (See Fig.1a), Dirichlet boundary conditions are

applied to the electrostatic potential. Along the remaining boundaries, homogeneous Neumann (reflecting) boundary conditions

$$\mathbf{J_n.n=0} \qquad \mathbf{J_p.n=0} \tag{1}$$

Apply, where n is the unit vector orthogonal to the surface and j_n, j_p are the electron and hole currents, respectively. $Ø_{MS}$ (work function difference between aluminum metal and n-Si) of -0.69 volt was used for given doping concentration.

3. Simulation Procedure

The above-mentioned MOS test device structures is used to study the frequency dispersion effect (change of C_{ox} with frequency on the C/V_g of MOS test structure using the two-dimensional device simulation software program ISE-T-CAD DESSIS version 2005.10 [7].

DESSIS solves the Poisson equation, the continuity equation for holes and electrons in the presence of traps. All of the above equations describe the static and dynamic behaviour of carriers in semiconductors under the influence of the electric field. Physical models; Shockley- Read-Hall (SRH) recombination, impact ionization , Auger recombination, doping dependent mobility, high field saturation model, interface trap model at Si-SiO_2 interface, impact ionization, and lucky model for gate current are taken into account in DESSIS version 2005.10 to recognize MOS test structure performance after irradiation. In simulator, dependence of time constant is taken into account through effective generation life time of charge carrier.

For C/V_g characteristics of MOS test structure, mixed mode simulation i.e. device and SPICE (Simulation Program of Integrated admittance (Y_p) of the Circuit

with Emphasis) is performed in DESSIS. DESSIS calculates the matrix of parallel capacitances (C_p) and parallel conductance's (G_p) at different gate voltages. For the parallel circuit, the admittance (Y_p) is given by;

$$Y_p = G_p + j\omega C_p \qquad [2]$$

In order to calculate, the serial capacitance, the following expression is used;

$$C_S = C_P(1 + \frac{1}{Q^2{}_P}) \qquad [3]$$

, where ($Q_P=\omega R_p C_p$) is the quality factor for the parallel model of circuit. Fig.2a and Fig.2 b shows the C/V_g measurement of MOS test structure in parallel and serial mode.

4. Theoretical calculation

In this present work, we have also done the theoretical calculations just for cross check for the value of C_{ox} and high frequency inversion capacitance for given doping concentration [8].

4.1 High frequency model for correction in capacitance and conductance

Due to discrepancies during processing, such as cleaning (less impact if cleaning is good) and mainly after low irradiation high interface trap density will be introduced at Si-SiO_2 interface of MOS test structure, an unwanted lossy dielectric layer will be developed at Si-SiO_2 interface causing the measured capacitance in strong accumulation to be high frequency dependent (>100 kHz). This is also may be due to the uncorrected series resistance (R_{SB}) of 6-7 kΩ of bulk of Si material in the inversion region of MOS

test structure at different frequency. This can be better understand from G/V_g characterstics as function of frequency, no conductance peak will be observed in the presence of uncorrected R_{SB} at high frequency (>100 kHz) and for the correction in R_{SB}, approx. 3 kΩ series resistance (it can be calculated from [8]) will be used from the accumulation to the inversion region of MOS test structure and G_{acc}, G_{inv} ([2, 8]) will be in same level.

In this sub-section, we have showed HF model for the correction in capacitances (imaginary part) and conductance's (real part) of C/V_g of MOS test structure in the presence of an unwanted lossy dielectric layer at Si-SiO_2 interface [9]. But in the present work of simulation, we have used this model only for the correction in capacitance (C_c).

Corrected capacitance (C_c) and conductance (G_c) is given by following expression [9];

$$C_c = \frac{(\omega^2 C_m C_E - G_m^2 - \omega^2 C_m^2)(G_m^2 + \omega^2 C_m^2)(C_E)}{(\omega^2 C_E^2)[G_m(1 - R_s' G_m) - \omega^2 R_s' C_m^2]^2 + (G_m^2 + \omega^2 C_m^2 - \omega^2 C_m C_E)^2} \qquad [4]$$

$$G_c = \frac{[G_m(1 - R_s' G_m) - \omega^2 R_s' C_m^2](G_m^2 + \omega^2 C_m^2)(\omega^2 C_E^2)}{(\omega^2 C_E^2)[G_m(1 - R_s' G_m) - \omega^2 R_s' C_m^2]^2 + (G_m^2 + \omega^2 C_m^2 - \omega^2 C_m C_E)^2} \qquad [5]$$

In equation 4 and 5, a numbers of symbols used like ω, C_{ox} , C_D, Y_{it}, C_T, R_T , C_E, R_E, R_s (here same R_{SB}) , $R_s' = R_s + R_E$, C_{ma}, G_{ma}, C_m and G_m are known as angular frequency ($\omega = 2\pi f$) oxide capacitance, depletion layer capacitance, admittance, capacitance , resistance due to unwanted lossy layer, lossy layer capacitance, , lossy layer resistance,

series resistance, total series resistance, capacitance in strong accumulation, conductance in strong accumulation, measured capacitance, measured conductance [9].

5. Simulation results

In this paper, we have done 2-D device simulation of irradiated MOS test structure as function of frequency. Simulations were performed in order to investigate the influence of high frequency on the measured capacitance in the strong accumulation region of the C/V_g characteristics of MOS test structure.

In our earlier work, it has been shown that that there is no frequency dispersion effect observed in the strong accumulation region of non-irradiated MOS test structure and the simulator has been already rigorously calibrated with experimental data at three low frequency[2].

Fig.3a shows the C/ V_g characteristics of irradiated MOS test structure with 0.5MGy at different high frequencies. Flat band voltages (V_{fb}) are measured at flat band capacitance (C_{FB}) for different frequency (see Fig.3a). It can be seen that when an increasing HF from 50 kHz to 800 kHz then V_{FB} decreases and C_{ox} has no frequency dependency for the HF <100 kHz which means that there is no frequency dispersion effect observed up to 100 kHz. But, it has been also found that C_{ox} changes with frequency only for higher frequencies if HF > 100 kHz. So we can say that C_{ox} is strongly frequency dependent for HF > 100 kHz whereas C_{inv} is constant.

Fig.3b shows the comparison of simulation results (50, 200 and 800 kHz) and experiment data at higher frequency (50, 500 and 800 kHz, no data for 200 kHz) just for cross-check the behaviors observed in the Fig.3a. It can be also seen that in Fig.3b, the

similar behavior is obtained which means that at high frequencies, C_{OX} are frequency dependent. There is in good agreement in C_{ox} and C_{inv} between experimental data and simulation at 50 kHz but the slope is not reproduce, this is just due to taken assumed interface trap in the present simulation work. At higher frequencies, there is a disagreement in C_{ox} and problem in C_{inv} at high frequency, reason not well understood.

It should be noted the preliminary comparison of results are presented. It is planned to take experimentally measured microscopic interface trap parameters from the TDRC signal versus E_c-E_t curve (peak of DOS gaussian profile of interface trap (cm^{-2} eV^{-1}) distribution in the band gap of Si with E_c-E_t from conduction band and width of gaussian σ_{it} (eV)) for detailed comparison of simulation result and experiment data as a function of frequency.

It can be seen that measured strong accumulation (V=-15 Volt) capacitance (C_{ma}) decreases with increasing frequency (see Fig.4). In actual, C_{ma} should constant with frequency variations.

Very preliminary understanding of simulated conductance–voltage (G/V_g) characterstics for 0.5 MGy irradiated MOS test structure as a function of frequency in Fig.5a. It has been found that G/V_g characterstics is strongly dependent on frequency. This is because of that interface traps are active at different small signal AC frequency and does not respond at very high frequency like 1 MHz and thus it is giving different values in all zone ($G_{accumulation}$, G_{peak} and $G_{inversion}$ [2]) at different frequency. The shape and peak of the G/V_g characterstics depends upon the distribution of the charge carrier (oxide charge, interface trap) at Si-SiO_2 interface.

Whereas, measured conductance in strong accumulation conductance (G_{ma}) increases with frequency (see Fig.5b).

Fig.6 shows the simulated serial capacitance (C_s) versus gate voltage and frequencies are as running parameter. It is clear that from Fig.7, simulated C_p at 50 kHz is less that than C_S at same frequency. The similar frequency dispersion effect is also observed for serial C/V_g characteristics (see Fig.7).

Fig.7 shows the C_c (corrected) parallel capacitance from the high frequency model at three different frequencies. It is observed that in Fig.6 there is no change in C_{ox} in strong accumulation region (1-2 % error) i.e. no frequency dispersion effect.

6. Conclusion

It has been found that irradiated MOS test structure is strongly dependent on frequency in terms of decrease of flatband voltage due to increase of frequency from 50-800 kHz. From the model used, we are able to correct the capacitance in irradiated MOS test structure and then we are able to confirm that an unwanted dielectric lossy layer formed at Si-SiO_2 interface with frequency in irradiated MOS test structure due to high interface trap density and leads to frequency dispersion effect in strong accumulation region at very high frequency (>100 kHz). After correction in capacitance, there is no frequency dispersion effect observed.

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Ajay K. Srivastava s/o Late Durga Prasad Srivastava and Madhur Srivastava was born in Azamgarh city (Uttar Pradesh), India, on 03rd August 1974. He did Ph.D. degree from the Department of Physics and Astrophysics, University of Delhi, India in 2007. His Ph.D. dissertation concerned with the "characteristics of silicon microstrip detector and study of some process in 14 TeV p-p interactions". He did mainly two dimensional numerical modelling of Si micro-strip sensor using 2-D T-CAD process simulator TMA SUPREM-4 and device simulator TMA MEDICI and I-V and C-V experimental measurements on silicon microstrip detector. At present, he is working as post-doctoral research scientist in the Institute of Experimental Physics, University of Hamburg, Germany from 2008. Now, he is involved in the two most prestigious high energy and photon science experiments i.e. Development of Si sensor for the large radii of a new CMS tracker for S-LHC at CERN, Geneva and XFEL (X-Ray Free-Electron Laser) experiment at DESY, Hamburg, Germany. He is doing two-dimensional numerical modelling for surface damage in MOS capacitor, segmented $p^+n^-n^+$ and $n^+n^-n^+$ Si sensors for the Adaptive Gain Integrating Pixel Detector (AGIPD) of the XFEL experiment at DESY, Hamburg, Germany and also perform numerical modelling on different test structures of strixel sensors for CEC (Central European Consortium within CMS). He has published and presented over than 14 papers in international journals, two CMS note, three national, more than twelve international conference proceeding. His current research interests are in the general area of the two and three dimensional semiconductor device (Si sensors) modeling and simulation using Synopsys TCAD and I-V and C-V experimental measurement on Si sensors.

Figure caption

Figure.1.a MOS test structure, where M is the metal contact, and the substrate is n-type Si. b) MOS equivalent high frequency model used. C_{ox} is oxide capacitance, C_D is depletion layer capacitance and R_{inft} and C_{inft} are the effective resistance and capacitance due to the surface states and interface trap density. R_{SD} (series resistance of the depletion region of MOS) is come from higher doping near to few microns from Si-SiO_2 interface during implantation and processing. R_{SB} (series resistance of bulk) and C_B (bulk capacitance) is considered when a high resistivity substrate is used.

Remark- no model parameters' taken for unwanted dielectric lossy layers formed at Si-SiO_2 interface of irradiated MOS test structure with frequency due to change of high N_{it}.

Figure.2a Equivalent Circuit for C/V_g taken in the parallel mode. b) Equivalent Circuit for C/V_g taken in serial mode.

Figure.3a. Simulated C/V_g characteristics for 0.5 MGy irradiated MOS test structure as a function of frequencies.

Figure.3b.Comparision of data and simulation - C/V_g characteristics for 0.5 MGy irradiated MOS test structure as a function of frequencies.

Figure.4. Comparison of data and simulation – C_{ma} versus frequency for 0.5 MGy irradiated MOS test structure.

Figure.5a. Simulated G/V_g characteristics for 0.5 MGy irradiated MOS test structure as a function of frequency.

Figure.5b. G_{ma} versus frequency for 0.5 MGy irradiated MOS test structure.

Figure.6. Serial capacitances (C_s) versus gate voltage, frequency are as running parameter.

Figure.7. Corrected capacitance versus gate voltage characteristics, frequency are as running parameter.

Table caption

Table.1: List of geometrical parameters.

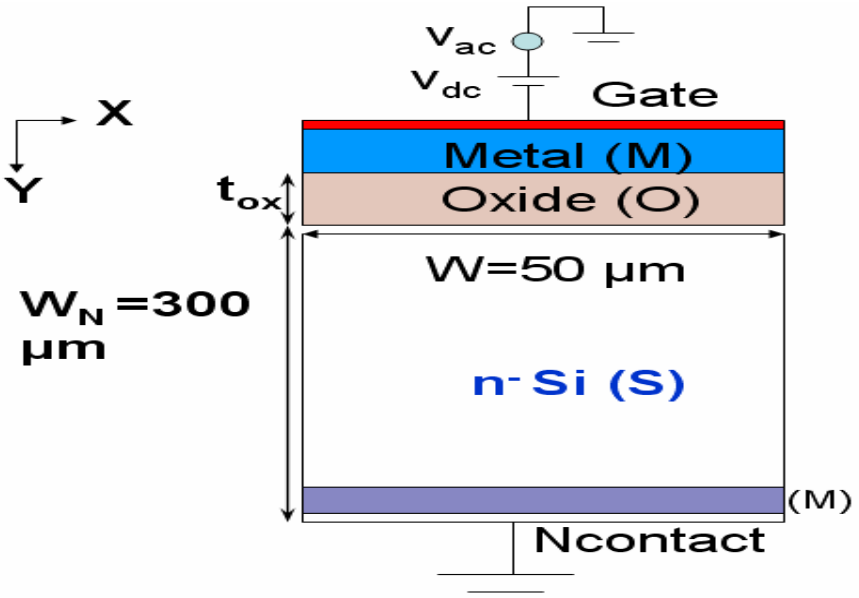
S.No.	Geometrical paramaters	Values
1.	MOS gate width(W)	50 μm
2.	Area of gate -experimental	0.404 mm^2
3.	Full volume of MOS test structure (2-D)	X=50 μm , Y=300 μm
4.	Default gate length (L) in 2-D simulation	1 μm

Table.2: List of physical parameters.

S.No.	Physical paramaters	Values
1.	Oxide thickness (t_{ox})	0.405 μm
2.	Time constant	130 μs
3.	fixed oxide charge (N_{ox})	≈ 0.5 MGy=2.48x10^{12} cm^{-2} (Experiment)- immediately after irradiation)
4.	Interface trap density (N_{it})	≈ 0.5 MGy=3.93x10^{13} cm^{-2} Level, E_C-E_t=0.4 eV from conduction band (Assumed)
5.	Gate voltage (V_g)	-65 volt
6.	AC voltage (V_{AC})	0.1V
7.	Frequency (f)	50-800 kHz

List of figures

Fig.1



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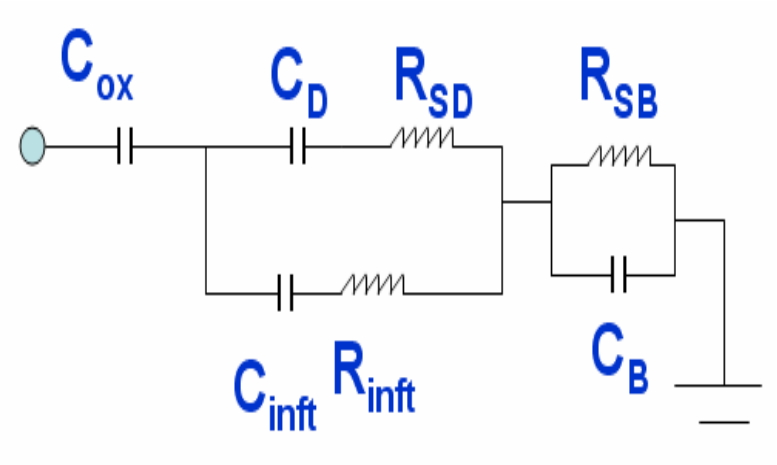
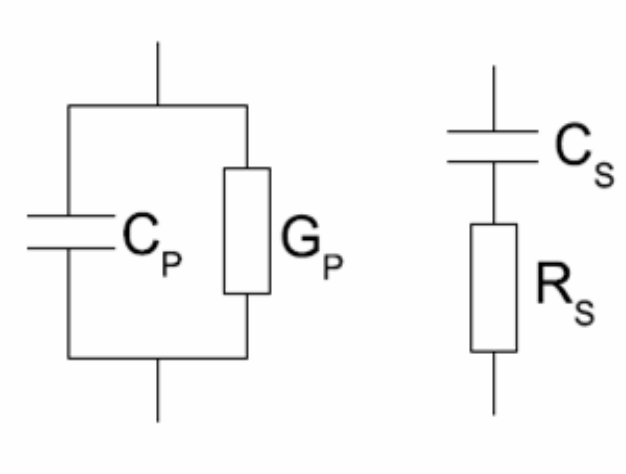


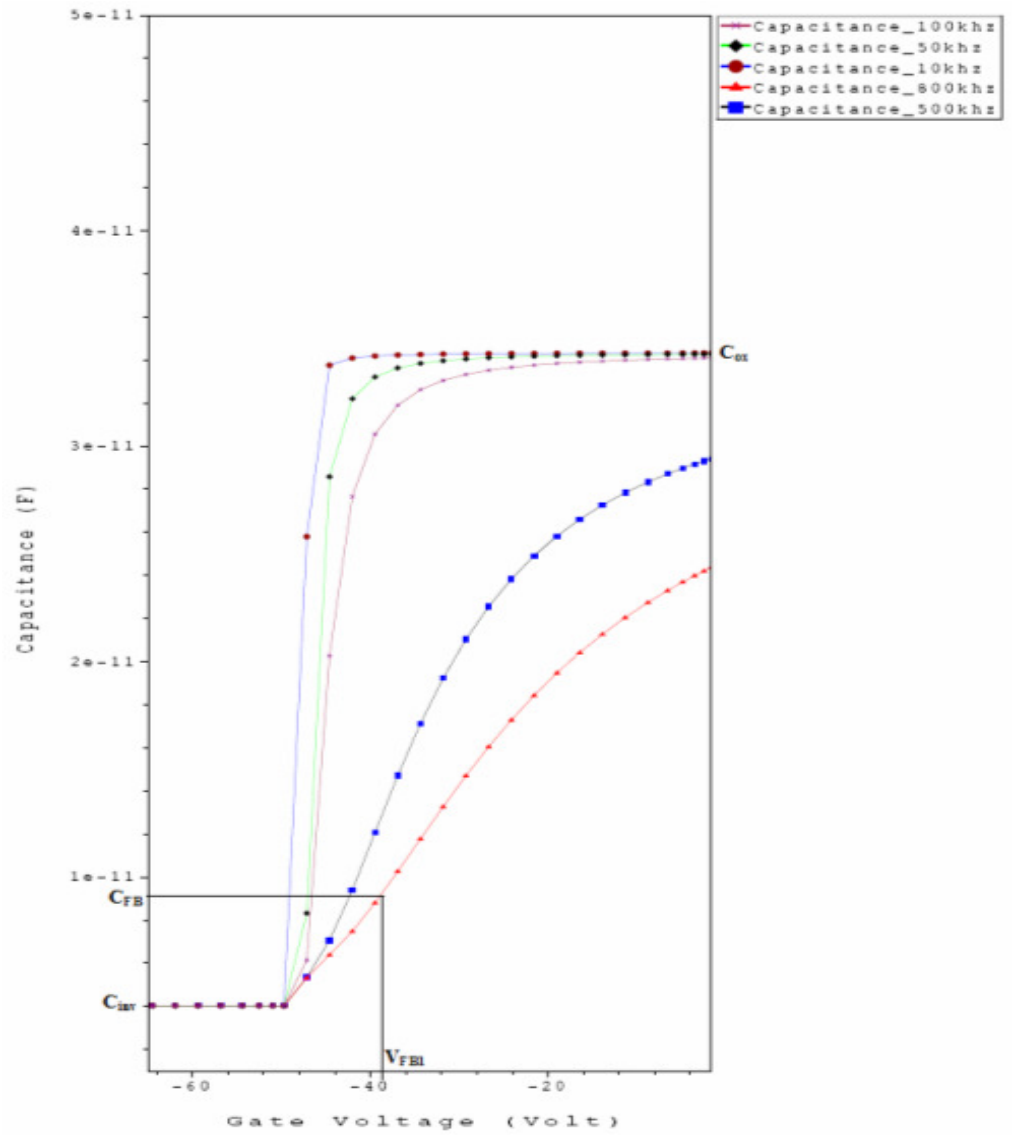
(b)

Fig.2



(a) (b)

Fig.3a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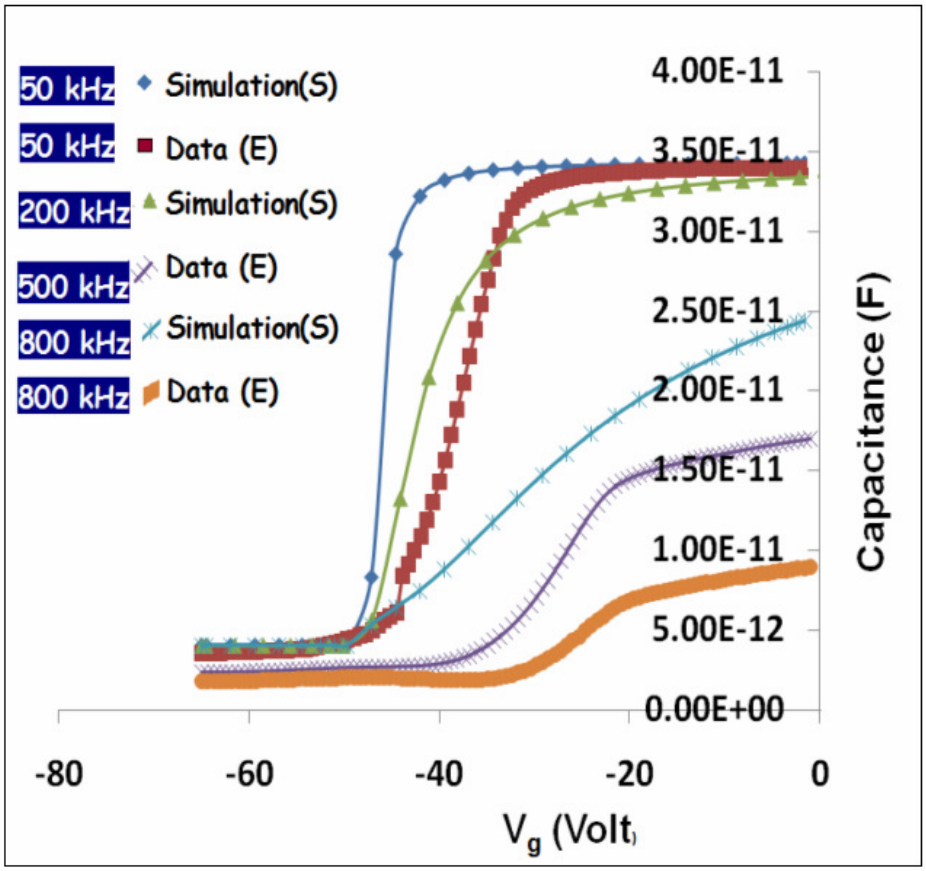
Capacitance_10khz
Capacitance_800khz
Capacitance_500khz
5e-11
4e-11
3e-11
2e-11
1e-11
Capacitance (F)
C_{ox}
C_{FB}
C_{inv}
V_{FB1}
-60
-40
-20
Gate Voltage (Volt)

Fig.3b


50 kHz
Simulation(S)
50 kHz
Data (E)
200 kHz
Simulation(S)
500 kHz
Data (E)
800 kHz
Simulation(S)
800 kHz
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4.00E-11
3.50E-11
3.00E-11
2.50E-11
2.00E-11
1.50E-11
1.00E-11
5.00E-12
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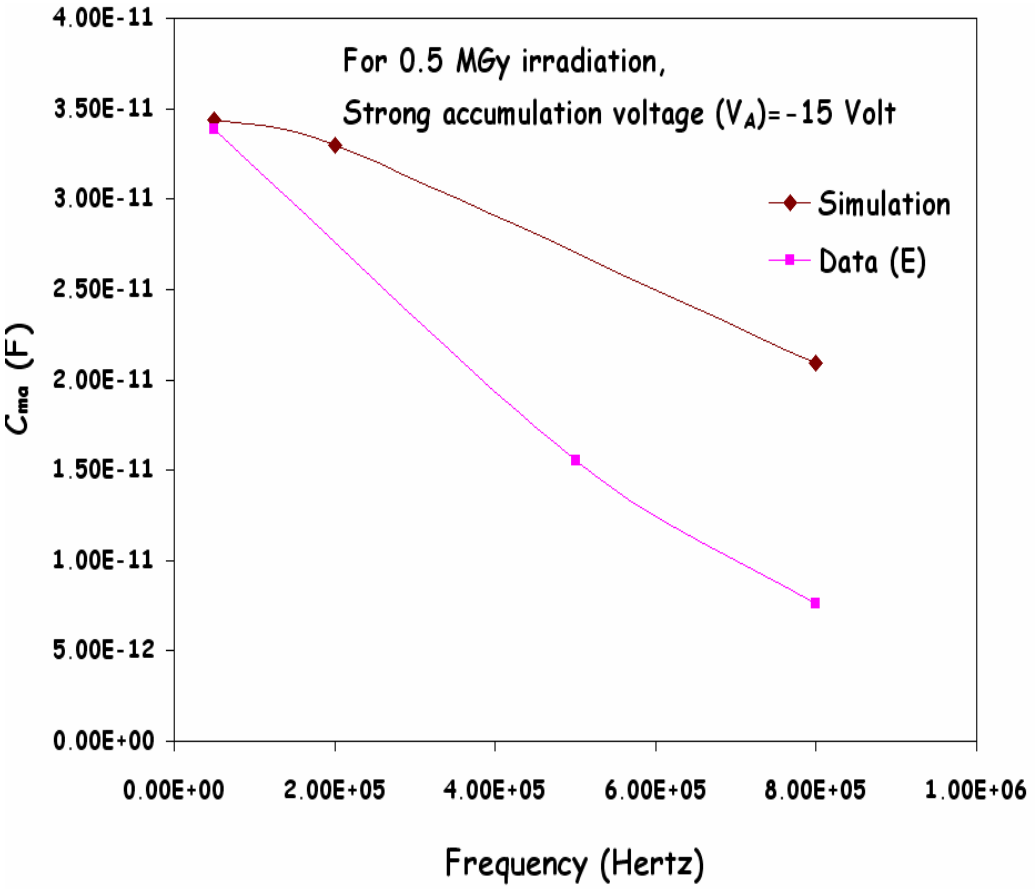
Capacitance (F)
-80
-60
-40
-20
0
Vg (Volt)

Fig.4


For 0.5 MGy irradiation,
Strong accumulation voltage (V_A)=-15 Volt
Simulation
Data (E)
C_{ma} (F)
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2.50E-11
2.00E-11
1.50E-11
1.00E-11
5.00E-12
0.00E+00
0.00E+00
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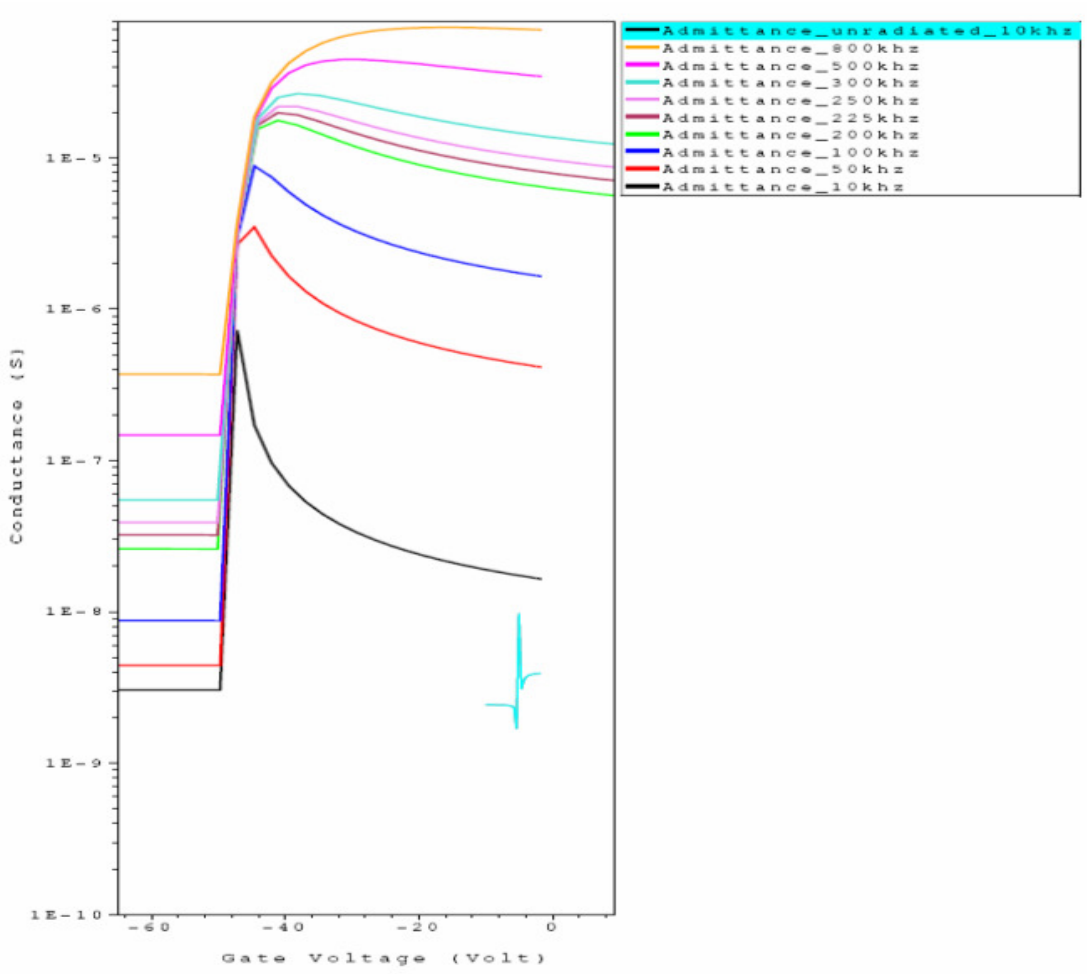
6.00E+05
8.00E+05
1.00E+06
Frequency (Hertz)

Fig.5a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Admittance_800khz
Admittance_500khz
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Admittance_250khz
Admittance_225khz
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Admittance_100khz
Admittance_50khz
Admittance_10khz
Conductance (S)
1E-5
1E-6
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1E-8
1E-9
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-60
-40
-20
0
Gate Voltage (Volt)

Fig.5b

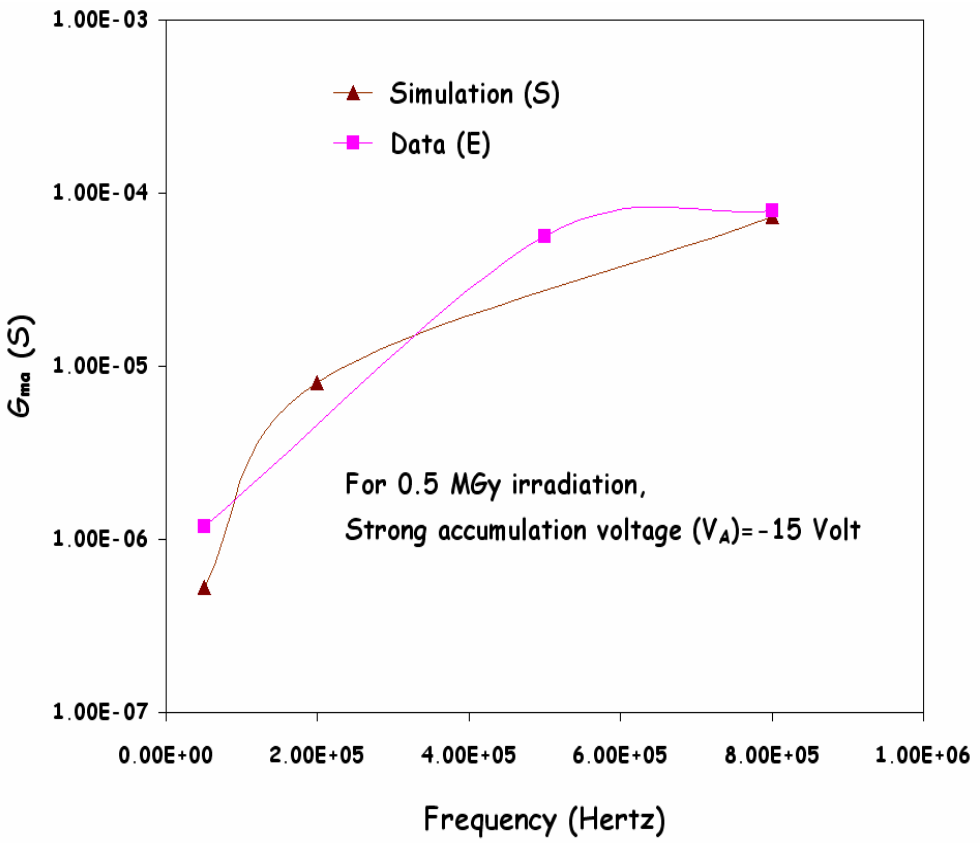
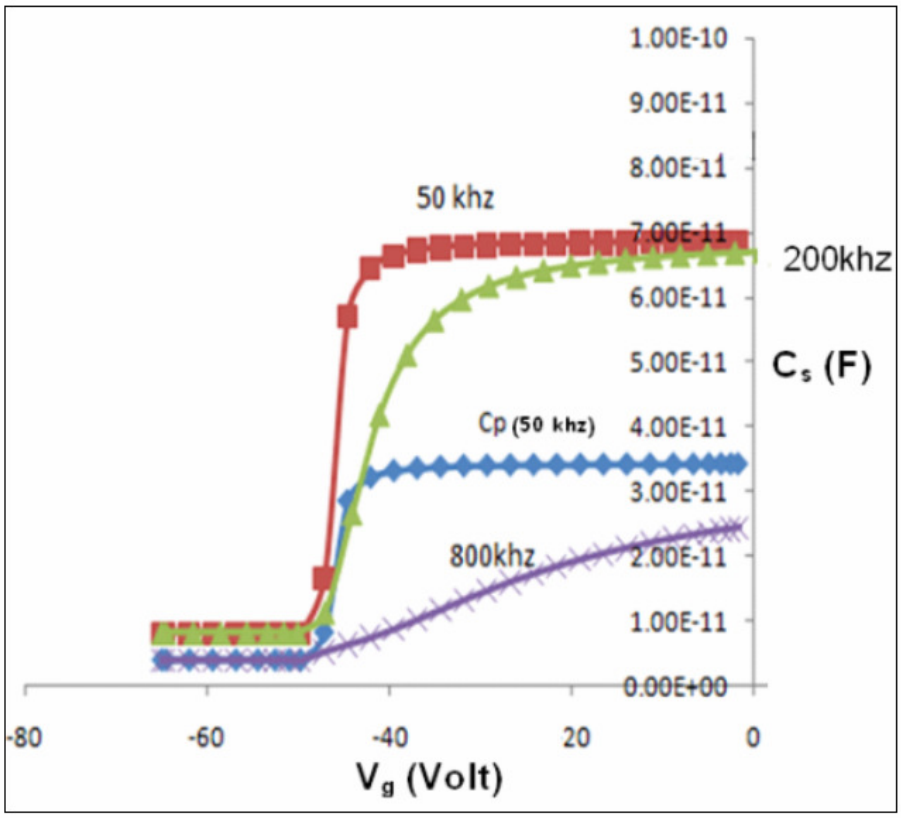

1.00E-03
1.00E-04
1.00E-05
1.00E-06
1.00E-07
G_{ma} (S)
Simulation (S)
Data (E)
For 0.5 MGy irradiation,
Strong accumulation voltage (V_A)=-15 Volt
0.00E+00
2.00E+05
4.00E+05
6.00E+05
8.00E+05
1.00E+06
Frequency (Hertz)

Fig.6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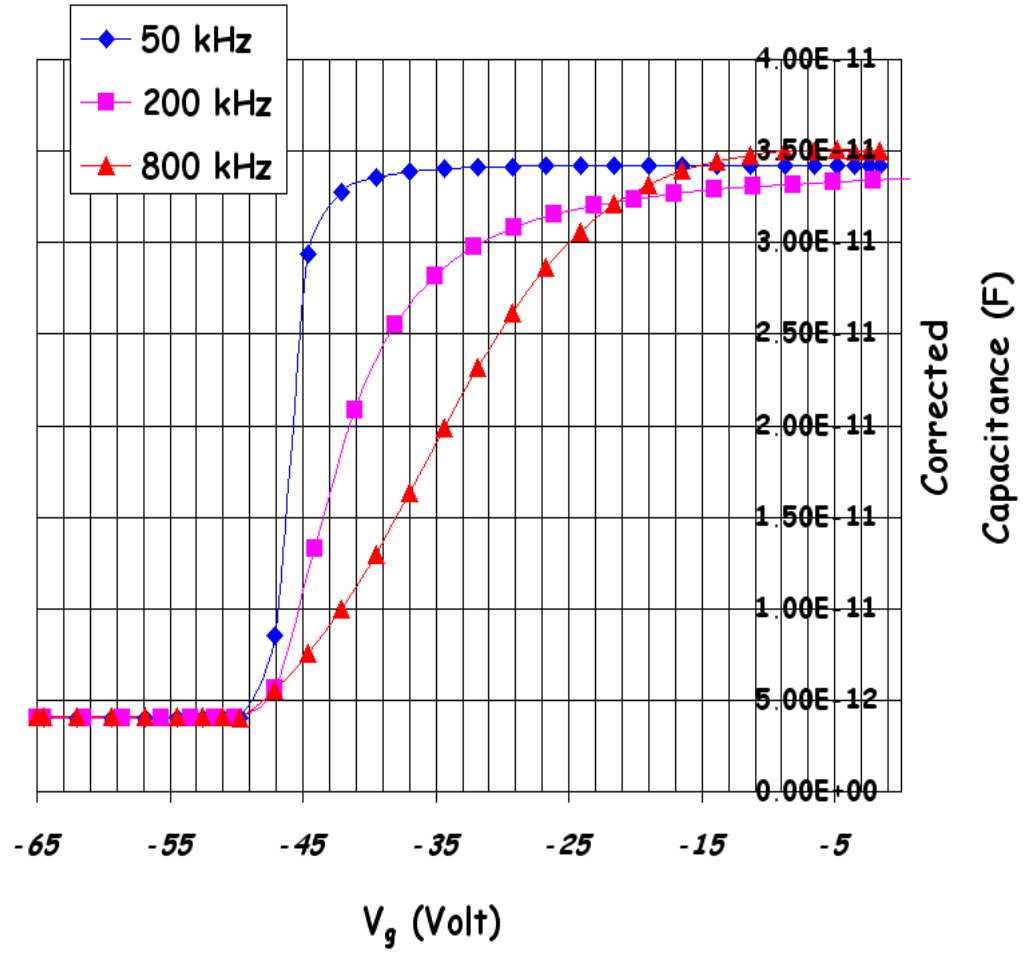
2.00E-11
1.00E-11
0.00E+00
50 khz
200khz
Cp (50 khz)
800khz
Cs (F)
-80
-60
-40
20
0
Vg (Volt)

Fig.7


50 kHz
200 kHz
800 kHz
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3.50E-11
3.00E-11
2.50E-11
2.00E-11
1.50E-11
1.00E-11
5.00E-12
0.00E+00
Corrected Capacitance (F)
-65
-55
-45
-35
-25
-15
-5
V_g (Volt)