Challenges in chip design for the AGIPD detector

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Abstract

AGIPD (Adaptive Gain Integrating Pixel Detector) is currently under development for the European X-ray Free Electron Laser (XFEL). It is a hybrid pixel detector with a specifically developed readout chip bump bonded to a silicon sensor. The chip is being designed in IBM 0.13 μm CMOS technology. This paper is focused on the readout chip design. The main challenges for this chip are: the high dynamic range (1 - 1.4×10^4) with single photon sensitivity, the long storage chain ($\geq$ 200) with a long hold time (99 ms), and the high radiation dose (up to 100 MGy). A charge integrating amplifier with a gain adaptive to the number of incoming photons is combined with a correlated double sampling (CDS) buffer to achieve the required dynamic range and single photon sensitivity. Several techniques are implemented in the storage cell design in order to reduce leakage current and signal-dependent charge injection. Four prototype chips have been designed for testing the performance of the implemented switches, capacitors, amplifiers, storage cells and periphery circuitry. The recently submitted test chip has a 16×16 pixel matrix , 100 storage cells in each pixel and a periphery circuitry for accessing and controlling the pixels and storage cells.

Key words:
hybrid pixel detector, CMOS, charge integrating, adaptive gain, correlated double sampling, X-ray free electron laser

1. Introduction

AGIPD is a classical hybrid pixel array detector with a silicon-sensor bump-bonded to a readout ASIC. Each pixel in the ASIC contains an analogue pipe-line for storing images at the 5 MHz XFEL repetition rate during the 600 μs bunch train, and a charge amplifier with a dynamic range of 1 - 1.4×10^4 incoming photons. The images stored in the ASIC are read out, digitized and written to mass storage during the 99 ms inter-train spacing.

The main challenges in the chip design arise from the readout amplifier and the storage chain:

1. The readout amplifier has to achieve the high dynamic range with the photon energy up to 15 keV. To detect the maximum number of photons, the gain of the readout amplifier has to be very small. However, to obtain single photon sensitivity, the gain has

to be very high and the noise of the amplifier has to be low.

2. The large storage depth per pixel ($\geq$ 200) asks for small storage capacitors because of the limited pixel size ($\leq 200 \times 200 \mu m^2$). However, the long hold time (up to 99 ms) and high analog resolution asks for large storage capacitor because of the dominant leakage current of the switches. Due to the strict requirement for leakage current, special approaches to minimize the leakage current have to be implemented.

3. The high radiation dose (up to 100 MGy) requires a radiation hard design. Although the employed IBM deep submicron CMOS technology (130 nm) is in favour of radiation hard designs thanks to its thin gate oxide (2.2 nm) [1], the radiation hard layout technique (i.e. enclosed gate layout) should be employed.

In the next section, the details of the chip are described. In section 3, the test chips and the measurement results are presented. At the end, we summarize the status of the project and draw conclusions.

2. Readout chip design

The readout chip has two main parts: pixel matrix and periphery circuitry. The details of pixel and periphery circuitry design are presented below.

2.1. Pixel design

The block diagram of the pixel is shown in Figure 1. The pixel consists of three parts: the readout amplifier, the storage chain, and the output buffer.
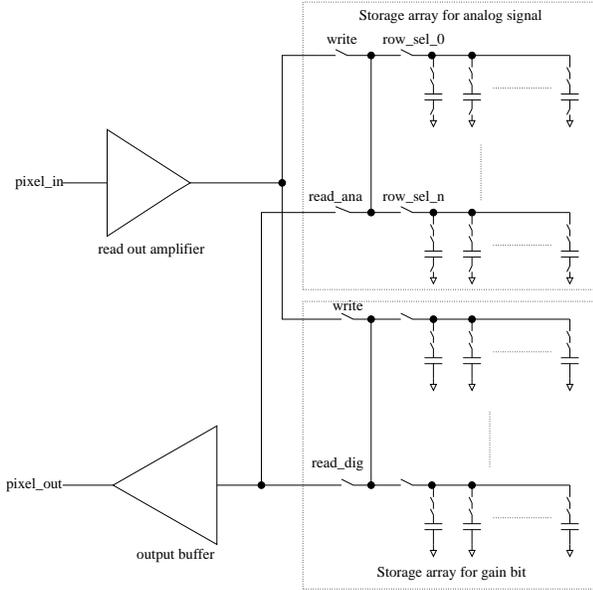

Figure 1: Block diagram of the pixel.
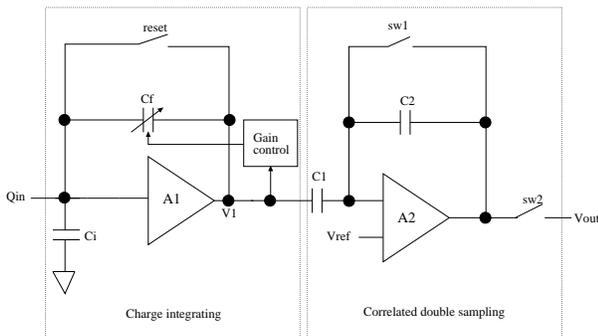
2.1.1. Readout amplifier

Figure 2: Readout amplifier.

The readout amplifier has to achieve high dynamic range with single photon sensitivity. One solution is to have a charge amplifier with a gain adaptive to the input charge [2]. The implemented amplifier is an adaptive gain charge integrating amplifier (CIA) cascaded by a correlated double sampling (CDS) buffer as shown in Figure 2. The output voltage V_{out} of the CIA is a function of the input charge Q_{in}, which can be expressed as:

$$V_1 = \frac{A_1 Q_{in}}{C_i + (1 + A_1)C_f} \simeq \frac{Q_{in}}{C_f} \qquad (1)$$

where C_i is the input parasitic capacitance including the sensor capacitance and the amplifier input capacitance, C_f is the feedback capacitance, and A_1 is the gain of the amplifier. The feedback capacitance C_f is adjusted by the block "Gain control" according to the output voltage of the CIA. In this way, the gain of the CIA is adapted to the number of the incoming photons. Before each bunch arrives and the generated charges are integrated, the CIA has to be reset through the switch "reset". The CDS buffer removes the low frequency noise of its input and provides an additional gain [3]. The output of the CDS buffer is expressed as:

$$V_{out} = V_{ref} + (V_{rst} - V_{sig})\frac{C_1}{C_2} \qquad (2)$$

where V_{rst} is the CIA output voltage just after the reset, V_{sig} is the CIA output signal just after the charge integration.

The analytical noise analysis of the readout amplifier shows that the CIA has a low pass noise transfer function. By increasing the capacitive load at the output of the CIA, more high frequency noise can be removed. The low frequency noise, mainly caused by the MOSFET flicker noise, is mostly removed by the CDS buffer.

The simulated output voltage of the readout amplifier as the function of the number of the input photon is shown in Figure 3. The simulated performance is summarized in Table 1. For the simulation, we assume that one photon (12 keV) generates 3000 electrons. The equivalent noise charge (ENC) is calculated based on the circuit noise simulations. In the region with the highest gain, single photon resolution is guaranteed because the ENC is much smaller than one photon. In the other two regions with lower gains, the ENCs are much lower than the Poisson statistical uncertainty of the incoming photons, therefore, the measurement precision is limited by statistical fluctuations of the input signal instead of the electrical noise of the amplifier.

It is well known that the leakage current of silicon detectors increases with irradiation. For the readout amplifier, a large leakage current can reduce the dynamic range and increase the output noise. Therefore, a leakage current compensation has to be implemented considering that the amplifier will work at high radiation

Table 1: Simulated performance of the readout amplifier with 12 keV photon.

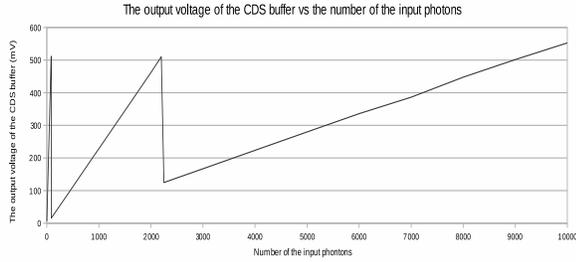| Number of photon	gain (mV / ph)	ENC (electron)	linearity error
1 - 85	5.99	143 (0.042 ph.)	0.6%
86 - 2220	0.23	2350 (0.71 ph.)	1%
2221 - 10000	0.055	15440 (4.6 ph.)	1.4 %

Figure 3: Simulated output voltage of the readout amplifier as the function of the input photon.

dose up to 100 MGy. Two leakage compensation approaches are implemented as shown in Figure 4. In the static leakage compensation scheme, a programmable current source at the readout amplifier input can be adjusted to compensate the leakage current. In the dynamic leakage current scheme, an opamp is used to form a negative feedback loop with the readout amplifier, such that the leakage current flows into the opamp instead of the readout amplifier. The calibration for leakage current compensation happens by switching on the switch "cal" during the 99 ms gaps between the photon bunch trains. After the calibration, "cal" is switched off and the opamp has no impact to the readout amplifier during the photon bunches except for the leakage current compensation.
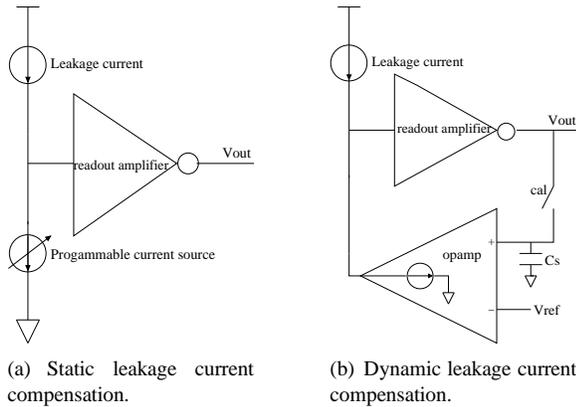

(a) Static leakage current compensation.

(b) Dynamic leakage current compensation.

Figure 4: Leakage current compensation schemes

2.1.2. Storage cell

The main challenge of the storage cell design is the switch because the leakage current of the switches is much higher than the leakage of the capacitors. During the sampling phase (less than 200 ns), the switch should have a small on-resistance for charging the sampling capacitor. During the holding phase (99 ms in the worst case), the switch should have a large off-resistance to keep the signal error caused by the leakage current less than 1% . Two kinds of storage cells are designed as shown in Figure 5. The passive storage cell consists of only passive capacitors and switches. The active storage cell contains an opamp to force the two terminals of the switch, which is connected to the top plate of the storage capacitor, to the same voltage, so that the leakage current over the switch is minimized. For both kinds of storage cell, the switch connected to the bottom plate of the storage capacitor helps to reduce the signal-dependent charge injection.
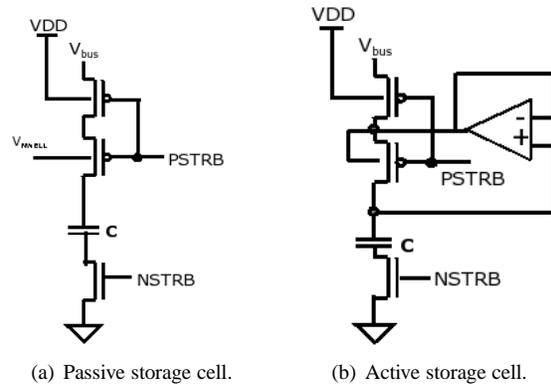

(a) Passive storage cell.

(b) Active storage cell.

Figure 5: Implemented storage cells.

2.2. Periphery circuitry

The main functions of the periphery circuitry are:

1. Addressing the pixel matrix and the storage cell matrix in the pixel.
2. Providing the control signals and biasing signals needed for the pixels.

3

3. Buffering the output signals to be read out of the chip.

Two approaches are usually used for pixel and memory addressing, i.e. shift register based addressing logic and decoder based addressing logic. Shift register in general is faster and smaller in area compared to a binary encoded state machine, which is usually used for decoder based addressing logic. However, decoder based addressing logic allows random access to any pixel or memory cell.

2.2.1. Shift register based addressing logic

With one shift register each, for column addressing and row addressing, the pixels and the memory cells can be easily accessed sequentially. In the simplest way, only one clock signal is needed if the shift registers are cascaded by connecting the clock input of the next one to the data output of the previous one. This addressing approach has been used in many pixel detectors, such as the Pilatus detector [4].

2.2.2. Decoder based addressing logic

A typical binary decoder is a combinatorial logic circuit with n address inputs and 2^n outputs. Depending on the value of the address input, only one output will be selected. The decoder based addressing logic is usually slower, has more input signals, and needs more area compared to the shift register based addressing logic.

2.3. Test chips

Four prototype chips have been produced for testing. The first chip contains capacitors and transistor based switches. The measurement of this chip shows the following results:

1. DGPMOS (thick oxide PMOS transistor) switches are usable for radiation dose up to 1 MGy. DGN-MOS (thick oxide NMOS transistor) switches and ZVTDGNMOS (zero threshold DGNMOS) are usable for radiation doses beyond 100 MGy.
2. The leakage currents of the switches are dominant over the leakage current of the capacitors (MIM capacitor and thick oxide MOSFET capacitors).
3. Cooling the chip from 20°C to −30°C can reduce the leakage current by 46% .

The second test chip contains several variations of the readout amplifier. The third chip is intended to test the storage cells. The last test chip contains a 16×16 pixel matrix with 100 storage cells in each pixel and a periphery circuitry with the shift register based addressing logic. Figure 6 shows the layout of the last chip.
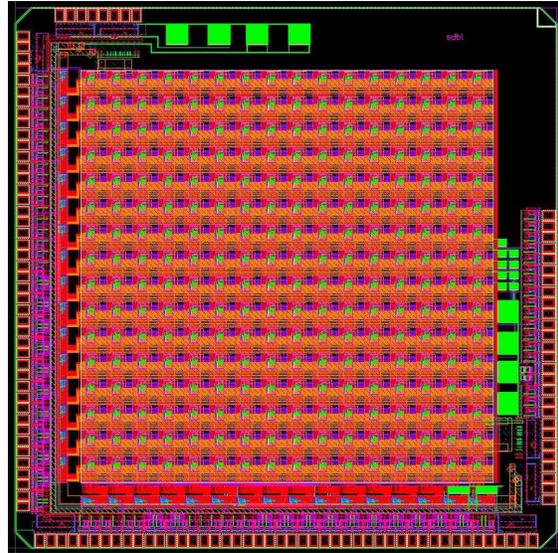

Figure 6: A prototype test chip with a 16 x 16 pixel matrix and 10 x 10 storage cells / pixel.

3. Conclusions

In this paper, we focused on the design of the readout chip for the AGIPD detector. We addressed the design challenges and studied the approaches to overcome the challenges. The circuit simulation of the implemented readout amplifier showed good performances to cover the high dynamic range with single photon sensitivity. Four prototype chips have been designed to characterize the performance of the switches, the capacitors, the readout amplifier, the storage cells and the periphery circuitry. The measurement of the first test chip provided useful information about the switches and capacitors under irradiation.

Acknowledgements

References

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