

Fig. 1. Schematic of the proposed pixel cell.

protein data base¹). A more fundamental understanding of the structure–function relationships of membrane proteins would make invaluable contributions to structural biology, pharmacology and medicine.

The ability to record detailed diffraction patterns from single molecules would eliminate the need for crystalline samples.

3. Requirements

AGIPD is foreseen to be used for both, CDI (on biological as well as on inorganic samples) and for X-ray photon correlation spectroscopy (XPCS).

For CDI an angular resolution of 0.1 mrad is required, which corresponds to a pixel size of 200 μm (for a sample to detector distance of 2 m). The visualized image has a high dynamic range from single photon resolution up to 20,000 photons. In terms of radiation damage this means that over three years of operation the detector will accumulate a dose of 1 GGy. This dose has to be sustained by both, ASIC and sensor without serious deterioration.

The European XFEL bunch structure requires the images to be stored with a 5 MHz repetition rate in the ASIC during the 0.6 ms bunch train. Whereas in the 99.4 ms intertrain spacing all stored events have to be readout, digitized and written to mass storage [2].

4. AGIPD detector system

Adaptive gain integrating pixel detector (AGIPD) is one of three detector development projects approved by the European XFEL project team. The development is done in a collaboration between DESY, the University of Hamburg, the University of Bonn (all Germany) and the Paul Scherrer Institute (PSI) in Switzerland.

AGIPD is based on the hybrid pixel technology. A newly developed ASIC will feature in each pixel a dynamic gain switching amplifier (to cope with the high dynamic range) and an analogue pipeline capable of storing the pictures at the desired 5 MHz speed. The high data throughput of such detectors also requires the development of a specific DAQ system.

The hybrid approach has the advantage that several developments can be divided over the four participating institutes in a

modular way. While DESY does the overall project coordination, part of the ASIC design, the mechanics plus the interface and backend electronics, the PSI and the University of Bonn are in charge of the dynamic gain switching and pipeline development. Bump bonding and the interconnection between Sensor and ASIC and the system calibrations will be done at PSI.

The University Hamburg is in charge of the sensor development.

In the following we give an overview of the planned detector and the current state.

4.1. ASIC design

Each pixel in the ASIC has to cover a dynamic range from single photon sensitivity to 4×10^4 coincident photons. This high dynamic range cannot be implemented on a single gain stage—to detect the maximum number of photons, the gain of the readout amplifier has to be very small. However, to obtain single photon sensitivity, the gain has to be very high and the noise of the amplifier has to be low. Thus, a self-regulating, adaptive gain switching mechanism is employed.

The charge is subsequently stored in an analogue pipeline with the 5 MHz XFEL repetition rate during the 600 μs bunch train. The large storage depth per pixel (≥ 200 images) calls for small storage capacitors because of the limited pixel size ($200 \times 200 \mu\text{m}^2$). However, the long hold time (up to 99 ms) and high analogue resolution favors a large storage capacitor because of the leakage current of the switches and the capacitor itself.

The high radiation dose (up to 100 MGy) requires a radiation hard design. The employed IBM deep submicron CMOS technology (130 nm) with its thin gate oxide (22 nm), yields a radiation tolerant design, however, radiation hard layout technique will be employed [5].

The basic architecture of the pixel cell will consist of an integrator with selectable feedback capacitors and an analogue storage pipeline (Fig. 1). Selecting feedback capacitors with different sizes will enable the adaption of the integrator to a large dynamic input range. The baseline configuration of such a pixel cell allows individual programming of the integrator gain to adapt to the expected photon intensity. In case the expected flux range is unknown, the feedback capacitors will be switched dynamically during the charge integration. In this adaptive gain switching (adaptive slope integration) mode the used gain setting has to be stored along with the data.

¹ <http://www.rcsb.org>

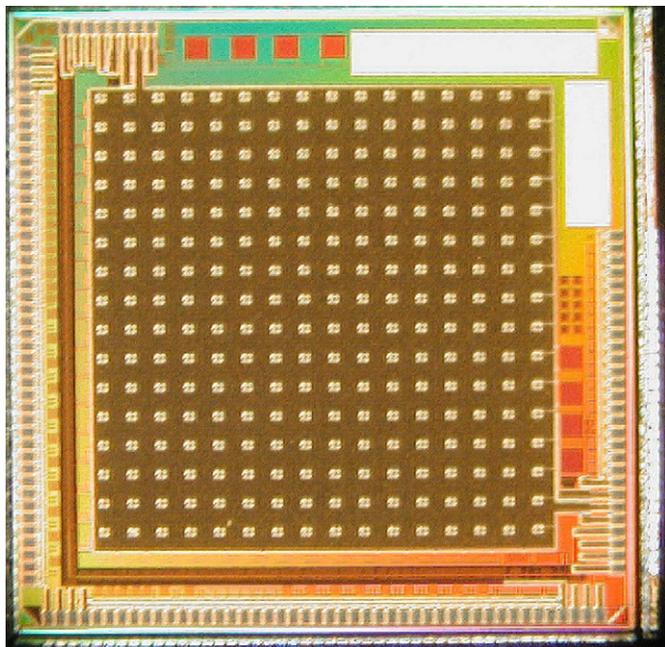


Fig. 2. Photograph of the AGIPD 0.2 pixel chip with a 16×16 matrix.

The analogue pipeline will store the integrator output voltages on sampling capacitors. It is foreseen to implement 200–400 capacitors in each pixel cell ($9 \mu\text{m}^2$). First floor plan estimations indicate that this is feasible with a pixel area of $200 \times 200 \mu\text{m}^2$. The pipeline steering logic will also include the processing of a fast “veto” signal, which tags a “bad frame” not to be stored in the pipeline. In order to identify critical components, a simulation of both the scientific experiments and the detector response was started [6,7]. Crucial is the understanding of noise contributions from the gain switching and the charge losses in the pipeline.

4.2. MPW designs

Since the project uses a relatively new technology, with 8 metal layers, and since the concept has many sensitive components, it was decided to test critical issues with multi-project wafer (MPW) runs. So far, four test chips were designed to pursue different fields of investigation.

A precarious problem is up to 99 ms charge storage without ungovernable charge loss. The first chip (HPAD 0.1) was dedicated to study critical circuit performance before and after irradiation. It showed that the main issues stem from the p–n junction leakage and revealed no additional mechanisms for radiation induced oxide leakage.

On HPAD 0.2 eight different sampling cells were designed in conjunction with eight pipeline cells that are operated by an advanced control circuit.

AGIPD 0.1 [8] has several preamplifiers with different leakage compensation strategies to find the optimal circuit suited to deal with the increasing leakage current due to radiation effects.

Finally, AGIPD 0.2 [8] combines all test structures to a 16×16 pixel matrix with an architecture close to the target design, designed to operate at the 5 MHz repetition rate, it is hosting a 100 cell storage pipeline in each pixel plus the periphery circuitry with the shift register based addressing logic. A suited single chip pixel sensor is designed in parallel ready to be bump bonded. This chip is also considered to indicate the final architecture for the detector and its performance parameters (Fig. 2).

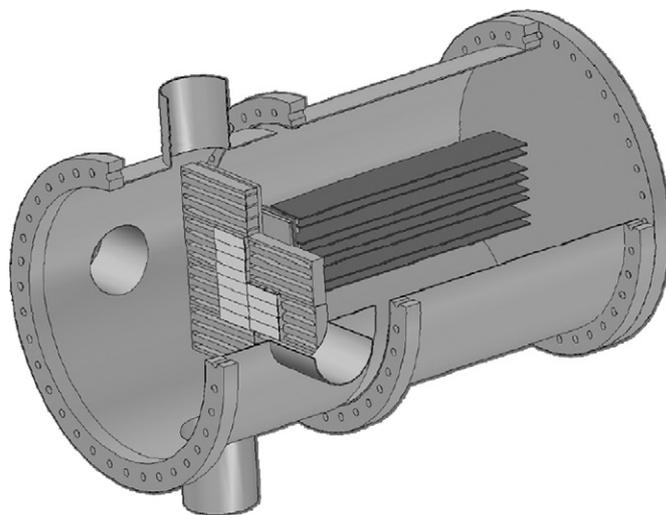


Fig. 3. Module mechanics and assembly.

4.3. Interface electronics

The interface electronics connects the chip control and readout with the XFEL data acquisition system. It provides the power, static signals and control patterns for the chips. Furthermore it is responsible for evaluation of the gain setting and dispatches the ADC conversion. It also provides a 10 GB Ethernet connection to the control electronics to allocate enough bandwidth to sustain the required high data throughput. Each ASIC has 16 parallel readout channels. On each channel the analogue charge information of several pixel pipelines are chained together feeding the ADC. The interface electronics board will host 64 ADC converters to deal with the data volume. A suitable converter has a precision of 14 bit with 50 Mbit/s.

4.4. AGIPD mechanics

An array of 2×8 ASICs are bump bonded to a monolithic pixelated silicon sensor. Bump bonding will be performed at PSI using the well developed in-house technology [9].

A high density interconnect (HDI), a highly flexible PCB provides the wire-bond pads for voltages, chip-stimuli and data signals. It will act as an intermediate between ASICs and interface electronics. Module mechanics, HDI and the ASICs together with the sensor form an AGIPD module. These modules will be mounted on cooling plate quadrants that can be sheared with respect to each other creating an adjustable central hole for the direct beam. In a first step a one megapixel detector can be built out of 16 modules with the prospect of later enlargement.

The drawing in Fig. 3 shows the conceptual mechanics design. Interface electronics (in dark grey) and modules are separated by a vacuum tight barrier. This allows easy access and maintenance of the interface electronics boards and simplifies the cooling of the power consuming ADCs.

5. Conclusion

We have presented the conceptual design of the AGIPD detector, identifying the critical components. First results have proven the validity of many of the components.

References

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