

# The Search for Si-XIII - an Unidentified High Pressure Phase of Si

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In the semiconductor manufacturing industry a typical wafer flow comprises several hundred individual processing steps and the wafer can visit up to 250 process tools. The wafer can travel on a journey of ~10-15 km during its process lifetime. Wafer handling is a critical operation during which micro-crack damage to silicon wafers can be introduced and this damage can be exacerbated by thermal processing resulting in catastrophic total wafer breakage during high temperature processing. It is estimated that for every silicon fabrication line producing between 20,000 300mm or 50,000 200 mm wafers per month the cost of repair, clean-up and tool down-time is >\$7M per annum at the 180nm node, rising to > \$120M per annum at the 22nm node.

Damage to silicon wafers is often introduced by misaligned wafer handlers and grippers, a process which can be simulated with great success by controlled laboratory-based nanoindentation experiments. Indentations create areas of high stress that result in phase changes to the crystal structure and the crystalline structure of these phases can play a vital role in the initiation, acceleration or retardation of the fracture process. Basically, as the crystalline FCC silicon in a typical wafer is subjected to damage induced stresses and thermal processing (wafers are annealed up to 1000 °C) a sequence of different phases of silicon are produced during stress loading/unloading, thermal ramp up/down, thermal ramp rates and the nature of the stress [1]. During the stress unloading regime from approx. 12 GPa to 2GPa, and upon heating to above 470 K, the typical Si-III changes first to an as yet unidentified phase of silicon known as Si-XIII [2,3]. Si-XIII can then transform to either a diamond hexagonal structure Si-IV or to amorphous Si [2,3] before reverting back to the normal room temperature cubic diamond structure, Si-I. It has to be noted, that this kind of wafer damage occurs in an open system and therefore the Si high pressure phase transformations happen under dynamic and non-hydrostatic conditions and the equilibrium phase diagrams are not valid [4].

To find the stability range of the unidentified Si-XIII a number of experiments at the "Extreme Conditions Beamline (ECB) P02.2" at "P02 Hard X-ray Diffraction Beamline" of PETRAIII were performed in a 1st campaign under hydrostatic, quasi-hydrostatic and non-hydrostatic conditions at room temperature. The data from 13 successful runs with loading up to 40 GPa are still under evaluation. Preliminary results are:

- Powdered B-doped Si-wafer and pure Si standard powder show the same behaviour.
- Nano-Si powder behaves similar but with less intensity because of high amorphous portion, which is important for the phase transitions where amorphous Si is involved.
- As a function of loading/unloading rate, certain Si-phases develop at different pressures.
- The identification of these phases is currently underway.

## References

- [1] V. Domnich and Y. Gogotsi, Rev. Adv. Mater. Sci. 3, 1 (2002).
- [2] A. Kailer, Y. Gogotsi, and K. G. Nickel, J. Appl. Phys. 81, 3057 (1997).
- [3] D. Ge, V. Domnich, and Y. Gogotsi, J. Appl. Phys. 95, 2725 (2004).
- [4] H. Katzke, U. Bismayer, P. Tolédano, Phys. Rev. B73, 134105 (2006).